



Progress of LHCb ECAL Upgrade II Studies

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LHCb Upgrade II



 New detector proposed for LHCb during Runs 5 and 6 of the LHC to ingrate 300 fb⁻¹ of data at the end of the LHC



Detector for Upgrade II

• Same performances as Run 3, with a pile-up of 40 instead of 6



Run 3

Run 5

- Same geometry for the detector with innovative technologies for sub-detectors and data processing
- Main elements:
 - Increase granularity
 - Add timing measurement (resolutions up to 10-50 ps)
 - Radiation hardness (up to 10¹⁶ n_{eq}/cm²)
 - Data rate: 200 Tb/s



Détecteur pour Upgrade II



Current LHCb ECAL and upgrade lb

- Current ECAL operating at $\mathcal{L} = 2 \times 10^{33} \text{ cm}^{-2} \text{s}^{-1}$
 - Shashlik technology:

 $4\times4/6\times6/12\times12\ \text{cm}^2$ cell size in inner/middle/outer region







Constant term [%] at the end of 2025 (28/fb)

- Radiation hard up to 40 kGy
- ECAL in upgrade <u>Ib</u>
 - The inner part need to be replaced due to performance degradation



ECAL Upgrade (PicoCal): Granularity

- Improve efficiently performaces at high luminosity
- Reorganize ECAL zones in rhomboic shapes to follow better the radiation and occupancy maps
- Five zones with cells of different sizes: (1 module = 1 bloc of 12x12 cm²)
 - 1.5x1.5 cm²: 32 modules (type SpaCal-W) 2048 cells
 - 3x3 cm²: 144 modules (type SpaCal-Pb) 2304 cells
 - 4x4 cm²: 448 modules (type Shashlik) 4032 cells
 - 6x6 cm²: 1344 modules (type Shashlik) 5376 cells
 - 12x12 cm²: 1344 modules (type Shashlik) 1344 cells
- **Baseline option** = Add longitudinal segmentation at shower maximum (separation electron/hadron) in all cells
- One cell = 2 channels for readout (1 front and 1 back)
 - Total of 30208 voies
- Descoped option = No longitudinal segmentation in outer modules (4x4 cm², 6x6 cm², 12x12 cm²)



PicoCal: Precise time measurement

- To fight again the large background due to pile-up: add time measurement in ECAL with a precision of 15 ps = PicoCal
- Select cells where $|t_{ECAL} t_{PV}|/\sigma(t) < 3$
 - t_{PV}: collision time measured in other detectors (VELO for example)
 - t_{ECAL} : time measured in the ECAL, corrected from time of flight
 - σ(t) : ECAL time resolution
- Participations of French and Chinese institutes:
 - Performance studies with simulation in particular to compare baseline and descoped options
 - R&D and characterisation of new modules
 - R&D of new electronics



0.4

0.2

í٥

0.4

0.2

0.6

0.8

Normalised Signal Efficiency

1.2

7

ECAL Modules

Ongoing R&D to produce modules allowing a precise time measurement and a relative energy resolution of 10%/sqrt(E)
 SHASHLIK:





W absorber, cristal fibers (GAGG, gadolinium aluminium gallium garnet): High radiation tolerance and small Molière radius

Pb absorber, polystyrene fibers



Current modules: external reg

Optimisation of GAGG scintillators

➤Good scintillator for innermost part of PicoCal

- ✓ Radiation-hard
- ✓ High density
- \checkmark High light output and fast decay time



✓Collaborate with SIPAT to reduce decay time by tuning composition and doping Decay time at cost ofight output ~5k/MeV acceptable

✓High-quality scintillator fibres and samples obtained







Optimisation of GAGG scintillators

➤GAGG samples characterisation at CERN & PKU

✓ Results feedback to SIPAT to iterate



Now decay time between 15 – 20 ns; light output ~10k/MeV
 R&D still ongoing

3D-printing tungsten (W) absorber

➤W has small radiation length and small Moliere radius

- >3D-printing technology to ease W matrix production
- ➤Collaboration with LaserAdd to produce W absorber
 - ✓ Good samples obtained
 - Good roughness needed not to scratch fibres
 - High density

✓ Characterisation W samples, feedback results to LaserAdd to opti











Sood roughness $R_a \approx 4 \,\mu m$ achieved, can smoothly insert fibres

≻Density (units: g/cm³)

Pure W	LaserAdd
19.3	18.9

Prototype SPACAL-W+GAGG

≻New prototype in construction

 ✓ 3 pieces of 3D-pinted tungsten absorber of 12 × 12 × 5 cm³ produced by LaserAdd



- ✓ 4x4 cells (1296 holes) equipped by → GAGG fibers from SIPAT
- Further cells will be equipped with fibers from other producers later for time resolution studies
- \checkmark Double-sided readout
- ➤ Testbeam at SPS this June



Prototype schematic



Resolution studies with full simulation



Performance studies with full simulation

 \succ Benchmark channel: $B^0 \rightarrow K^{*0}\gamma$



 ✓ Larger background level with downscoped PicoCal setup (worse time resolution)



Reconstruction algorithm development

A new reconstruction algorithm is being developed to take into account the longitudinal segmentation (i.e. Layered reconstruction)





*Shift of seed cell from front to back section



*Position resolution with single-photon:large improvement with new algorithm

> The algorithm is promising to improve π^0 reconstruction efficiency



Electronics for PicoCal

• Architecture:



- Readout with PMTs
- Two separate paths with dedicated ASIC developed in parallel, with the same technologiy (TSMC 65 nm), running at 40 MHz:
 - Time ASIC (SPIDER): waveform TDC in analog memories (R&T IN2P3, Orsay/Clermont-Ferrand/Lyon/Caen/Nantes) (dynamic range of $E_T = 50$ MeV to 5 GeV, resolution 15ps RMS)
 - **Energy ASIC** (Barcelone, Valence), measurement of the integrated charge at 40 MHz over 12 bits with two gains (dynamic range between $E_T = 0$ and 40 GeV)

Mesure du temps: Waveform Digitizing

- Time measurement is done by sampling the signal shape using analog memories and a FPGA: development of a dedicated ASIC called SPIDER
- Time is computing using:
 - A counter (~1 ns step), **DLL2**
 - A DLL to define the region of interest (~100 ps step)
 DLL1
 - Samples on the signal shape: Cell banks
- The interpolation in a FPGA allows to measure the time with a precision of a few ps RMS with a precise calibration even with signals with small amplitudes.
- The main disadvantages that must be addressed in the new SPIDER chip:
 - Large deadtime (~ 100 μs) limiting usage at high rate (goal = 40 MHz) => ADC massively parallel to reach at least 50% occupancy
 - Need of a trigger: every channel is self triggered



- 10-bit Wilkinson ADC at 5 GHz
- Memory cells (switches/capacitors) with ~0.8V dynamic range and noise level ~0.5mV RMS
- DLL between 40 and 640 MHz
 First prototype Automne 2024 (final version end 2029)





Conclusions

- Common activities in Chinese and French groups about LHCb ECAL Upgrade :
 - R&D for new modules with GAGG fibers
 - Performance studies with simulation
 - Design of ASIC to measure timing precisely
- In the near future:
 - Test beams at DESY and SPS to measure module characteristics
 - First prototype of electronics
- On the longer term:
 - Full production of innermost ECAL modules
 - Full production of Front-End electronics
 - Implementation of algorithms in FPGA to improve calorimeter reconstruction

Backup