中国科学技术大学
University of Science and Technology of China

MAPS R&D for the STCF Inner Tracker

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On behalf of the STCF ITKM working group

USTC

CHiP Cross-Strait Workshop on Advanced Detectors and Technologies
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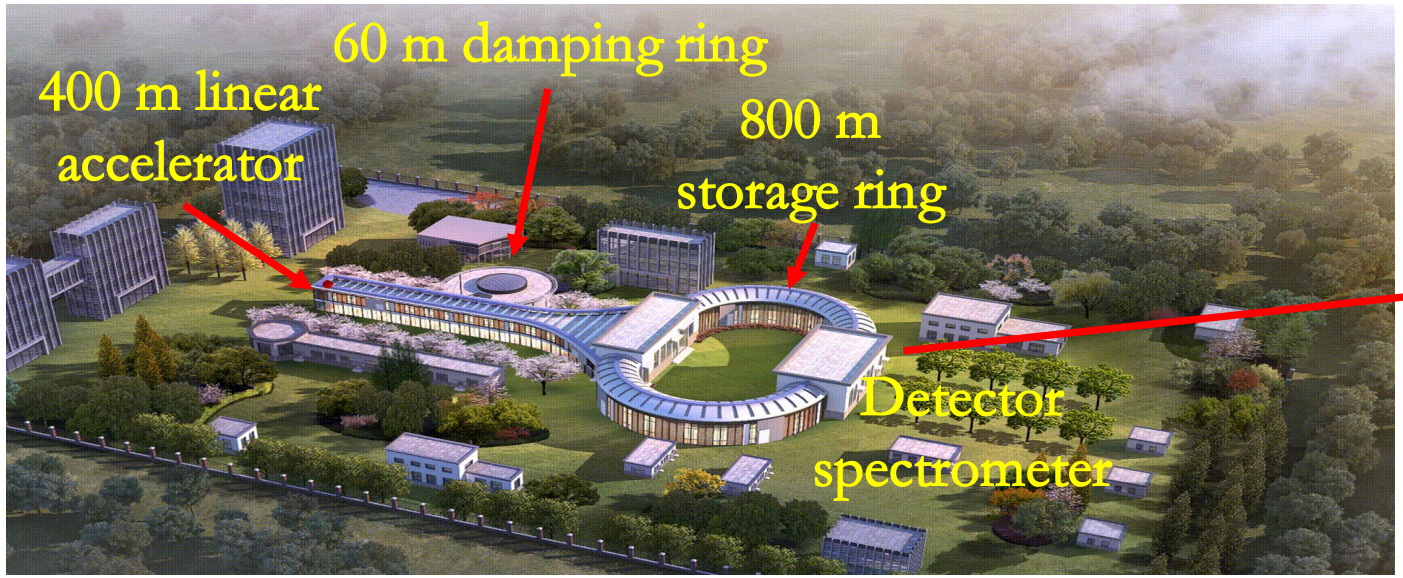
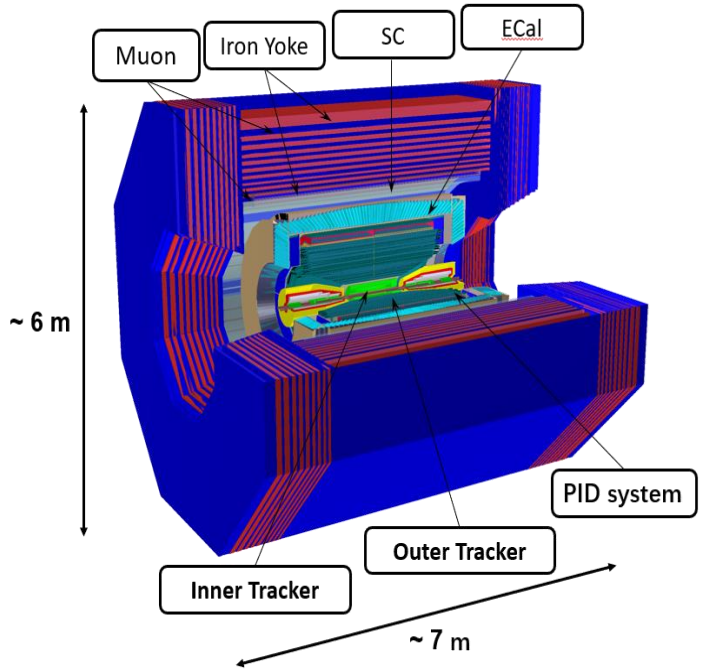
Super Tau-Charm Facility

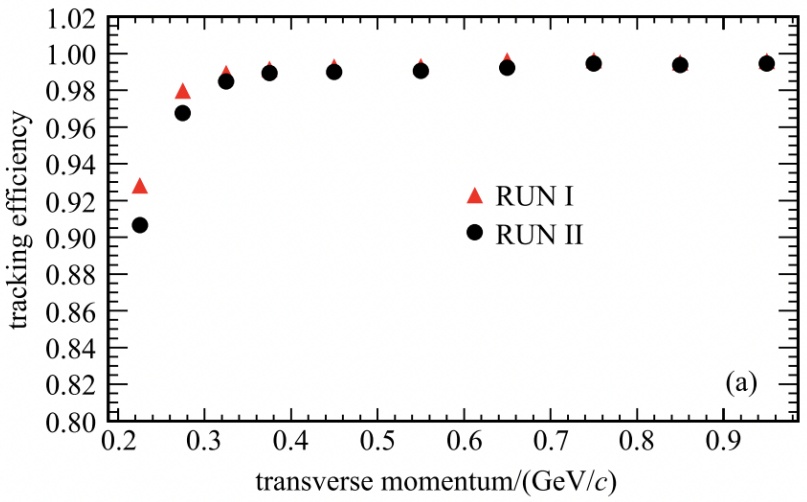
- **STCF: next generation e^+e^- collider in China:**
  - Center-of-mass energy: **2-7 GeV**
  - Peak luminosity: **> 5×10^{34} $cm^{-2}s^{-1}$ at 4 GeV**
  - Collision data: more than **1 ab^{-1}/y**
  - With potential to further **increase luminosity** and **beam polarization**

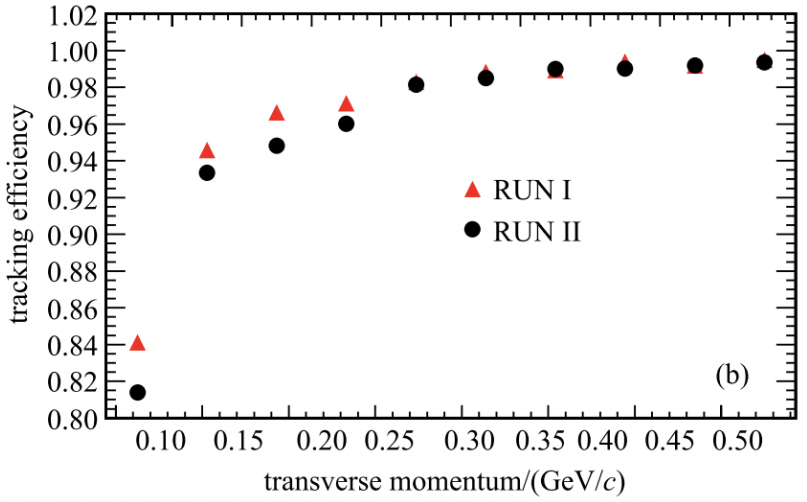


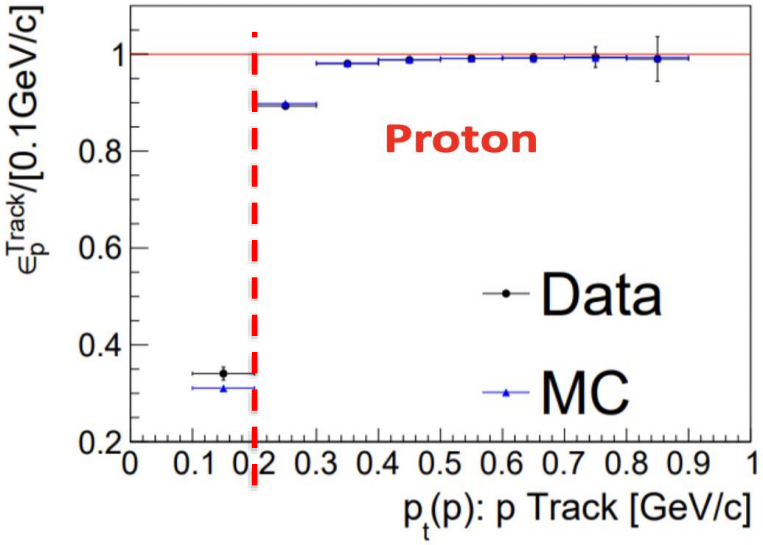


Detector Considerations for ITK

- The challenge at the low p_T region
  - For BESIII, the tracking efficiency drops sharply below 100MeV
- There is strong physics motivation to go to low p_T region







BESIII tracking efficiency, Chin.Phys.C 40 (2016) 2, 026201

Detector Considerations for ITK

- Physics requirements
  - No stringent requirements on vertexing
  - The main challenge is the tracking at the low momentum region (p_T < 100 MeV)

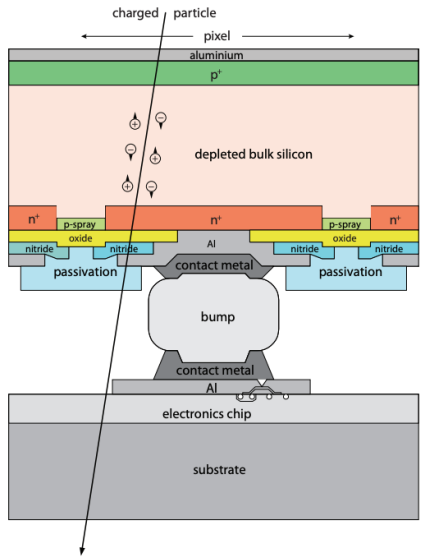
Process	Physics Interest	Optimized Sub-detector	Requirements
$\tau \to K_s \pi \nu_\tau$,	CPV in τ sector,		acceptance: 93% of 4π; trk. effi.:
$J/\psi \to \Lambda\bar{\Lambda}$,	CPV in hyperon sector,	Tracker	> 99% at $p_T > 0.3$ GeV/c; > 90% at $p_T = 0.1$ GeV/c
$D_{(s)}$ tag	Charm physics		$\sigma_p/p = 0.5\%$, $\sigma_{\gamma\phi} = 130\ \mu$m at 1 GeV/c

- Tracking challenges at low p_T
  - Momentum resolution: Multiple Coulomb scattering
  - Track reconstruction efficiency
- Low material budget is essential to satisfy the physics requirements

CMOS Pixel Sensors

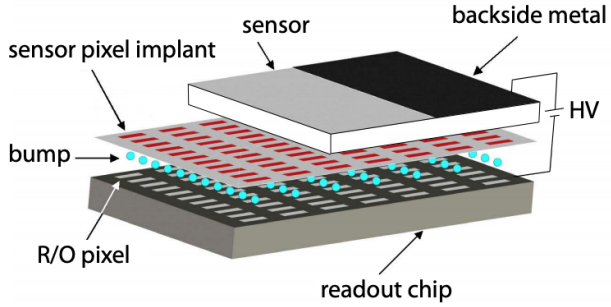
❖ Hybrid pixels

- Sensor and readout circuit can be optimized separately
- Widely used in ATLAS/CMS
- Disadvantages:
  - Relatively large material budget
  - Hybridization: complex, expensive



(a) Hybrid pixel

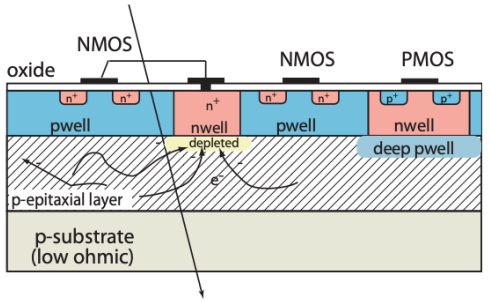
arXiv:1705.10150v3



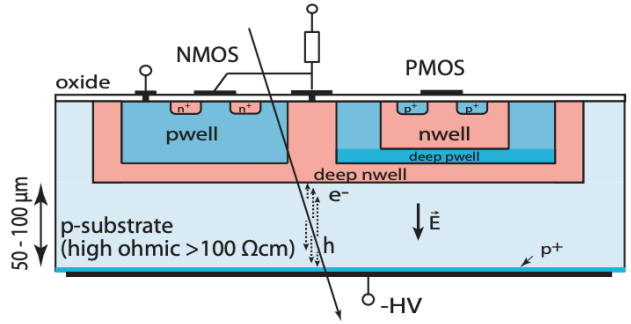
(b) Pixel matrix

❖ Monolithic active pixel sensors (MAPS)

- Easier integration, lower cost
- Potential of low material budget
- Adopted in STAR and ALICE ITS2



(a) MAPS

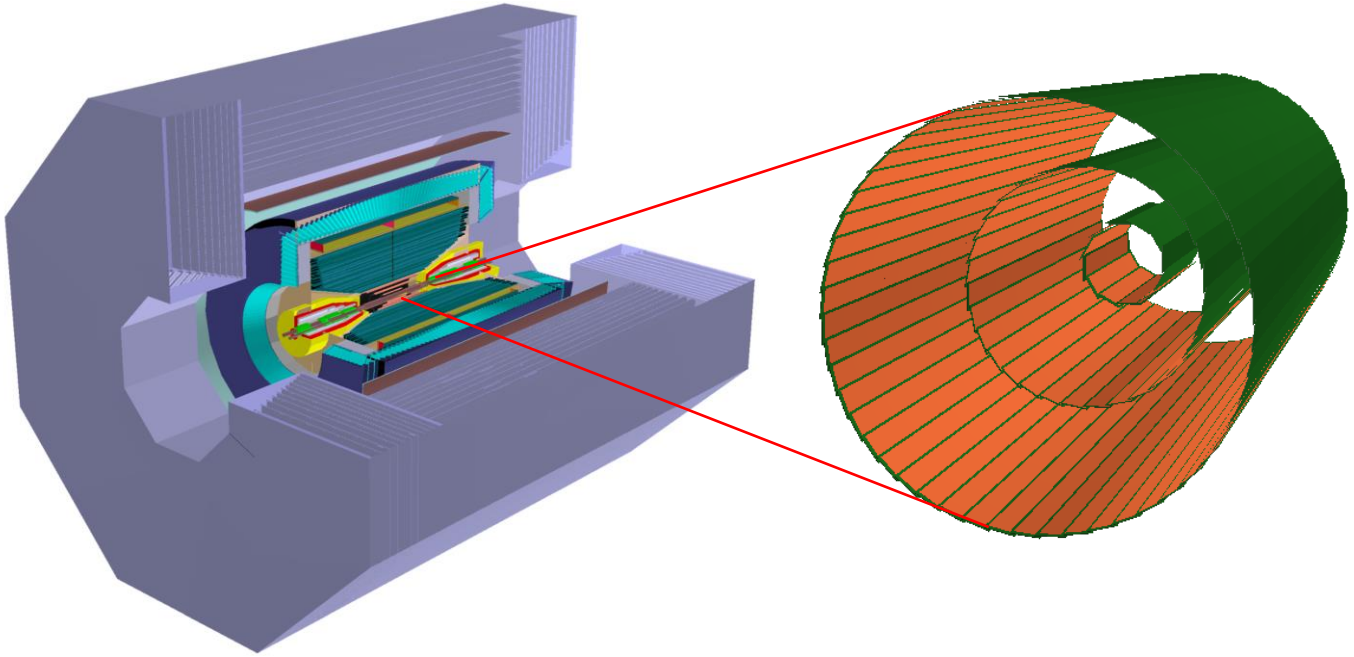


(b) DMAPS

MAPS is a viable solution for STCF ITK and a small fill-factor design is preferred

Conceptual Design

- A preliminary design of the MAPS based Inner Tracker (ITKM)
  - An alternative option to the MPGD based Inner Tracker (ITKW)
- Three layers of silicon pixel detectors, with radii of 36mm,98mm,160mm
  - Beam pipe radium: 30mm
- Acceptance: polar angle of 20°~160°
- Total area: 1.3m^2



Layer	Radius (mm)	Length (cm)	Area (cm^2)
1	36	19.78	447.46
2	98	53.85	3315.87
3	160	87.92	8838.63

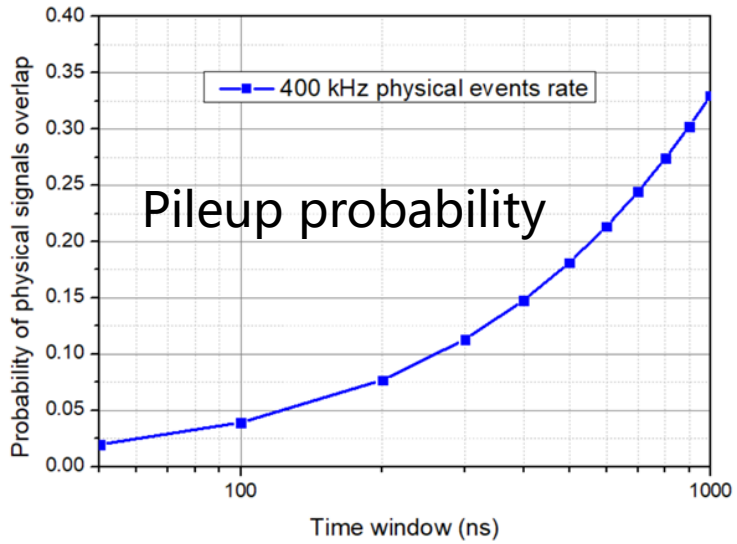
- Geometry/layout still being optimized
- Might extend to 4 or more layers

Design Targets

- Requirements on the MAPS based Inner Tracker
  - Spatial resolution: $\leq 100\mu m$
  - Material budget per layer: $\leq 0.3\%\ X_0$
  - Power consumption: $\leq 100 mW/cm^2$
  - Time resolution: $\leq 50\mathrm{ns}$ (to deal with the pileup issue at high luminosity)
  - Time-over-threshold (TOT) measurement:
    - Time-walk correction
    - Correction of multi-coulomb scattering in track finding

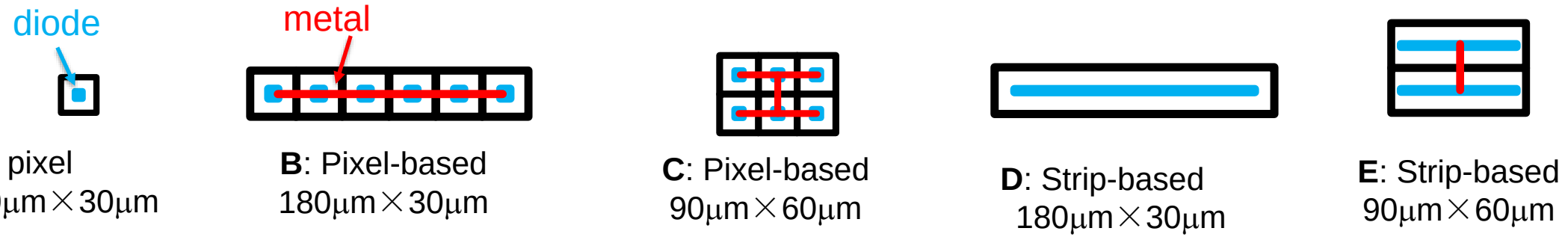
High event rate at STCF

Physics Process	Cross-section (nb)	Rate (Hz)
$\sqrt{s} = 3.097$ GeV, $\mathcal{L} = 0.75 \times 10^{35}\ \mathrm{cm^{-2}s^{-1}}$, $\Delta E = 0.848$ MeV		
J/ψ	4500	337500
$\rightarrow e^+e^-$	270	20000
$\rightarrow \mu^+\mu^-$	270	20000
Bhabha ($\theta \in (20°, 160°)$)	734	55000
$\gamma\gamma$ ($\theta \in (20°, 160°)$)	36	2700
$\mu^+\mu^-$	11.4	900
Hadronic from continuum	25.6	2000
2γ process ($\theta \in (20°, 160°)$, $E > 0.1$ GeV	~23.3	1740
Total	~5300	~400000



Sensor Design

- Pixel size considerations
  - Higher priority on the power consumption than the spatial resolution → larger pixel size to reduce the power consumption density
  - The ALPIDE sensor is already optimized and proven experimentally → keep the sensor geometry as close to ALPIDE as possible
    - Pixel-based: analog connected small pixels $(1 \times 6 \rightarrow 1, 2 \times 3 \rightarrow 1)$ using metal lines
    - Strip-based: extended diode size in one direction
    - A 3rd option also under design: digital connected small pixels



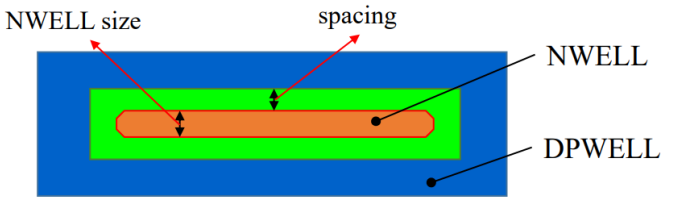
Alternative CMOS Technologies

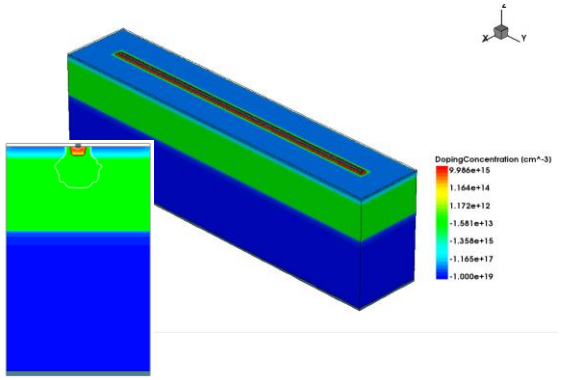
- Usually MAPS is based on high-resistivity epitaxial wafers
  - Resistivity: $\gtrsim 1\mathrm{k}\Omega \cdot cm$; epi thickness: ~20 μm
- Other options are also being considered, based on available technologies in domestical foundries
  - Low resistivity epi wafers:
    - Resistivity: $\gtrsim 10\Omega \cdot cm$; epi thickness: 10~20 μm
  - High resistivity substrates:
    - Resistivity: $\gtrsim 1\mathrm{k}\Omega \cdot cm$, no epi layers

TCAD Simulation

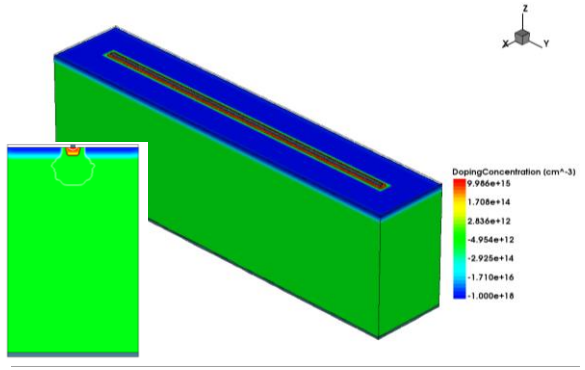
- TCAD simulation setting
- Pixel size: 170μm × 30μm
- NWELL size 2μm
- NWELL-DPWELL spacing 2μm
  - HR epi: 20μm 1kΩ·cm + 30μm substrate
  - HR substrate: 50μm
  - LR epi: 10μm 1kΩ·cm + 40μm substrate
  - Modified-TJ180nm (N-blanket design)
  - Modified-TJ180nm with pstop

Doping profile

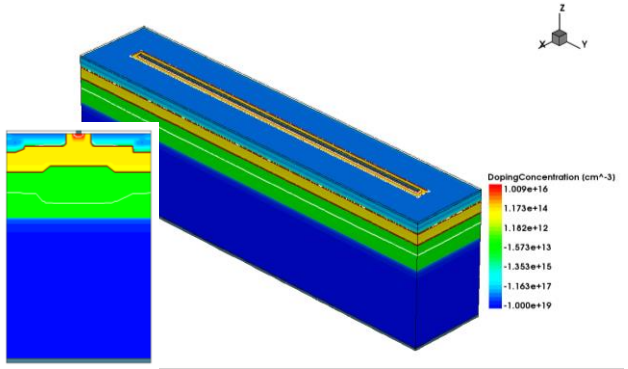




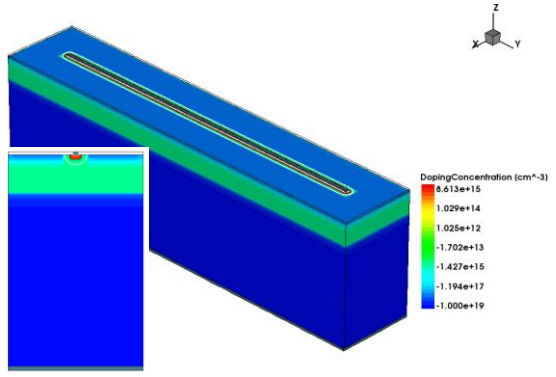
HR epi (TJ180nm)



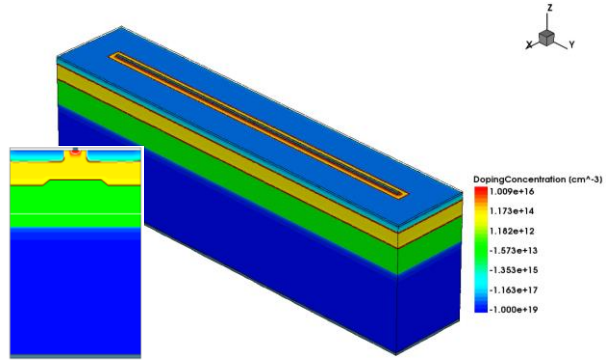
HR substrate



Modified-TJ180nm pstop



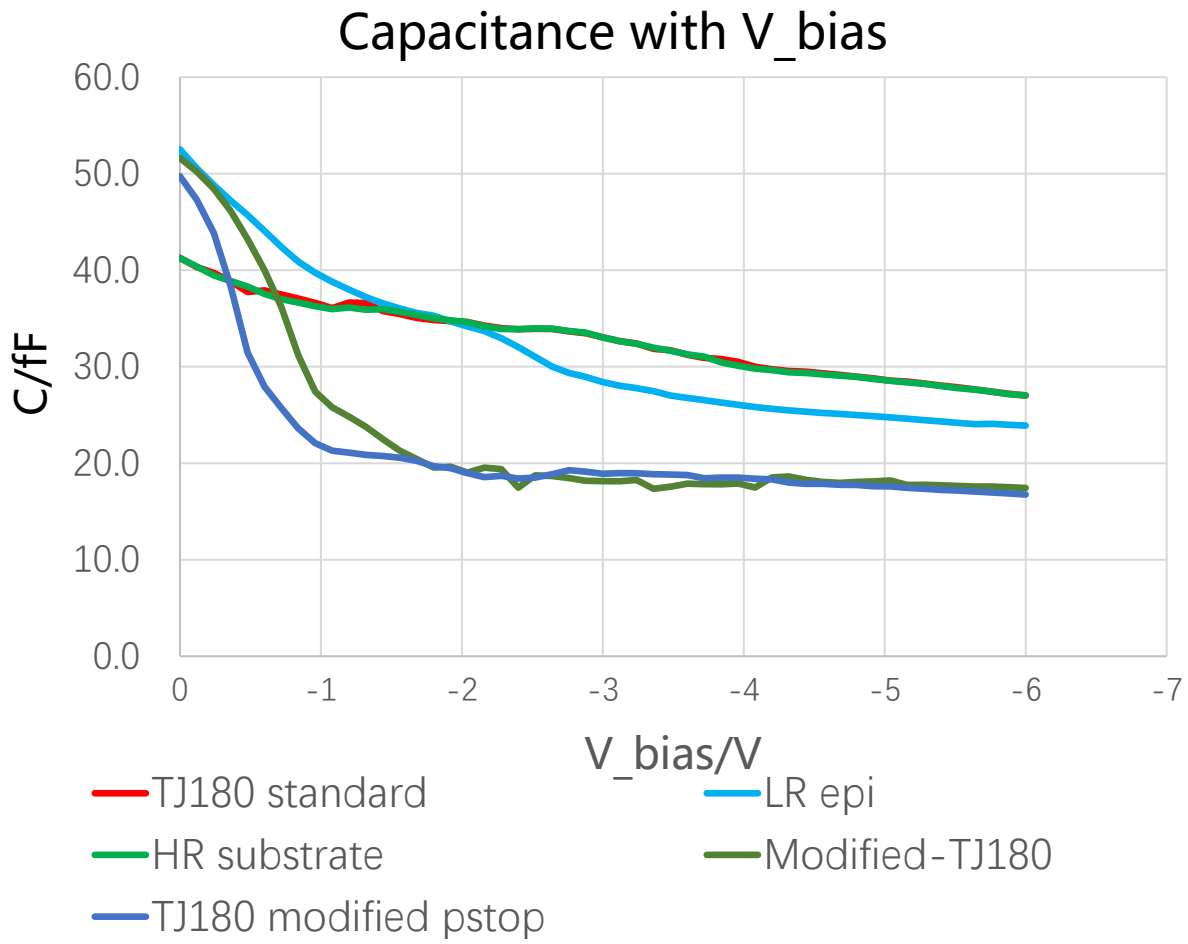
LR epi



Modified-TJ180nm

Sensor Capacitance Simulation

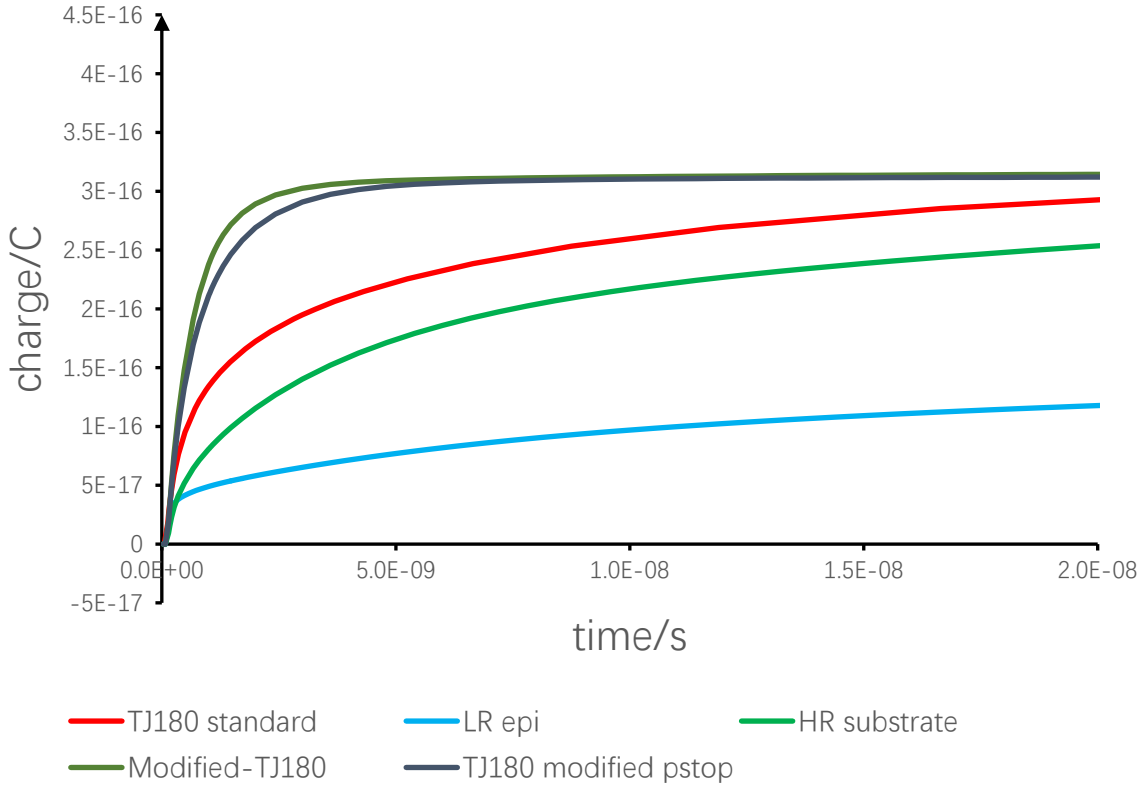
❖ Nwell voltage set to 0.8V, substrate voltage scanned from 0 to -6V



Charge Collection Simulation

- Ionization density 80$e^-/\mu m$
- Ionization injection from center of pixel

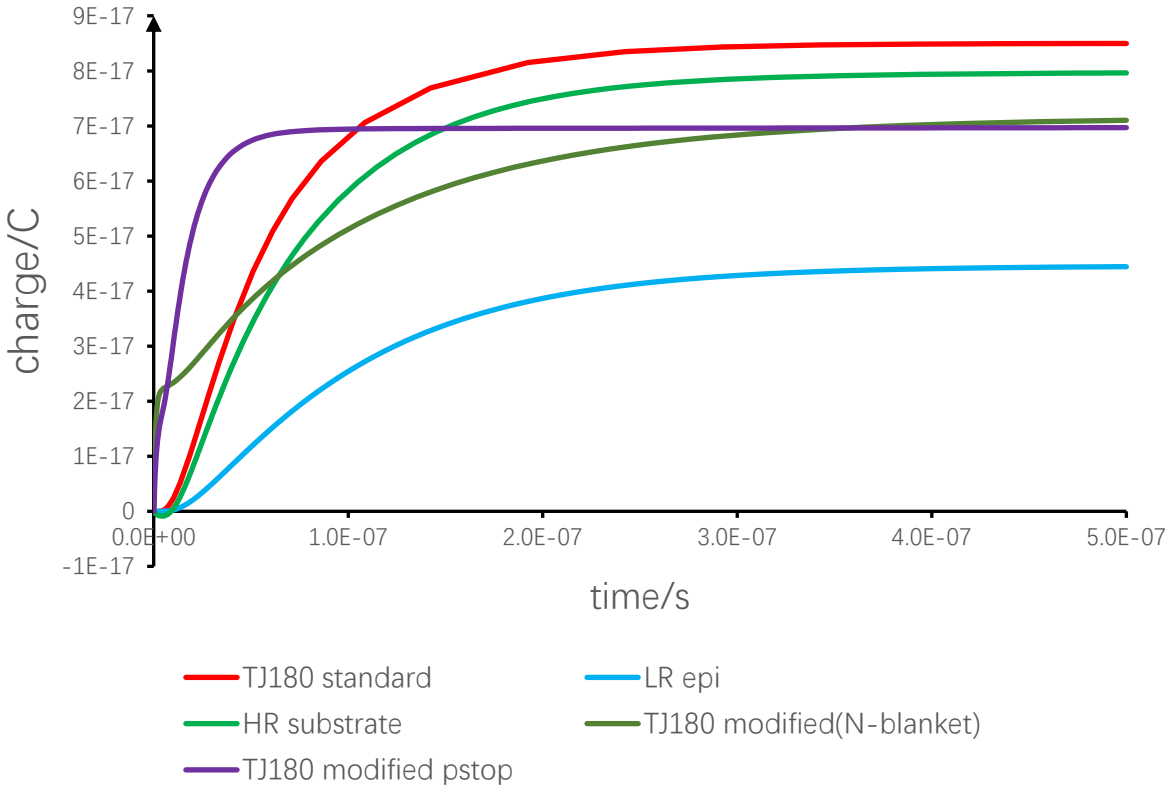
	Collected charge (e)	Collection time(ns)
HR epi (TJ180nm)	**2039.81**	**20.56**
HR substrate	**2477.65**	**89.72**
LR epi	**1089.64**	**74.57**
Modified-TJ180nm	1969.85	1.81
Modified-TJ180nm pstop	1952.04	2.47



Charge Collection Simulation

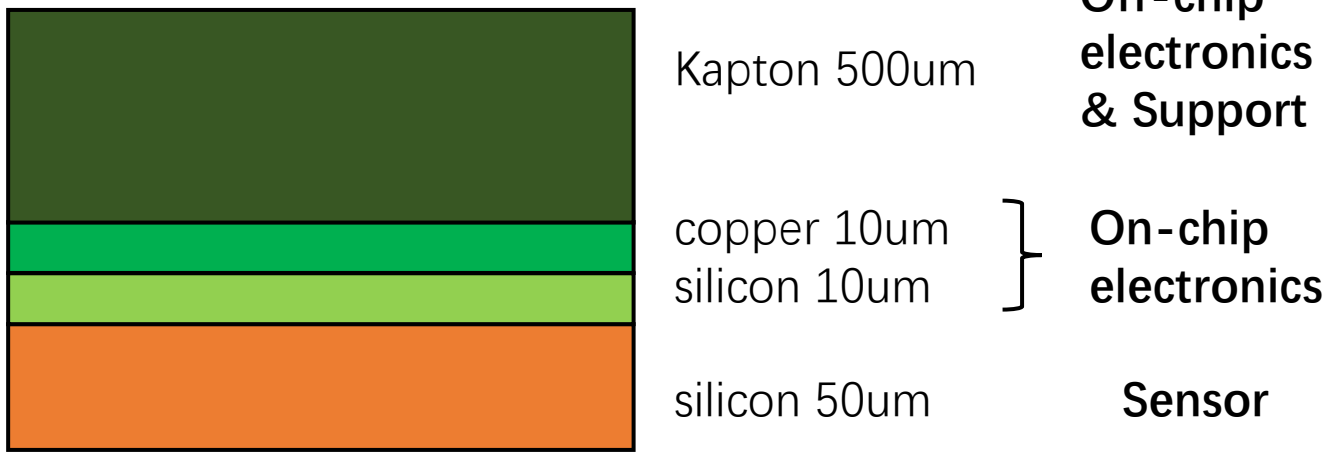
- Ionization density 80$e^-/\mu m$
- Ionization injection from corner of pixel (charge sharing)

	Collected charge (e)	Collection time(ns)
HR epi (TJ180nm)	**531.76**	**139.83**
HR substrate	**508.06**	**163.64**
LR epi	**277.42**	**220.92**
Modified-TJ180nm	443.38	203.91
Modified-TJ180nm pstop	435.06	34.07

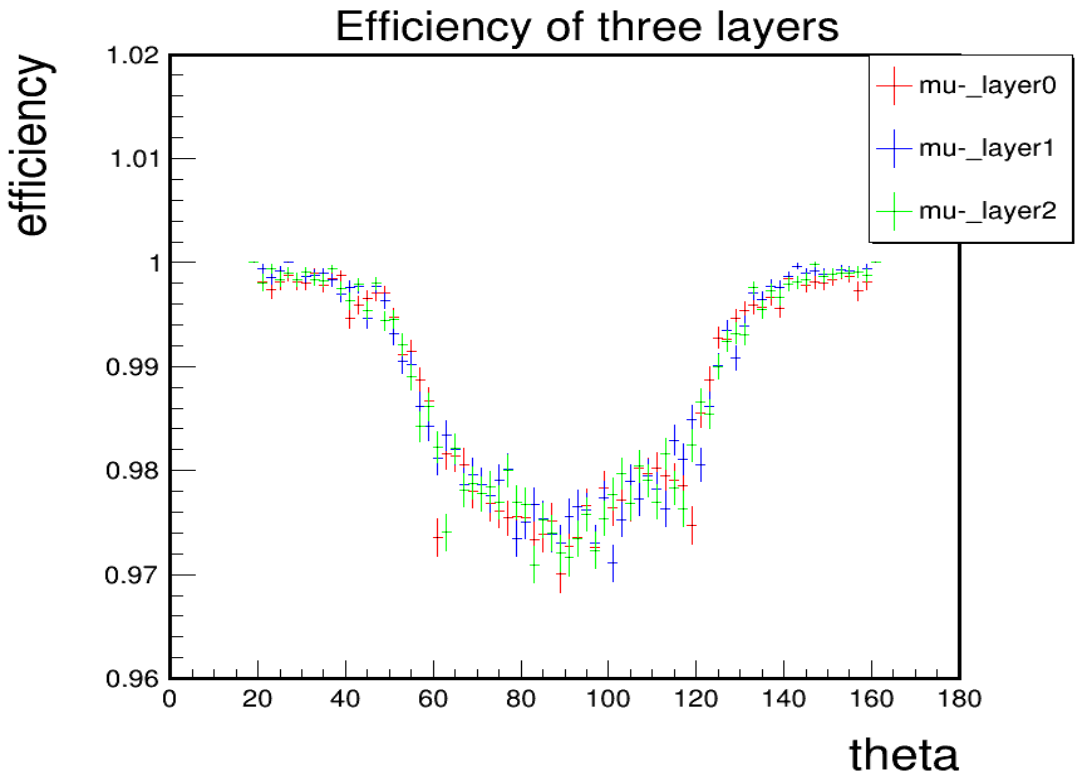


Efficiency Simulation

- Simulation settings:
  - Chip size 2cm × 2cm
  - Pixel geometry: 170μm × 30μm TJ180nm techno
  - 1GeV/c muon, θ range 20°-160°
  - Pixel threshold: 300e$^-$

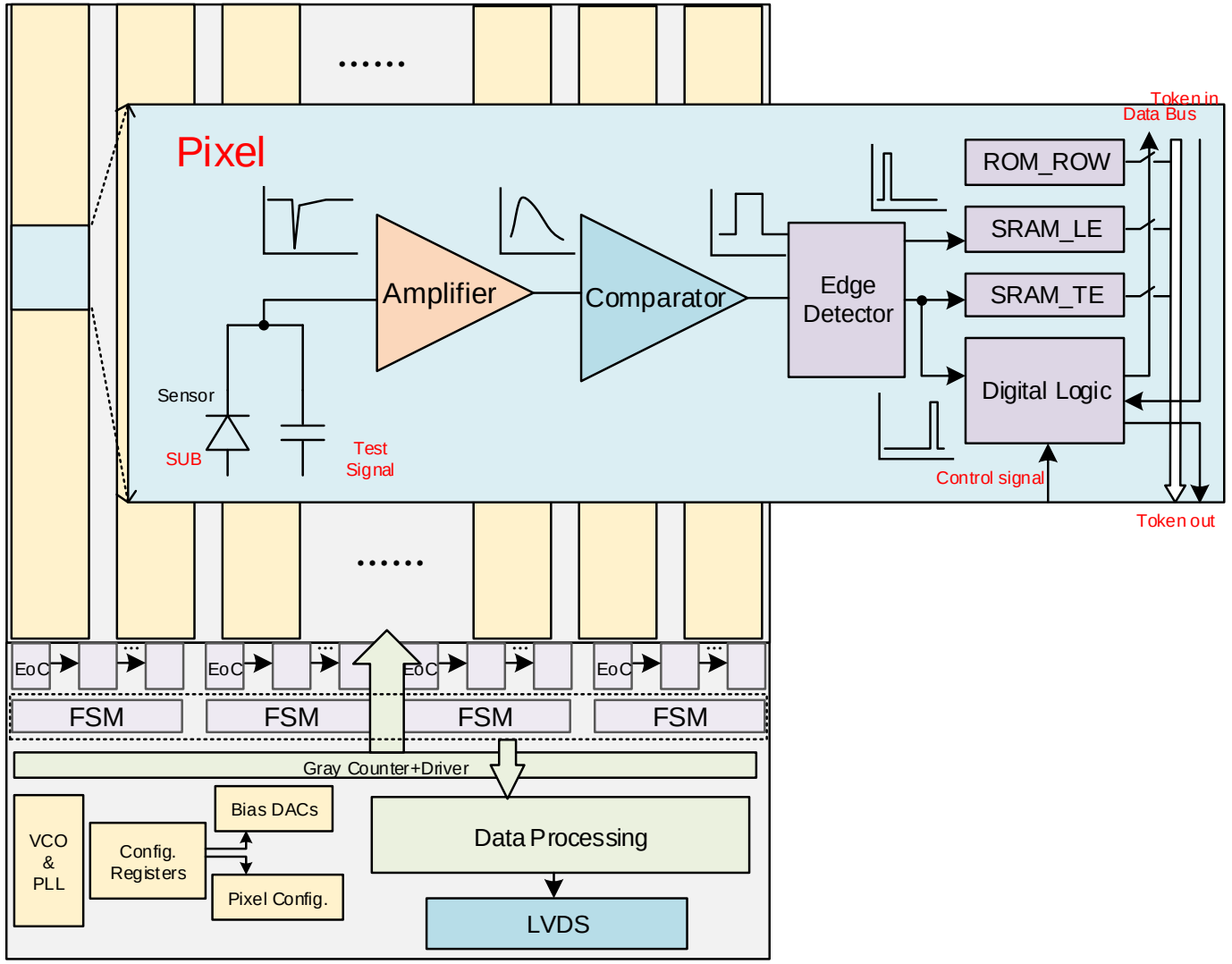


Geometry setting of single layer



Detection efficiency vs. polar angle

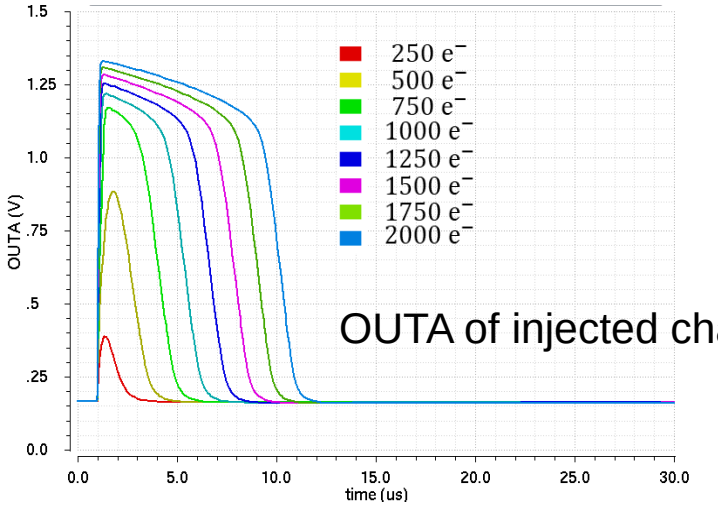
Readout Architecture



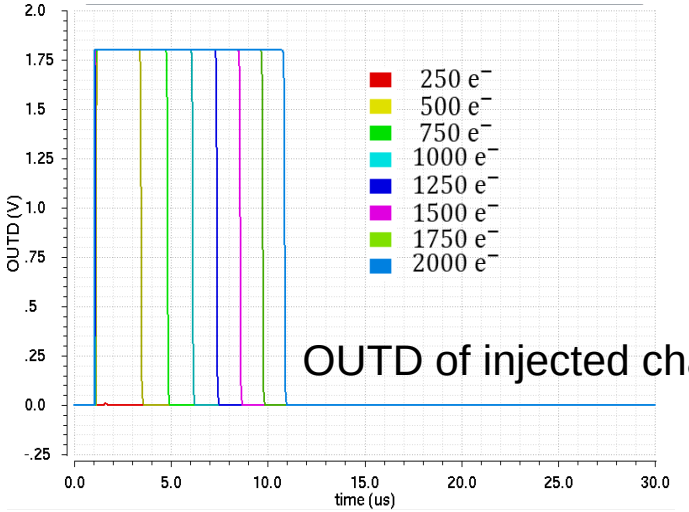
- In-pixel circuits
  - Analog amplifier, comparator
  - Coarse time
- Digital readout
  - Column level priority logic
  - Data processing module
- Peripheral
  - Serializer
  - PLL, LVDS
  - VDAC×2, IDAC
  - Bandgap, EoC current mirror
  - I2C

In-pixel: analog front-end

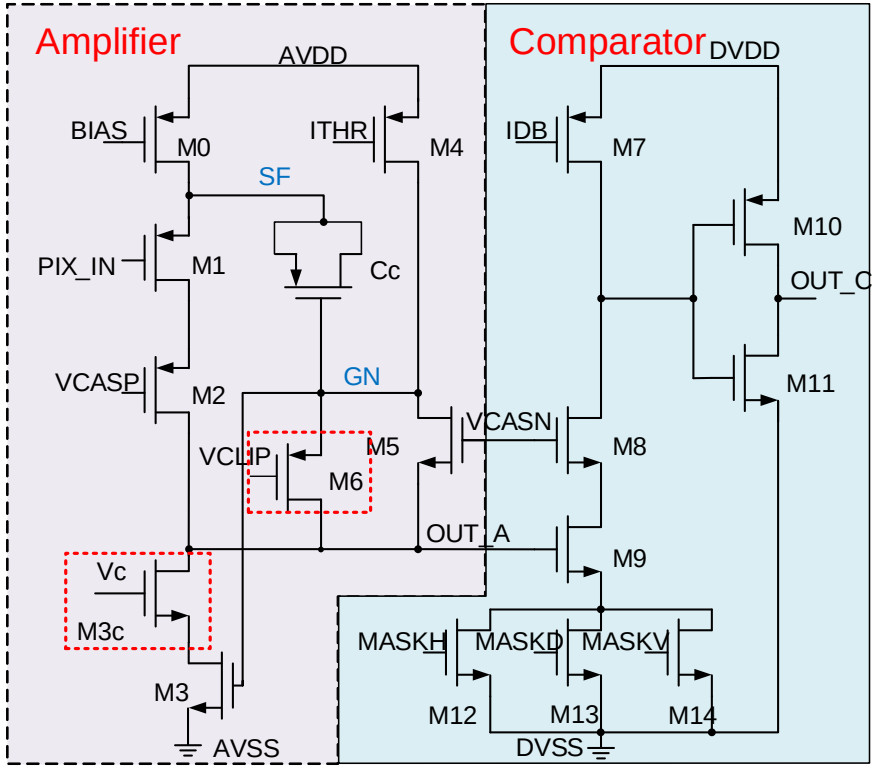
- Amplifier + Comparator
- Simulated performance (180μm×30μm,strip-based sensor)
  - In the timing measurement mode: Threshold=309.0 e^-, ENC=11.4 e-, MISMATCH=5.7 e^-
  - Power consumption: ~800 nA/pix, ~26 mW/cm^2
  - ΔToT/ ΔQ_{inj}=4.8 μs/ke^-



OUTA of injected charge

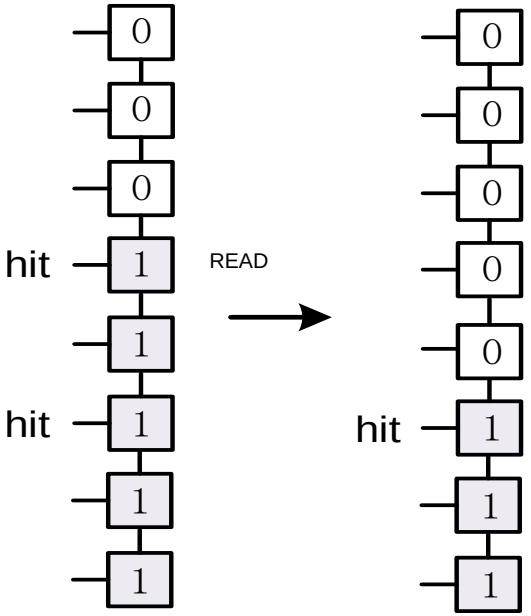


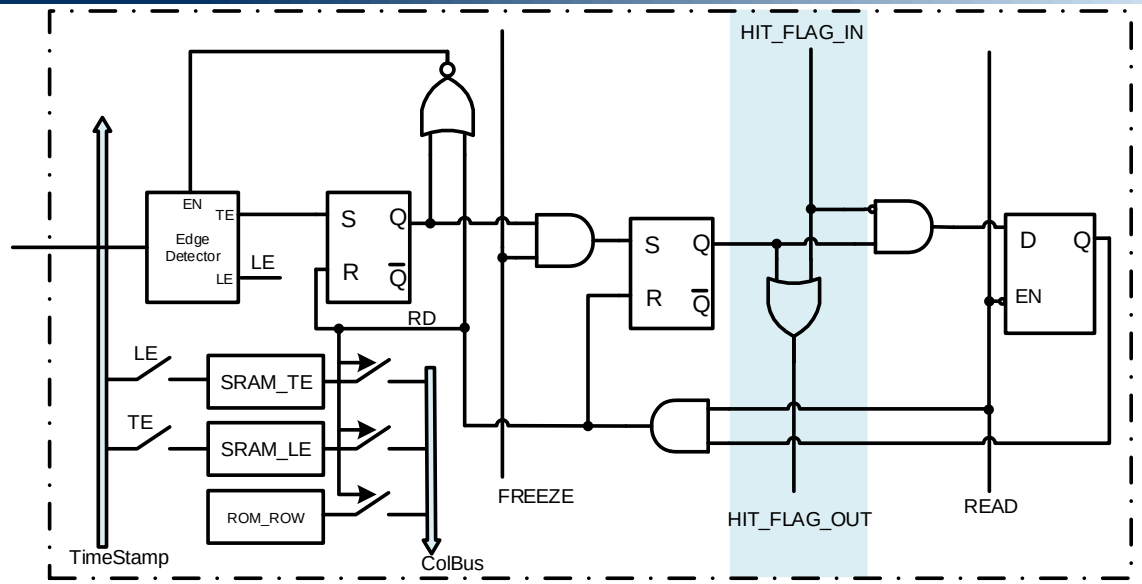
OUTD of injected charged

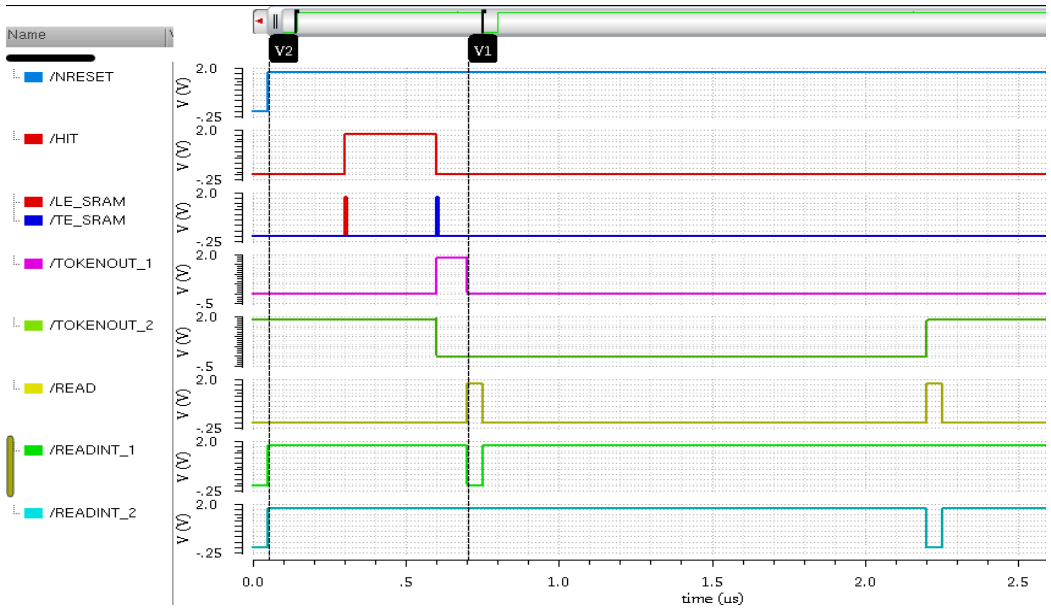


In-pixel: digital

- In-pixel digital circuits
  - Priority readout based on TOKEN (FE-I3)
  - Timestamp frequency: 20 MHz
  - 8-bit leading-/falling-edge
  - Readout clock: 10MHz







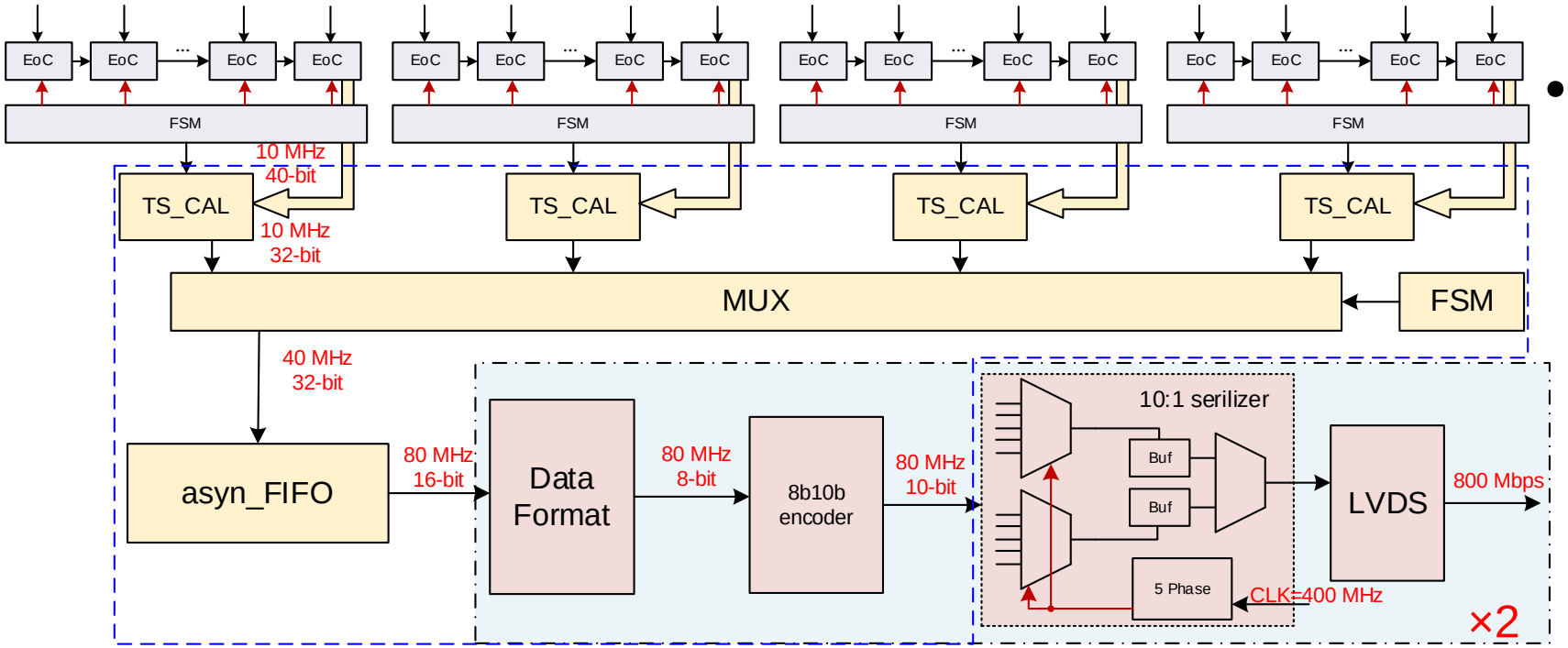
Peripheral Readout

❖ EoC data readout circuit

– Grouped columns with each group readout in parallel to reduce waiting time

– Readout rate >29.6 MHz/Chip，40-bit/Hit(55-bit/Hit after frame encoding)

– Bandwidth: 800Mbps×2



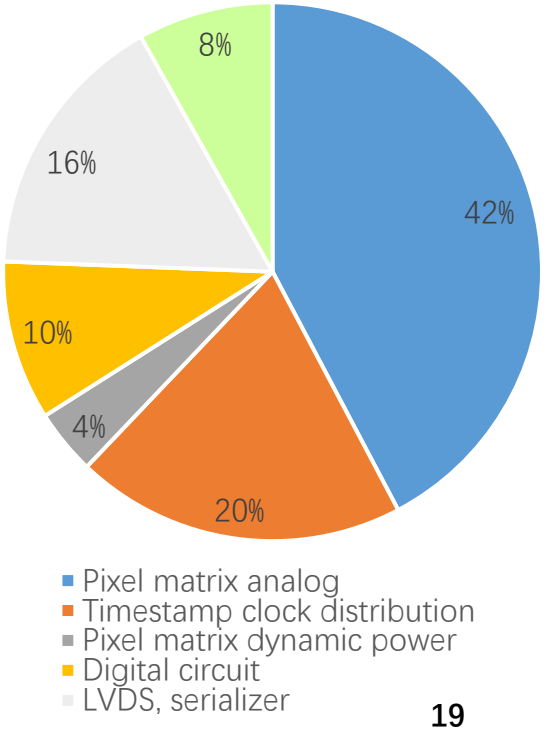
- Data processing unit
  - Timestamp calibration
  - Column group MUX
  - Async FIFO
  - Frame builder
  - 8b10b encoder
  - Searilizer

Power Density Estimation

- Estimated power consumption extended to the full scale chip (~2 cm×2 cm)
  - Strip-based: 55.7 mW/cm^2
  - Pixel-based: 46.2 mW/cm^2
- Expected to reach the target of ~50 mW/cm^2
  - With the potential to use air cooling

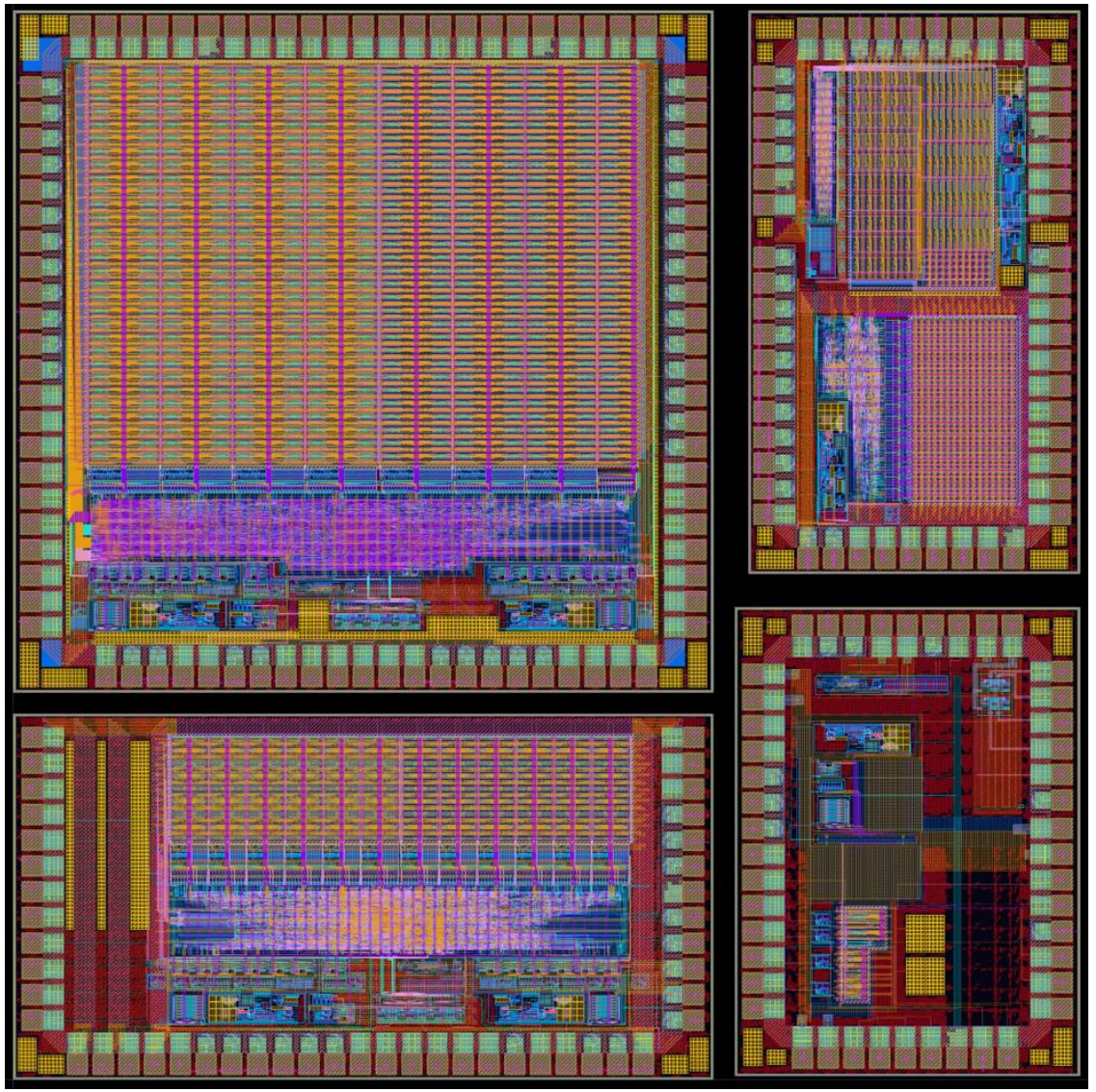
Items	Power consumption	Notes
Analog in pixel matrix	~26 mW/cm^2	Strip-based
	~15 mW/cm^2	Pixel-based
Timestamp clock distribution	12.2 mW/cm^2	
Dynamic power consumption of the pixel matrix	2.4 mW/cm^2	with a data rate of 8.7 MHz/cm^2
Periphery	23.5 mW	32MHz event rate
PLL, serializer, LVDS	39 mW	x 2 data/clock output
Analog configuration	20 mW	
Total	222.6 mW	Strip-based
	184.6 mW	Pixel-based

Power consumption breakdown



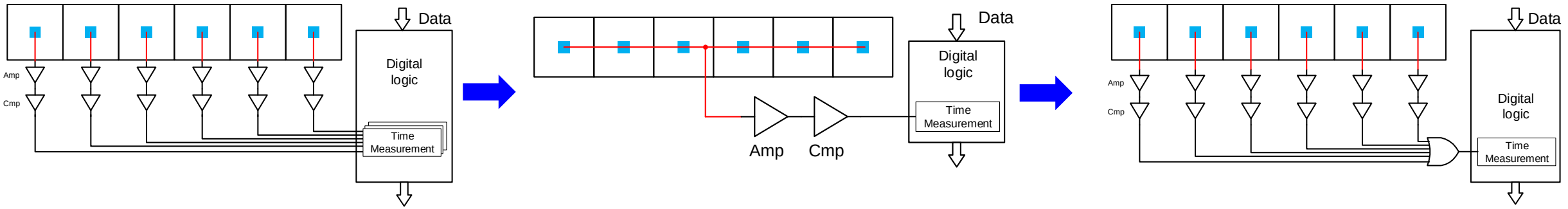
Prototype Chips

- Layout of the 4 prototype chips
  - ALPIDE-like chip (0/1 readout)
  - 30μm×170μm pixel + TOA&TOT
  - 30μm×28μm pixel + TOA&TOT
  - Analog readout
- Has been submitted in March



Timing Improving Consideration

- ❖ Precise timing provides more potential
- ❖ Promising readout architecture：digital “OR” for multiple small pixel



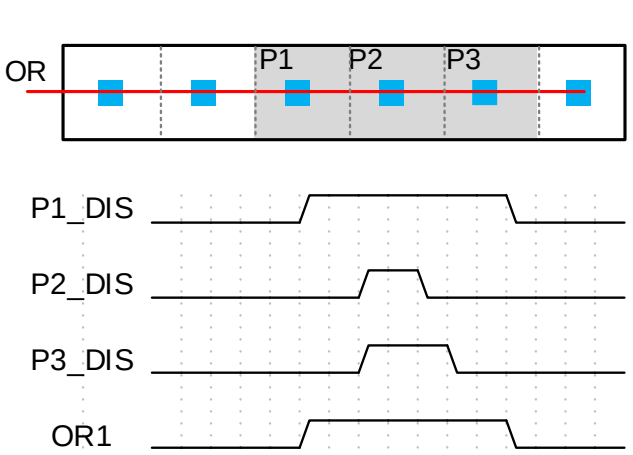
- ✓ Small collection electrode
  → High analog performance
- ✓ Multiple readout channels
  → High digital power

- ✓ Large collection electrode
  → Lower analog performance
- ✓ Fewer readout channels
  → Low digital power

- ✓ Small collection electrode
  → High analog performance
- ✓ Fewer readout channels
  → Low digital power

Super Pixel Design

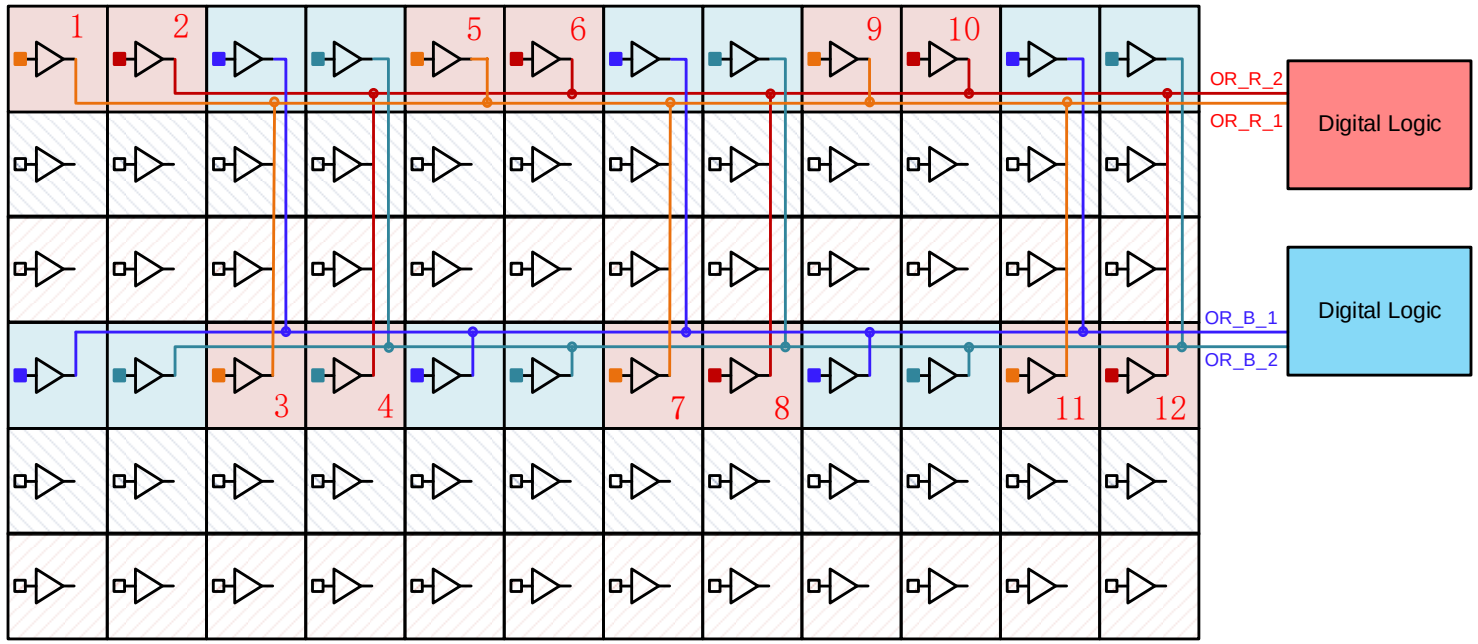
- Combining non-adjacent pixels: avoid ToT loss
- Super pixel with 6×12 pixel array
  - 6 sets of digital readout logic
  - When cluster size < 3X4, no ToT loss occurs



Combining adjacent pixels

→ ToT loss

Additional 3-bit for group address



Providing both high position and high time resolution !

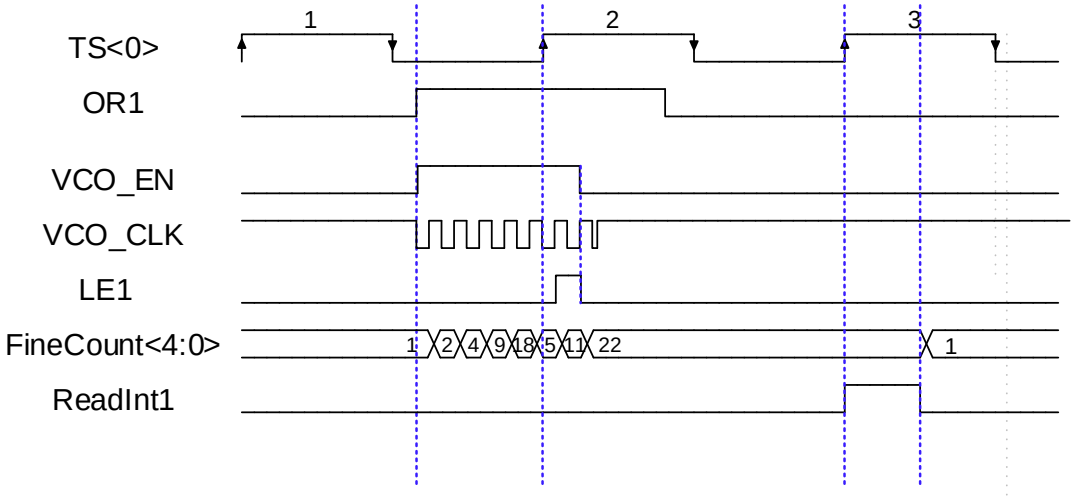
In-pixel: analog front end

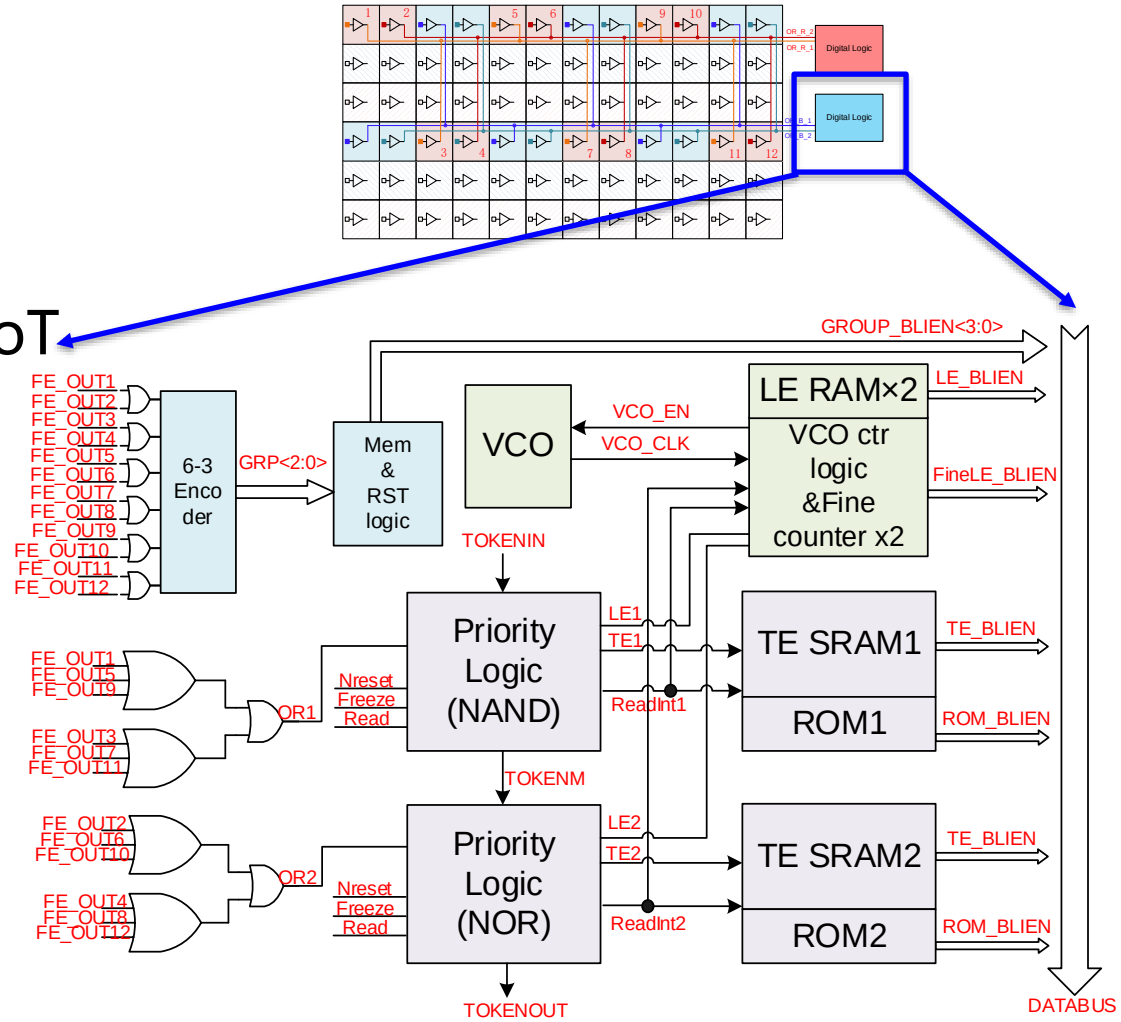
- In-pixel analog circuit
  - Amplifier & comparator
  - Similar to the design in TJ process
- Simulation results (post-sim)
  - Pixel Cp ~ 2.5 fF
  - ΔToT/ΔQin=189 ns per 100e-

	TJ-MAPS	**GSMC-MAPS**
Current	**800 nA/pix**	**120*6 nA/pix**
Supply Voltage	1.8 V	1.2 V
Threshold	309.0 e^-	153.8 e^-
ENC	11.4 e^-	5.1 e^-
Mismatch	5.7 e^-	5.8 e^-
t_r @400 e^-	**200 ns**	**81 ns**

In-pixel: digital readout

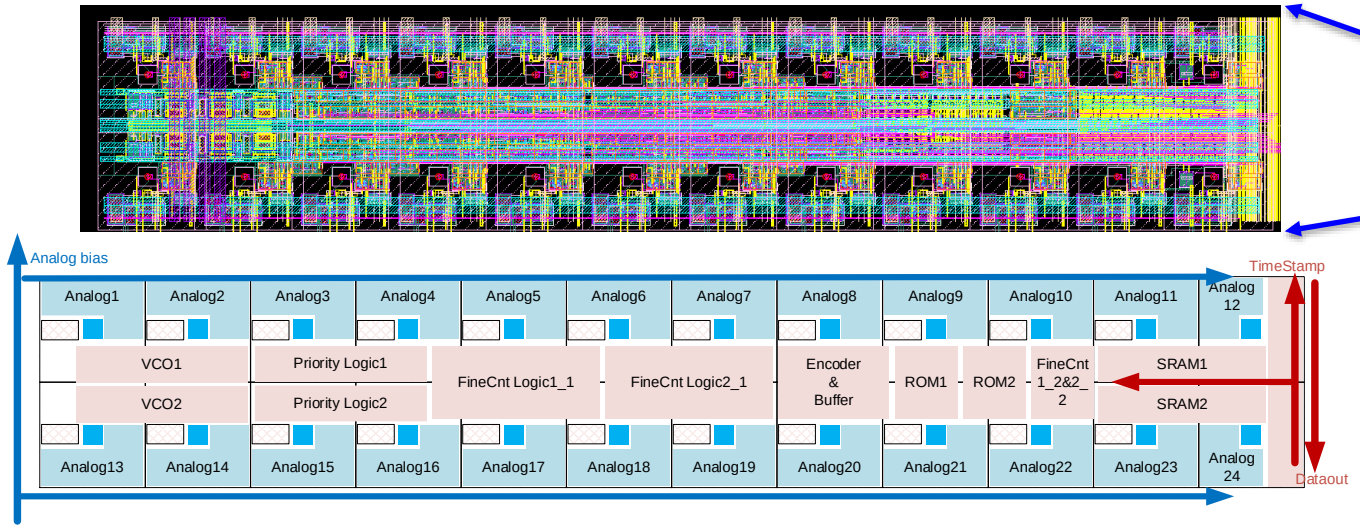
- Multiple pixels share readout logic
- Start-stop VCO in super pixels
  - Record fine ToA @500 MHz
  - Almost no static power consumption
  - 5-bit fine ToA, 8-bit coarse ToA, 8-bit ToT

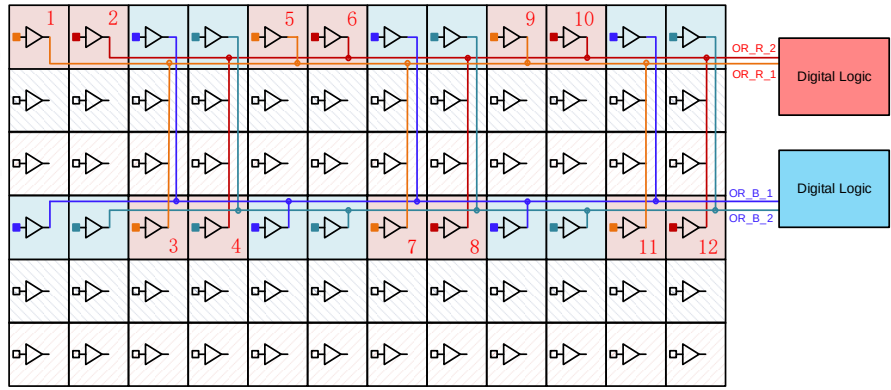




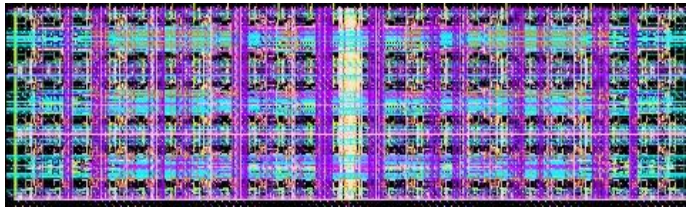
Layout

❖ Layout of super pixel: 2×6 pixel array





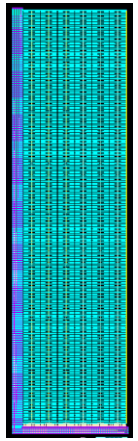
❖ Layout of pixel array



Double_super_pixel

double_column_part

double_column

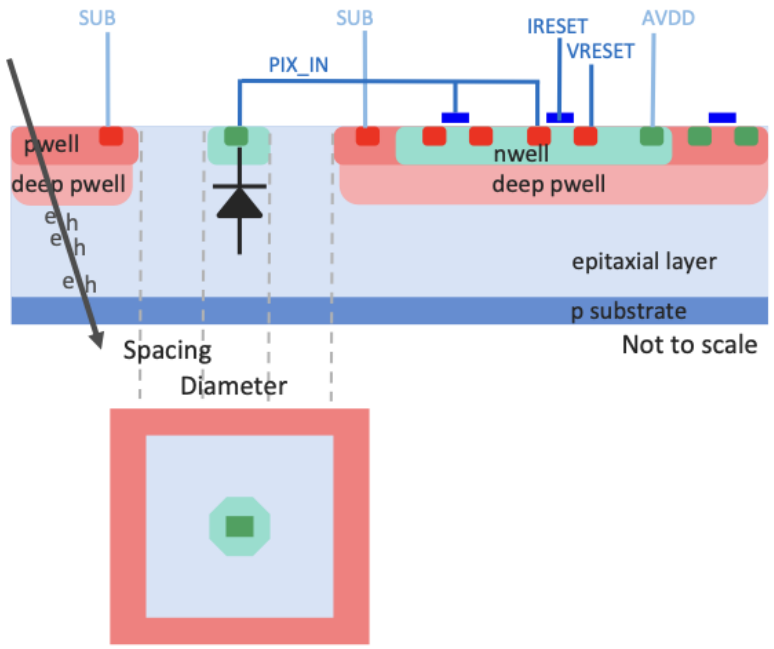


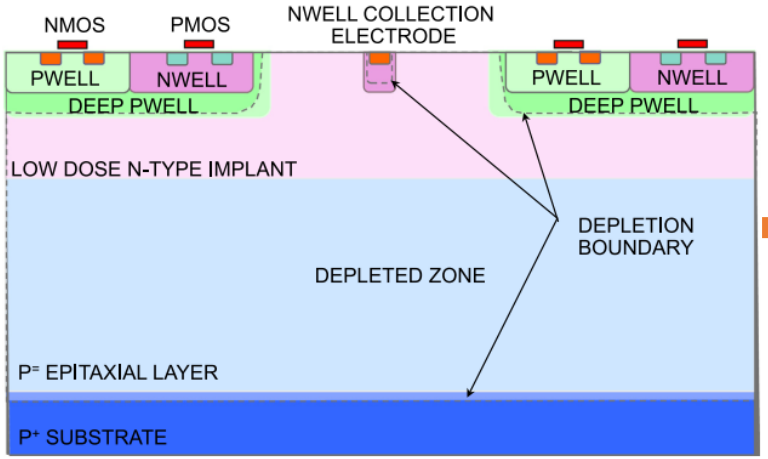
pixel array

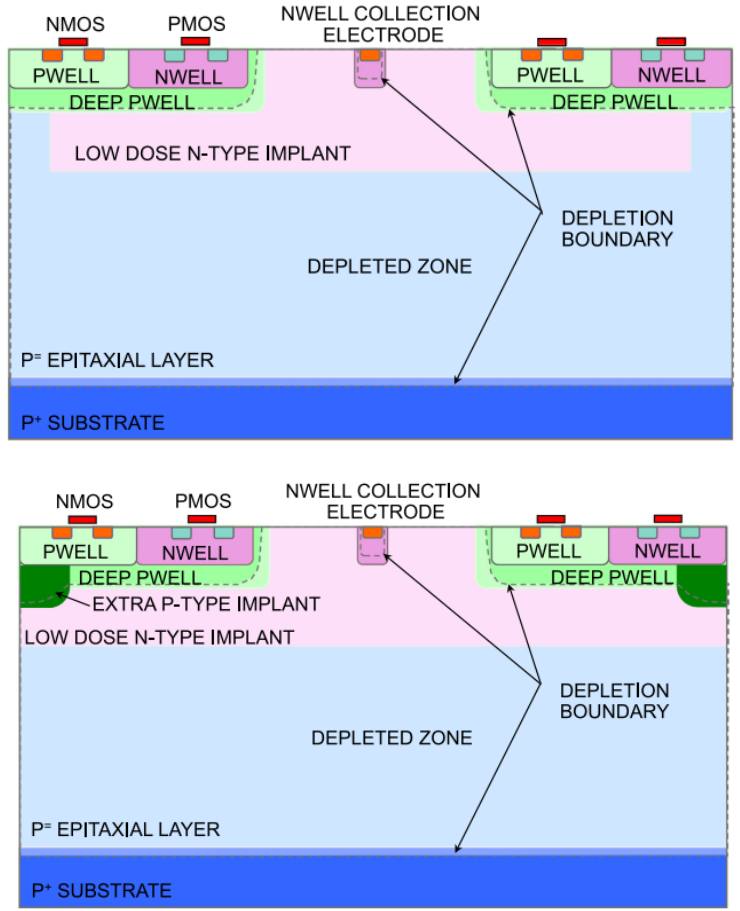
Summary

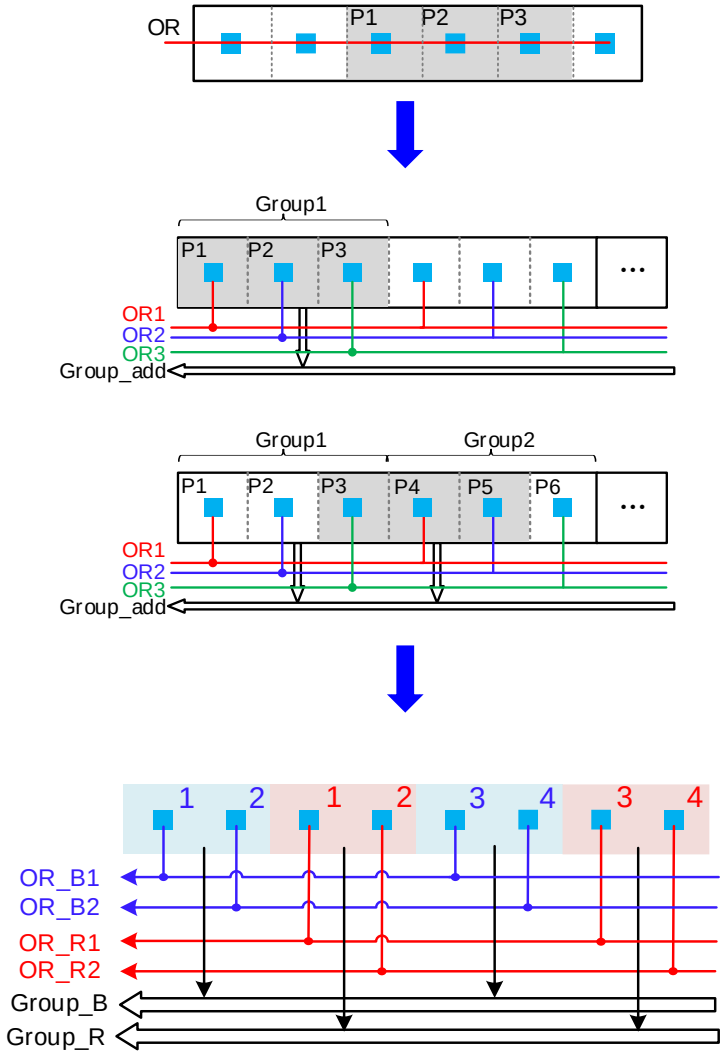
- MAPS-based inner tracker is a promising option for the STCF
  - Spatial resolution: $\leq 100\mu m$
  - Power consumption: $\leq 100mW/cm^2$ ↓
  - Low material budget per layer: $\leq 0.3\%\ X_0$
  - Time resolution: $\leq 50\text{ns} \rightarrow 5\text{ ns}$
- Prototype chips design finished and has been submitted to the foundry in 2024.3
  - Based on the HR epi technology
- Also exploring alternative CIS technologies
  - 90nm CIS with LR epi
  - 130nm CIS with HR substrate

Thank you for your attention !


SUB
SUB
IRESET
AVDD
VRESET
PIX_IN
pwell
deep pwell
nwell
deep pwell
epitaxial layer
p substrate
Not to scale
Spacing
Diameter


NMOS
PMOS
NWELL COLLECTION ELECTRODE
PWELL
NWELL
DEEP PWELL
LOW DOSE N-TYPE IMPLANT
DEPLETION BOUNDARY
DEPLETED ZONE
P⁻ EPITAXIAL LAYER
P⁺ SUBSTRATE


NMOS
PMOS
NWELL COLLECTION ELECTRODE
PWELL
NWELL
DEEP PWELL
LOW DOSE N-TYPE IMPLANT
DEPLETION BOUNDARY
DEPLETED ZONE
P⁻ EPITAXIAL LAYER
P⁺ SUBSTRATE
EXTRA P-TYPE IMPLANT



相邻像素做“OR”

✓ 小信号像素的ToT丢失(Cluster>1时)

错位像素做“OR”

✓ 避免小信号ToT丢失(Cluster>1时)

✓ 读出有效Group地址

✓ 多个Group同时有效时，位置信息丢失

错位像素做“OR”、错位摆放Group

✓ 避免小信号ToT丢失

✓ 避免位置信息丢失

✓ 进一步减小数字功耗