Detector Data Links (Optical Communication) and ASIC R&Ds

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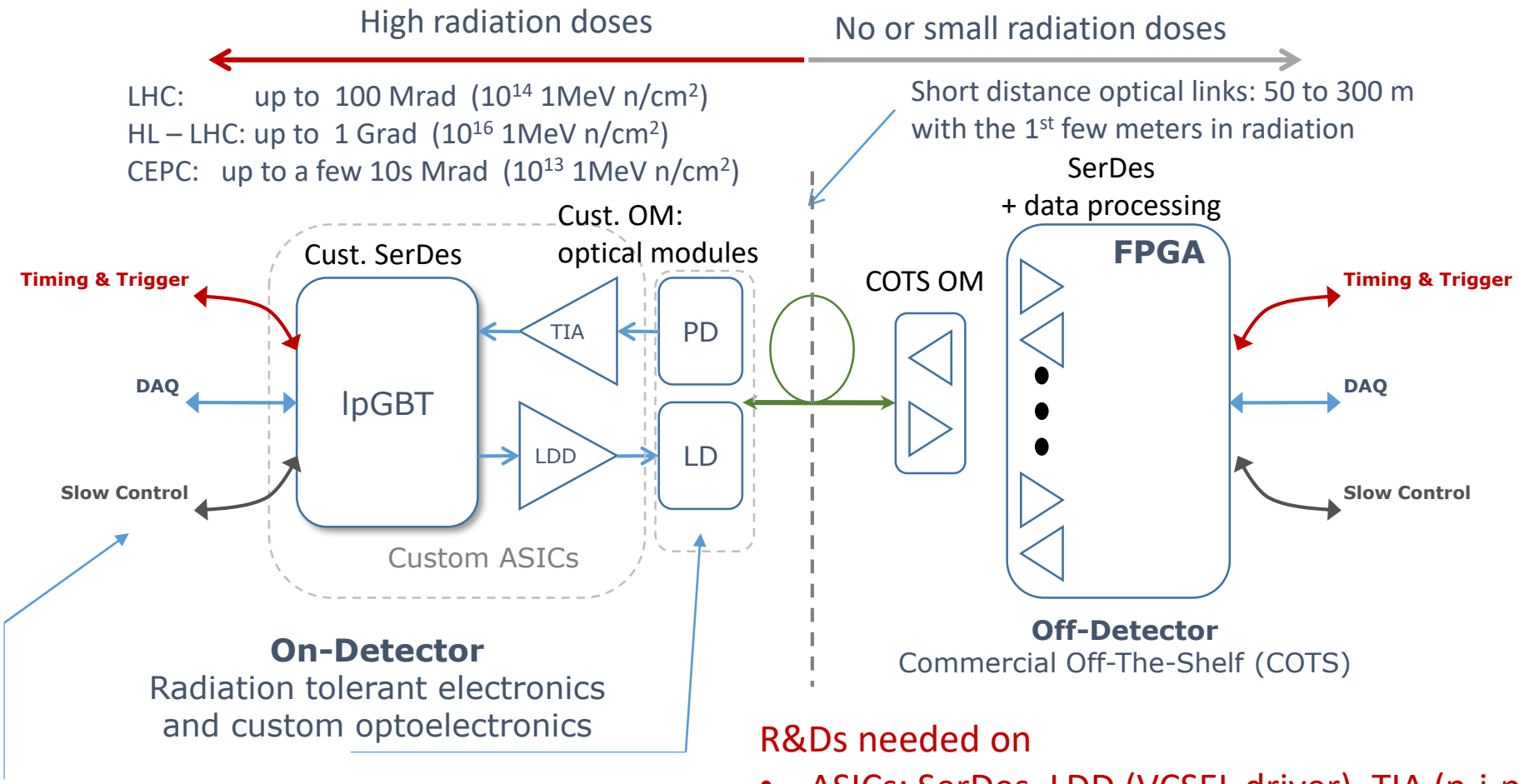
Contents

- A bird's eye view of the detector data link, DDL
- A recount on the ASICs and optical modules developed in the community
- A proposal to go ahead

HEP Detector Data Links(DDLs)



Electrical links to the frontend modules. Lengths: *cm* to few *m*
May need equalization

R&Ds needed on

- ASICs: SerDes, LDD (VCSEL driver), TIA (p-i-n diode amplifier)
- Optical Modules: single-channel or array
- The link system (FE, BE, fiber)

* Some contents borrowed from P. Moreira

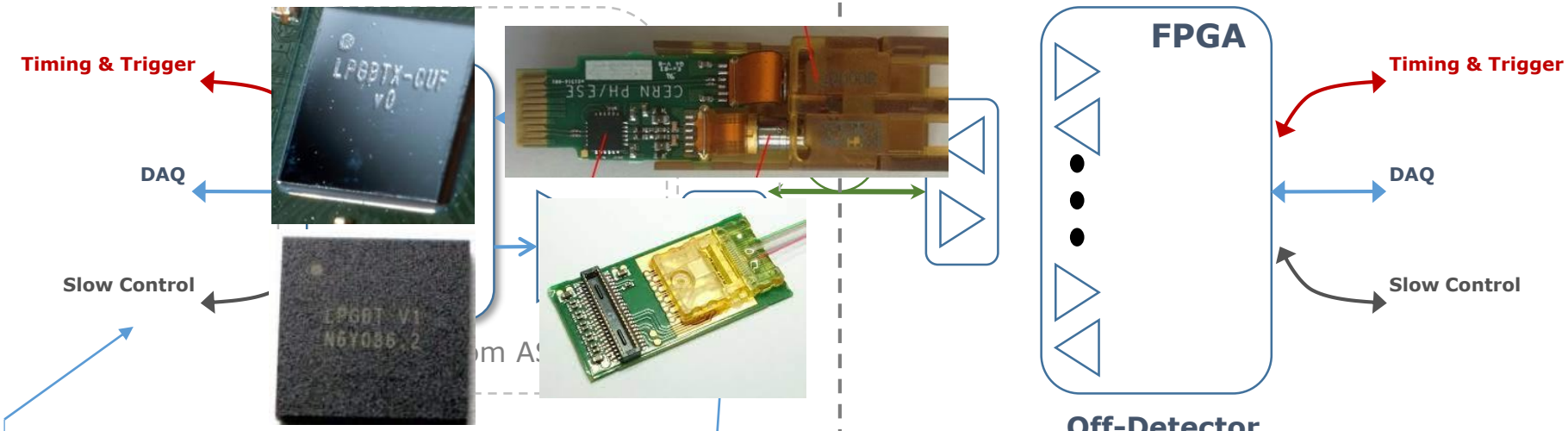
HEP Detector Data Links(DDLs)

High radiation doses

No or small radiation doses

LHC: up to 100 Mrad (10^{14} 1MeV n/cm^2)
HL – LHC: up to 1 Grad (10^{16} 1MeV n/cm^2)
CEPC: up to a few 10s Mrad (10^{13} 1MeV n/cm^2)

Short distance optical links: 50 to 300 m
with the 1st few meters in radiation



On-Detector
Radiation tolerant electronics
and custom optoelectronics

Off-Detector
Commercial Off-The-Shelf (COTS)

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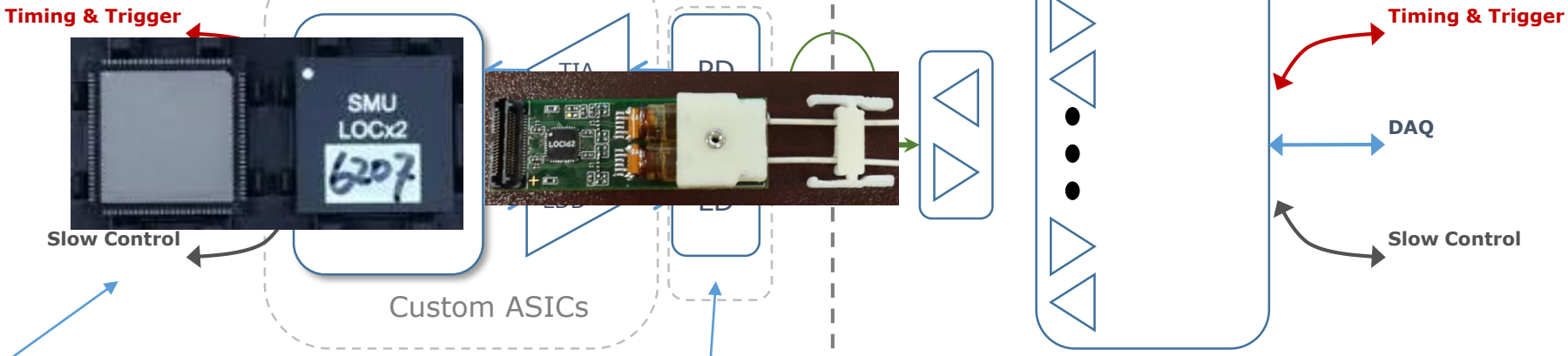

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ASICs for DDLs

ASIC name	Main functions	In experiment
GOL	Serializer, 8B/10B, 1.6 Gbps	LHC
LOCx2	2-chnl serializer, cust.frame, 2x5.12 Gbps	ATLAS LAr
LOCld	Dual-channel VCSEL driver, 2x5.12 Gbps	ATLAS LAr
GBTx	SerDes, cust.frame, 2x4.8 Gbps	LHC phase-1
GBTSCA	TTC and Slow-control	LHC phase-1
GBLD	Single channel VCSEL driver, 4.8 Gbps	VTRx
GBTIA	Single chnl p-i-n TIA + LA, 4.8 Gbps	VTRx, VTRx+
lpGBT	SerDes, TTC, SCA, 2.56 Gbps, dwn,10.24 up	HL-LHC
LDQ	4-chnl VCSEL driver	VTRx+
cpVLAD	4-chnl VCSEL driver, high rad-tol	To be used
QTIA	4-chnl p-i-n receiver, high S/N ratio	To be used

There are a few more, like GBS20 (w/PAM4), GBCR (equalizer), etc.

Optical Modules for DDLs

ASIC name	Main functions	In experiment
[1)]OTx, ORx	TOSA, ROSA based, 1.6 Gbps	ATLAS LAr
[2)]MTx, MTRx	2-chnl Tx, TRx, 2x5.12 Gbps	LAr phase-1
VTRx	2-chnl TRx, TOSA, ROSA based, 2x4.8 Gbps	LHC phase-1
[2)]MTx+	MTx w/ goldfinger and better fiber connt.	CEPC?
VTRx+	4-Tx 4x10.24 Gbps, 1-Rx 2.56 Gbps, MT	LHC phase-2
[2)]QTRx	4-Tx 4x10.24 Gbps, 4-Rx 5.12 Gbps, firefly	CEPC?
[2)]ATx	12-Tx 12x10.24 Gbps, firefly	CEPC?

There are R&D on moving the Serializer to the mezzanine board (GBT20), with PAM4, to reach 20.48 Gbps per fiber. The GBT20 idea will free the system engineers from fast and impedance-matching PCB layout on a large board, saving on development time and material cost.

[1)] From a collaboration between Academia Sinica and SMU

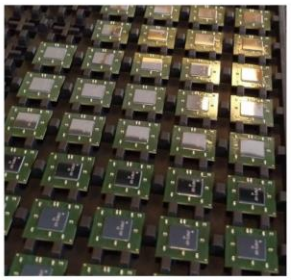
[2)] From a collaboration of Academia Sinica, NJU, and SMU

A few details

CERN的Versatile Link和GBT 项目：

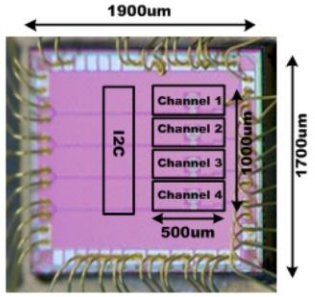
- ✓ 起始于2007年，目标构建应用于HEP抗辐照、高速、双向光纤数据发送系统，主要由GBT系列芯片组和光模块组成。
- ✓ 第一代GBT系列ASIC基于130 nm工艺（2011年）最高串行数据率4.8 Gbps
- ✓ 第二代lpGBT系列芯片基于65 nm CMOS工艺（2019年），最高串行数据率10.24 Gbps.

It took many person-years of development time to arrive at the final objects (packaged chips and modules) for the experiments.



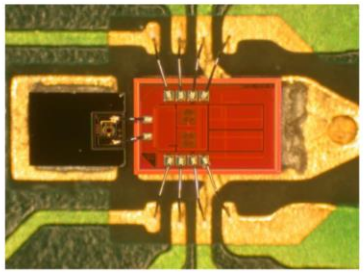
第二代GBTx芯片（lpGBTx）

- 65nm CMOS
- Downlink: 2.56 Gbps
- Uplink: 最高10.24 Gbps
- 0.5mm pitch BGA封装, 289 Pins



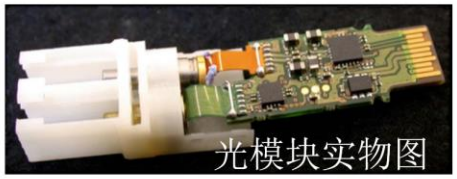
第二代GBLD芯片（LDQ10）

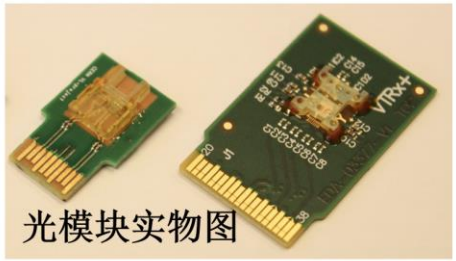
- 65nm CMOS
- 4 x 10 Gbps 四通道阵列式VCSEL激光器驱动



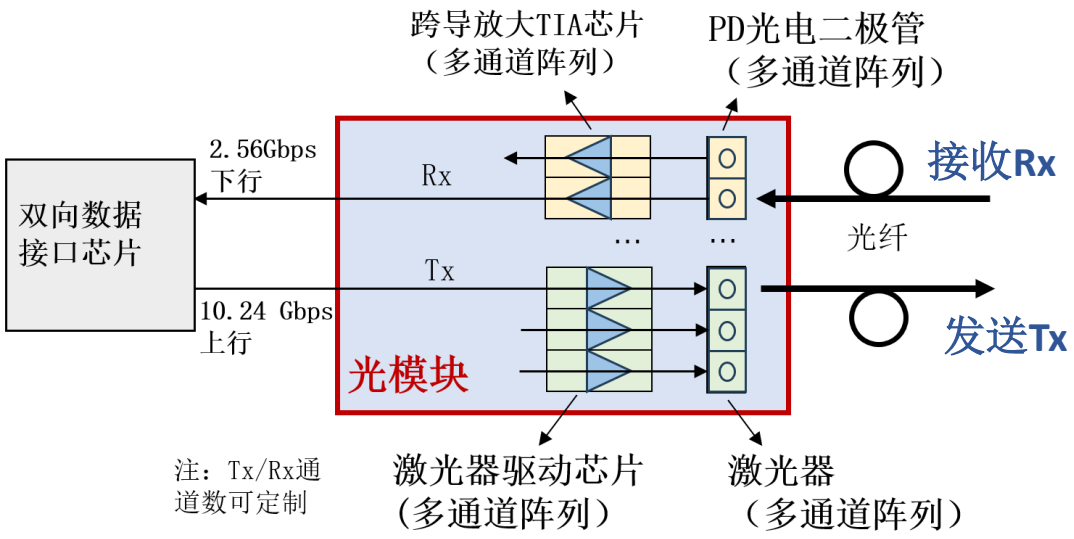
GBTIA芯片

- 130 nm CMOS
- 5 Gbps 单通道接收放大芯片



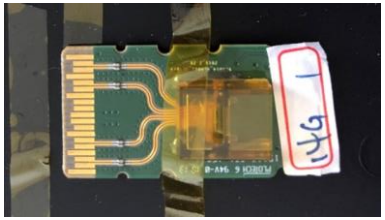


A few details



图中展示的是2Rx + 3Tx情形

商用光模块QSFP (4Tx+4Rx)



自研的阵列式光模块4Tx

- 光模块本质：

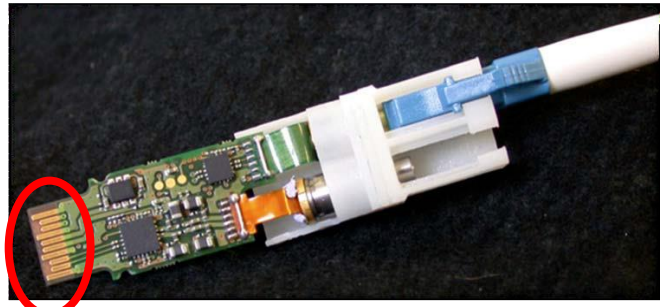
激光器驱动芯片+ 激光器　　（发光，Tx方向）
TIA跨导放大芯片+PD光电二极管　（接收光，Rx方向）

以上四个芯片外加光耦合器件的载体

CERN VTRx+光模块 (4Tx+1Rx)

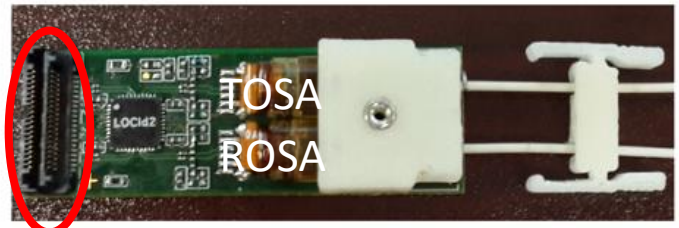
TOSA/ROSA based VTRx and MTRx

- 单通道式光模块：1Tx + 1Rx
  - 商用的SFP光模块即为此类型
- 基于成熟的TOSA 和 ROSA光组件
  - 把激光器、PD封装在里面
    并提供了LC接口
- Tx/Rx方向均使用LC光纤接口（2根多模LC接口的光纤）
- 定制化“相对简单”，主要为设计高速高密度基板、LC光纤的“固定”装置（图中白色）
- 模块高度最小可缩减至 6mm（由TOSA/ROSA组件所限制）
- CERN “非常关注”光模块的高度问题
  以Inner Tracker为例，其读出板“缝隙”很小



CERN的第一代VTRx光模块 (1Tx+1Rx)

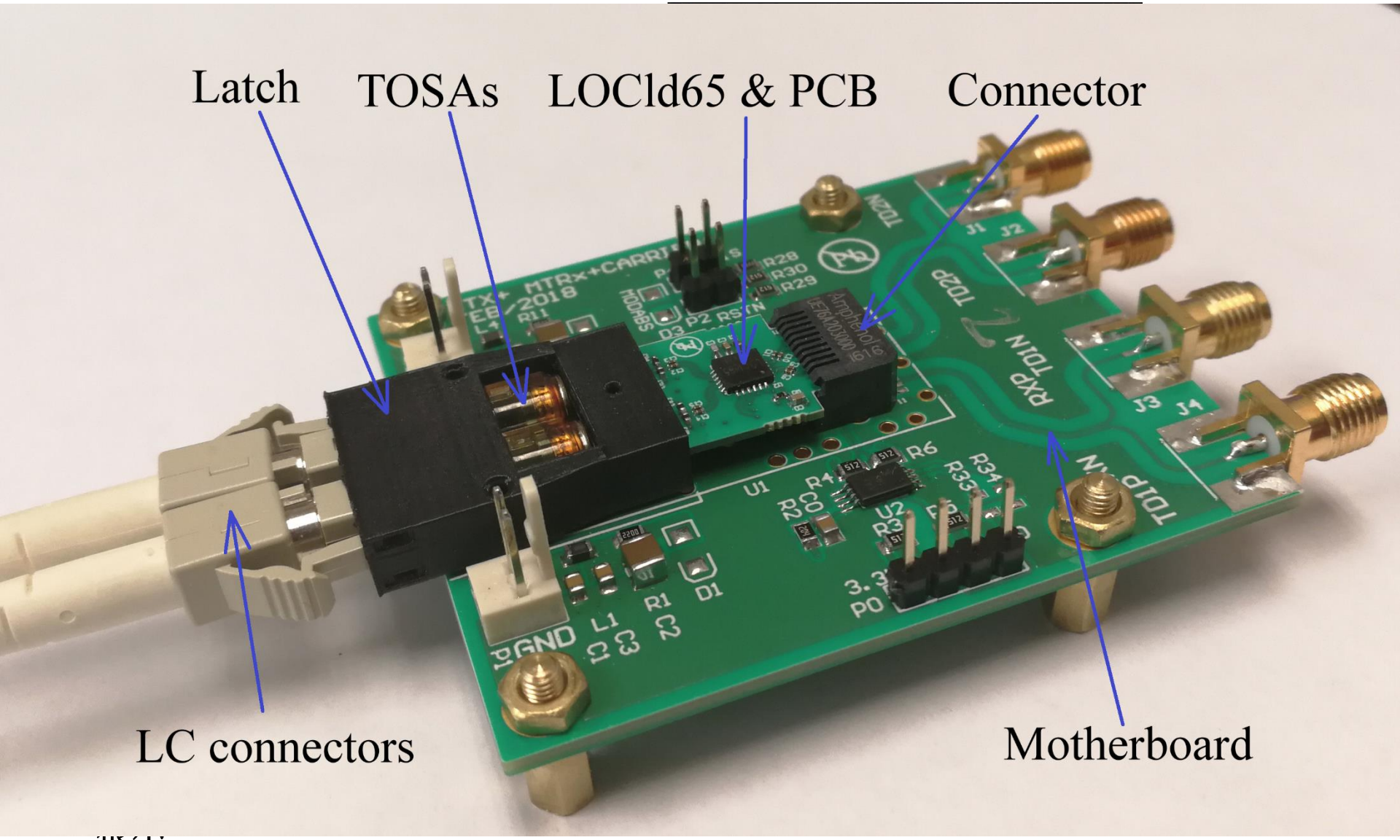
electric connector



另一款 (1Tx+1Rx)定制化光模块MTx

Due to the special QA on optical component, optical modules are usually a pluggable device. It is important to choose a reliable electric connector.

TOSA/ROSA based VTRx and MTRx



Array optics based

- 阵列式光模块：**4Tx + 1Rx, 4Tx + 4Rx, …**

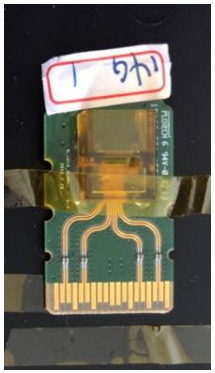
- 使用阵列式的激光器芯片、阵列式**PD**光电二极管
- 使用阵列式的光路耦合器件（图中黄色“盖子”）

- 不再使用**LC**光纤接头，使用**MTP**接头
- 通道数可定制
- **CERN**的第二代**VTRx+** 即升级为了阵列式光模块（采用了**4Tx + 1Rx**）

- 目前阵列式光模块的组装生产已非常成熟

- 模块高度最小可缩减至 **3mm**左右

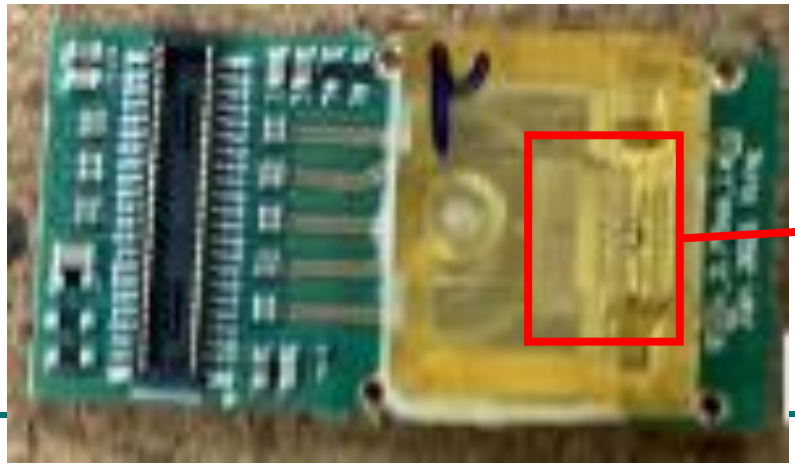
商用光模块QSFP (4Tx+4Rx)

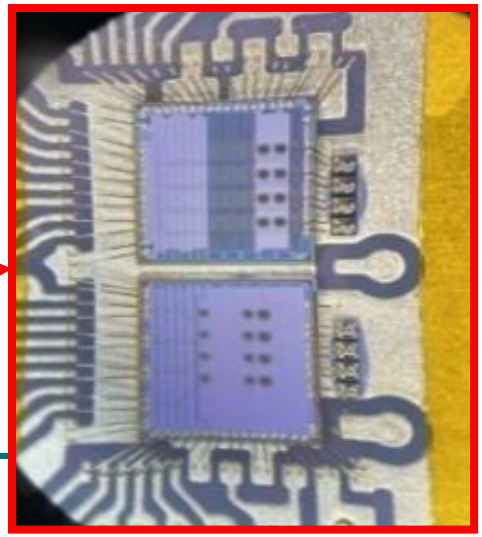


CCNU: 阵列式光模块 4Tx

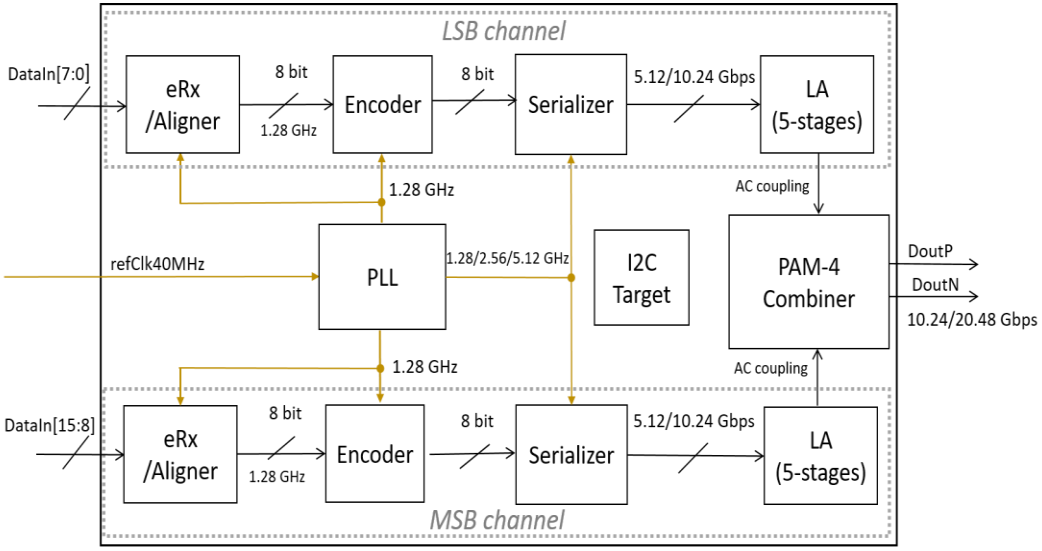
CERN VTRx+光模块 (4Tx+1Rx)

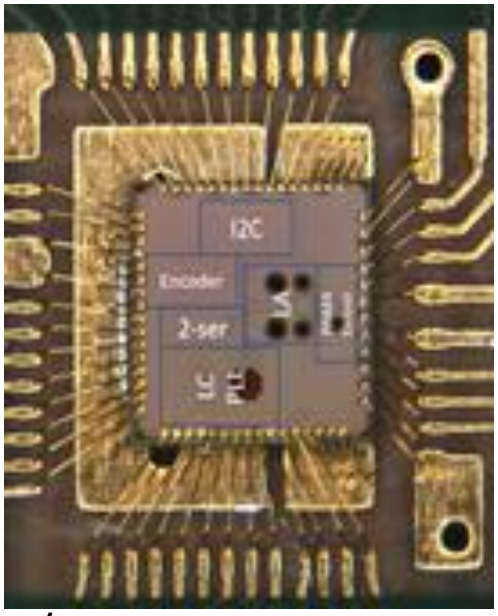
QTRx: 4Tx+4Rx OM
ASICs: SMU/CCNU/IHEP
OM: Academia Sinica



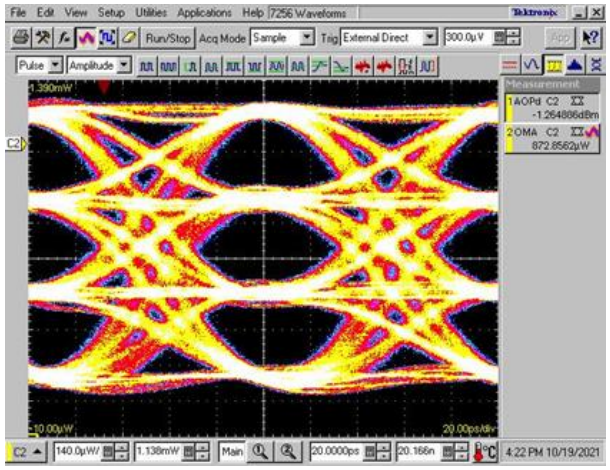


Going to 20 Gbps per channel

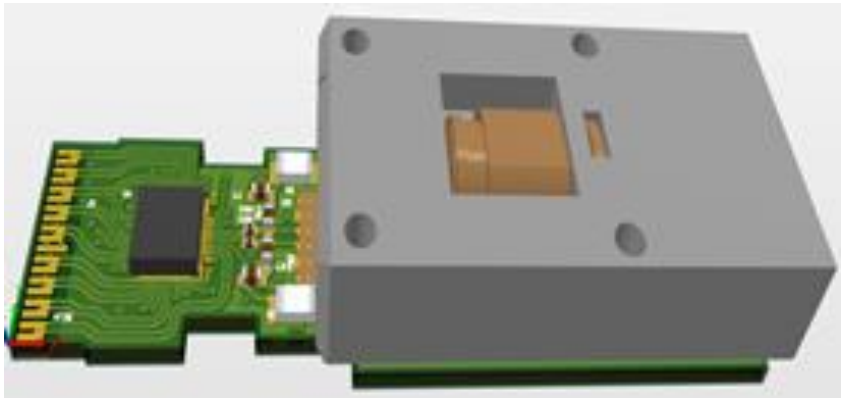




GBS20, the 1st dual-serializer w/ PAM4 in HEP



Tested to 20.48 Gbps



The design of GBT20: a 20 Gbps optical transmitter with GBS20, to have all fast PCB traces in the module PCB. Size: 40 x 13 x 5.75 mm^3.

What we propose

We propose to develop a detector data link system for future experiments. The R&Ds will have the following:

- ASICs, 55 or 28 nm CMOS
  - lpGBT-like (need a name), with a wide clock frequency range, dual-Ser and SerDes.
  - VLAD: VCSEL Array Driver, 1, 4, 8 and 12 chnls
  - DIER: True differential p-i-n receiver, 1 and 4 chnls.
  - Advance chip packaging (ex., flip-chip BGA).
- Optical Modules: array and TOSA/ROSA based.
- Fiber and system issues: follow the foot steps in the CERN Versatile-Link common project.

What we propose

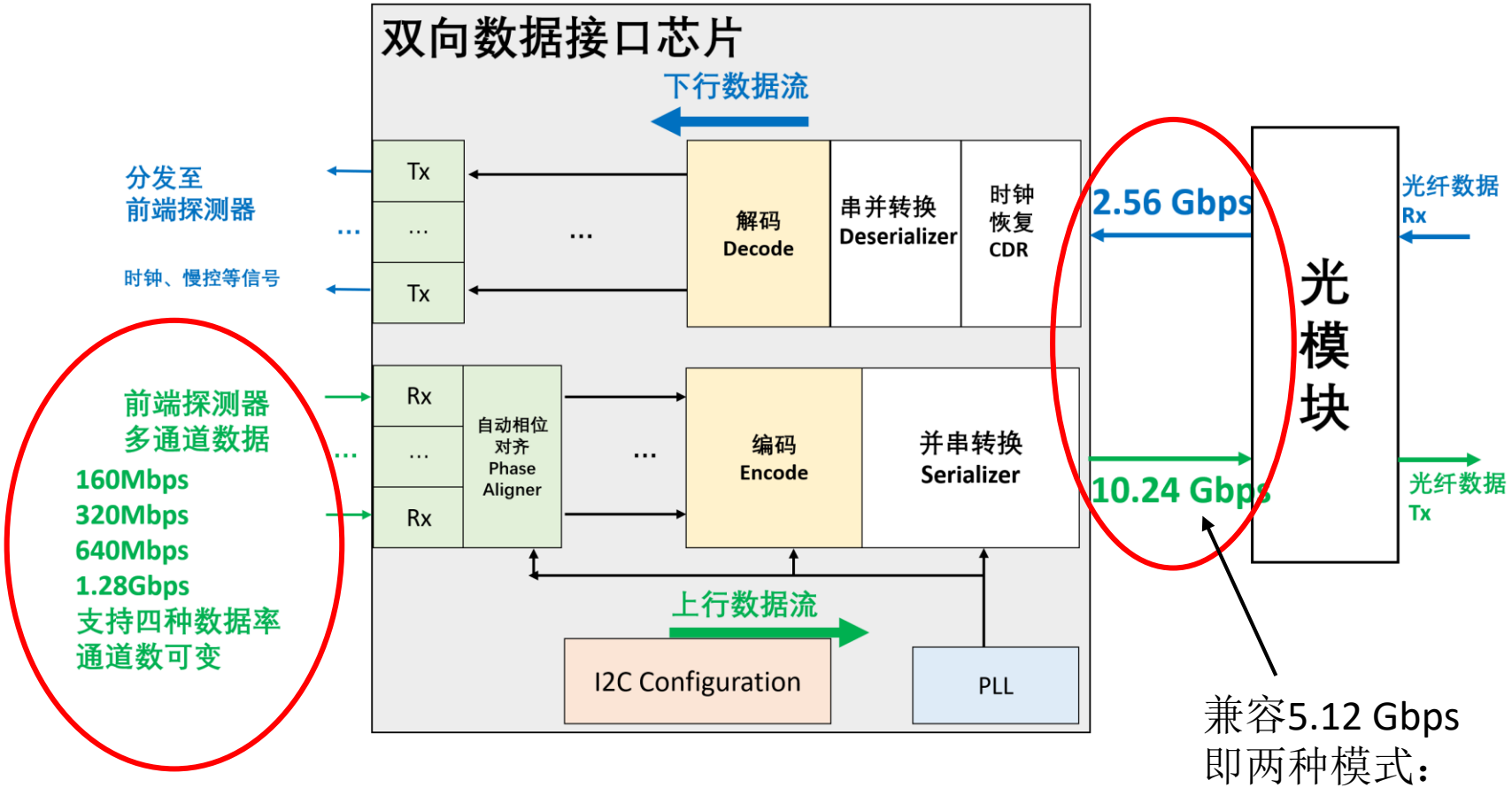
- The DDL common project:
  - The collaboration is forming, all contributions are welcome. There will be a coordinator (for the moment Guo Di) and IB.
  - Work-packages will be specific to developments and deliverables.
  - Developments will be based on what we have already, with a focus on the clock unit and the lpGBT-like SerDes.
  - Suen will lead the development of the optical modules, and the procurement of the fiber.

The take-aways

- It takes many years with contributes from many engineers and physicists to develop the ASICs and modules for the DDL system.
- There is a lot of prior experience, and successful examples, mostly for the LHC experiments. We were (or still are) part of the team.
- But for experiments like CEPC and STCF, the R&Ds on the DDL need to start now (I wanted to say that they should have started years back, but …).

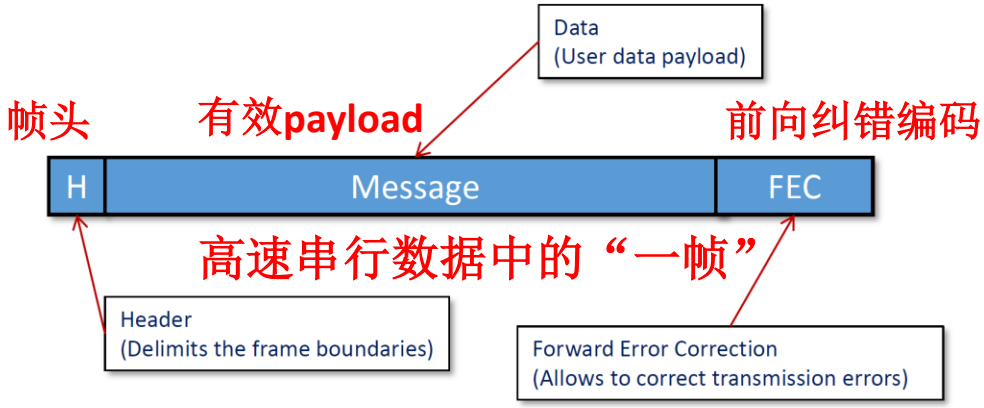
Thank you

What we propose



上行数据编码 帧格式

- The LpGBT supports the following uplink data rates:
  - 5.12 / 10.24 Gbps
- Data is transmitted as a frame composed of:
  - Header
  - The data field
  - A forward error correction field: FEC5 / FEC12
- The data field is scrambled to allow for CDR operation at no [additional] bandwidth penalty
- Efficiency = # data bits/# frame bits



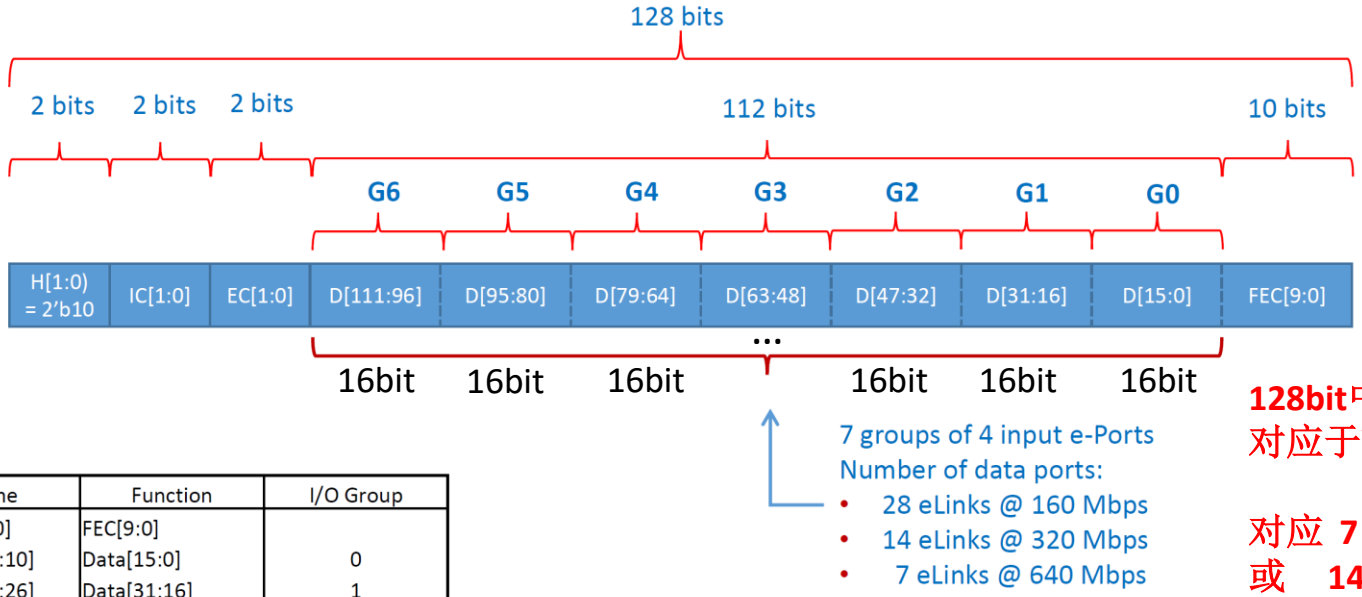
	uplink			
	5.12 Gbps		10.24 Gbps	
	FEC5	FEC12	FEC5	FEC12
Frame [bits]	128		256	
Header [bits]	2		2	
Data [bits]	116	102	232	204
FEC [bits]	10	24	20	48
Correction [bits]	5	12	10	24
Efficiency	91%	80%	91%	80%

四种帧格式的资源消耗和效率情况

内容引用自lpGBTx相关文档

- 在上行方向支持两种数据率 **5.12 Gbps/ 10.24 Gbps**
- 编码方面支持**2**种不同强度的前向纠错**FEC**编码（抵抗**SEU**翻转导致错误）
- 总计支持“**4**”种**frame protocol**

上行数据编码 帧格式



一帧为 128bits
帧速率为 40M
串行bit率 5.12Gbps

128bit中 112bit (7 x 16 bit)
对应于输入的前端多通道数据

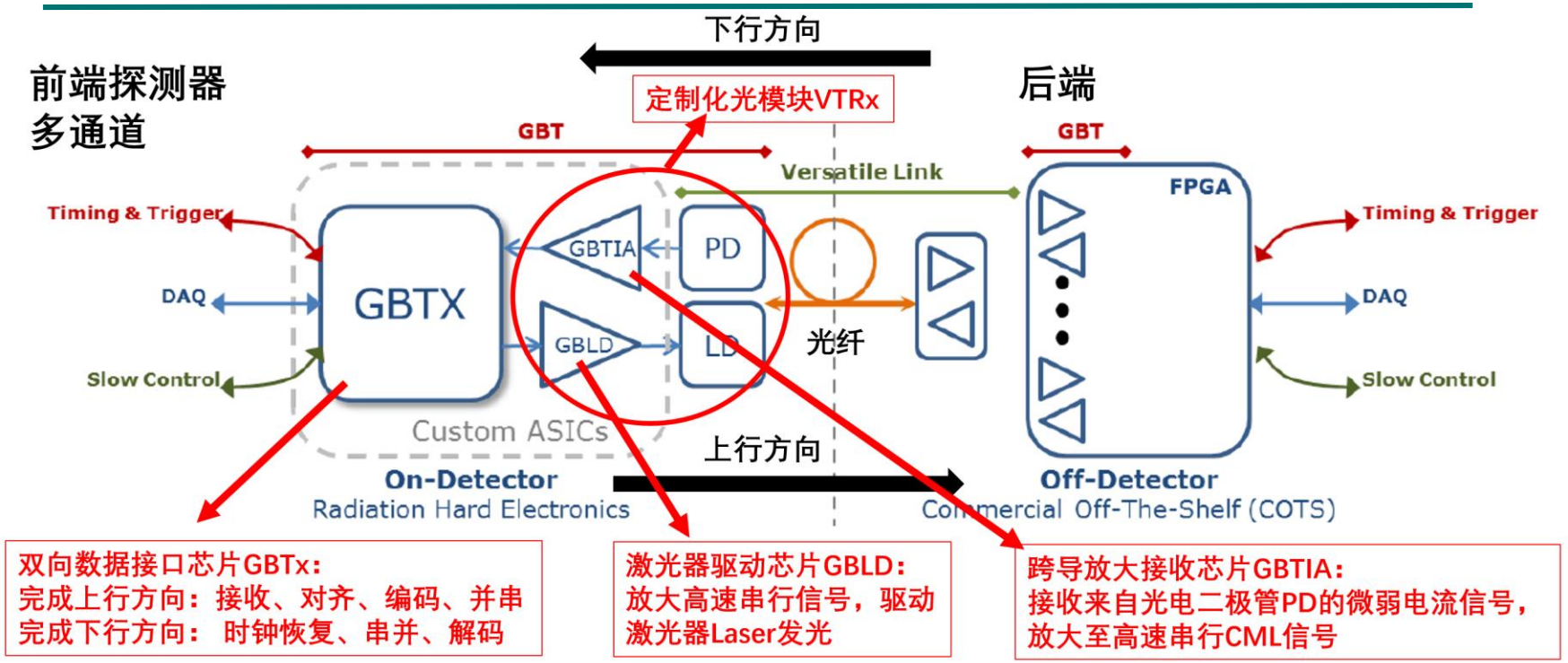
对应 7 * 640Mbps 的前端数据
或 14 * 320Mbps 的前端数据
或 28 * 160Mbps的前端数据

Frame	Function	I/O Group
FRMUP[9:0]	FEC[9:0]	
FRMUP[25:10]	Data[15:0]	0
FRMUP[41:26]	Data[31:16]	1
FRMUP[57:42]	Data[47:32]	2
FRMUP[73:58]	Data[63:48]	3
FRMUP[89:74]	Data[79:64]	4
FRMUP[105:90]	Data[95:80]	5
FRMUP[121:106]	Data[111:96]	6
FRMUP[123:122]	EC[1:0]	EC
FRMUP[125:124]	IC[1:0]	
FRMUP[127:126]	H[1:0] = 2'b10	HFH[1:0] = 2'b10

内容引用自lpGBTx相关文档

- 这里以5.12 Gbps数据率输出，选择FEC5 情形下的“帧格式”定义

HEP Detector Data Links

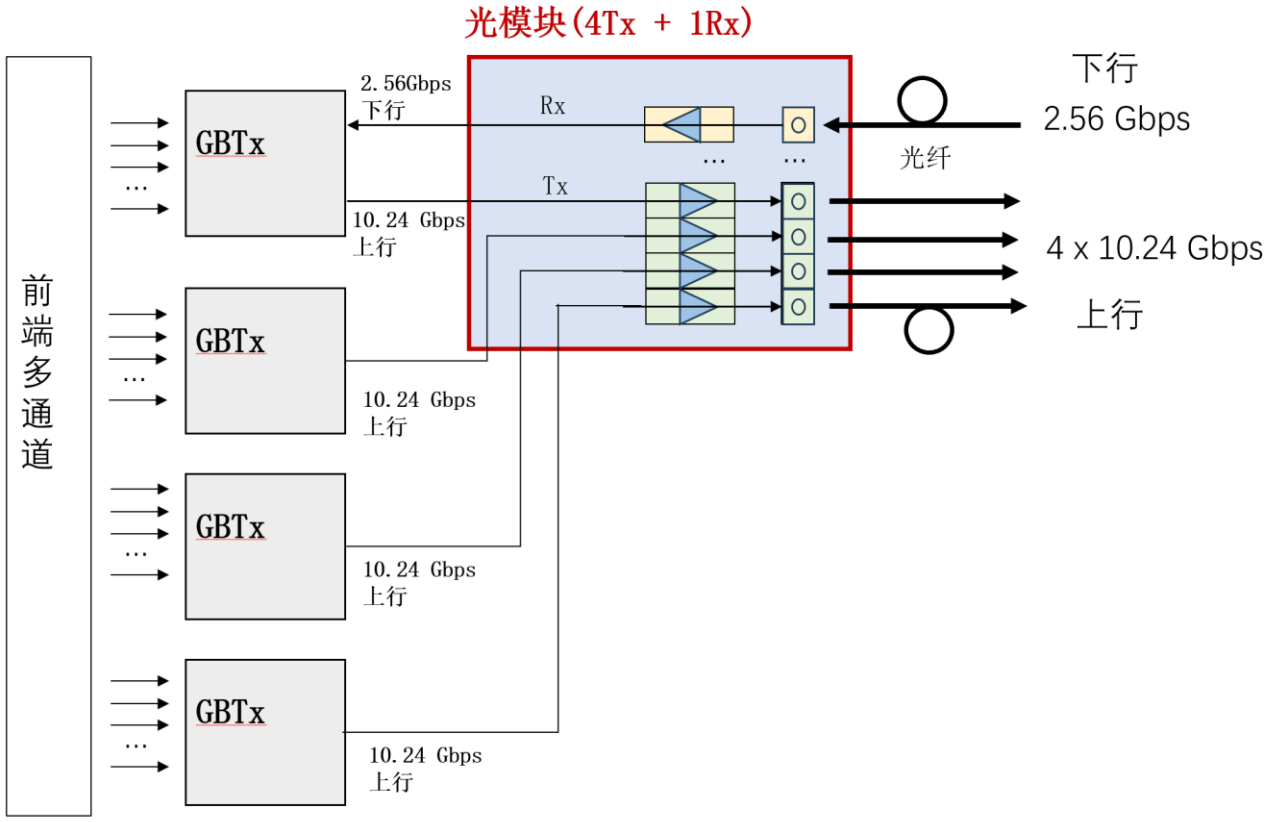


CERN研发的GBT系列芯片等构建起双向光纤数据传输系统：

- ✓ GBTx：双向数据接口芯片
- ✓ GBLD：激光器驱动芯片 （**LD: Laser Driver**）
- ✓ GBTIA：跨导放大芯片 （**TIA: Transimpedance Amplifier**）
- ✓ **VTRx光模块**
- ✓ 抗辐照 **400Mrad** 总剂量 （**CERN在Phase II升级中对于Link系统的要求**）

阵列式的光模块

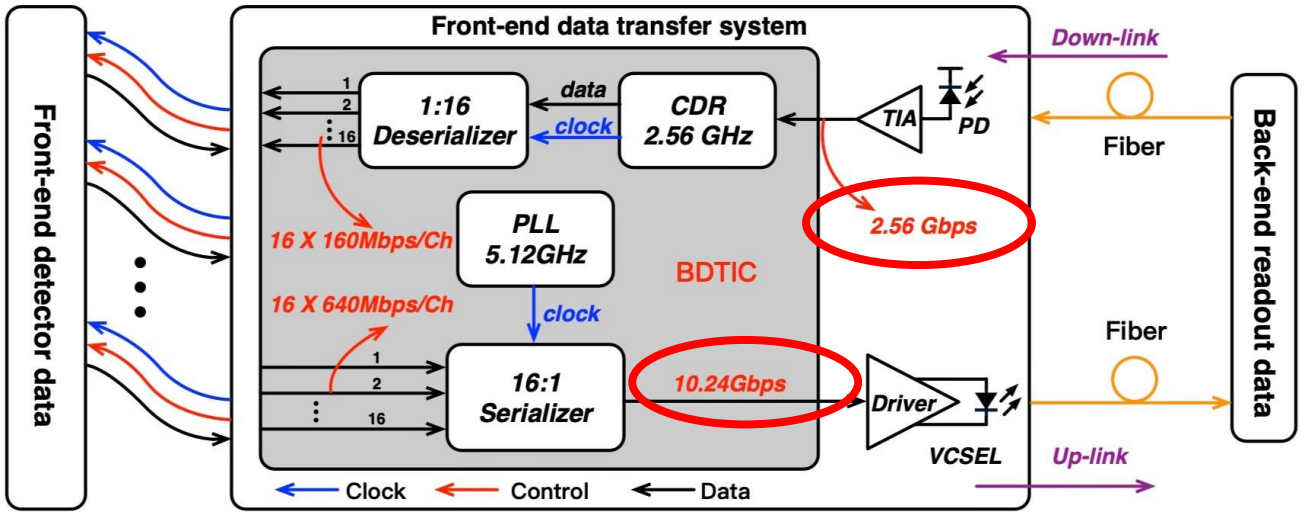
- 在数据通量巨大的单板上，使用阵列式光模块可减少光模块使用数量，减少光纤数量



前端双向光通信系统

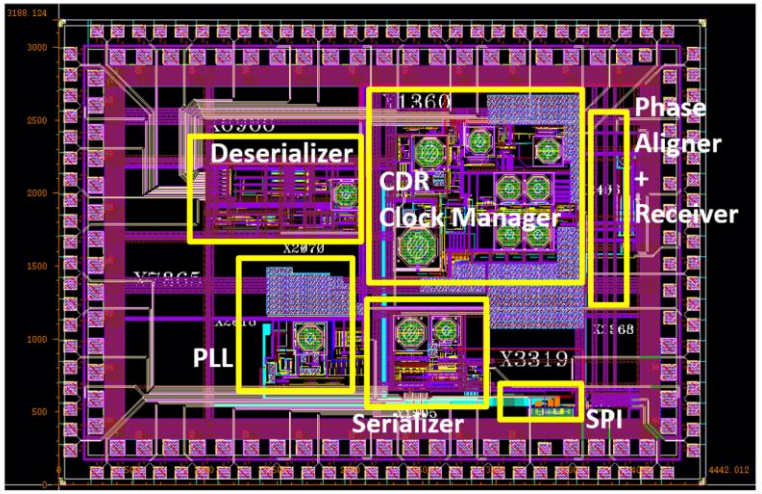
双向数据接口芯片、
定制化光模块、
驱动芯片
跨导TIA放大芯片
方面的已有部分研发基础

双向数据接口-BDTIC芯片



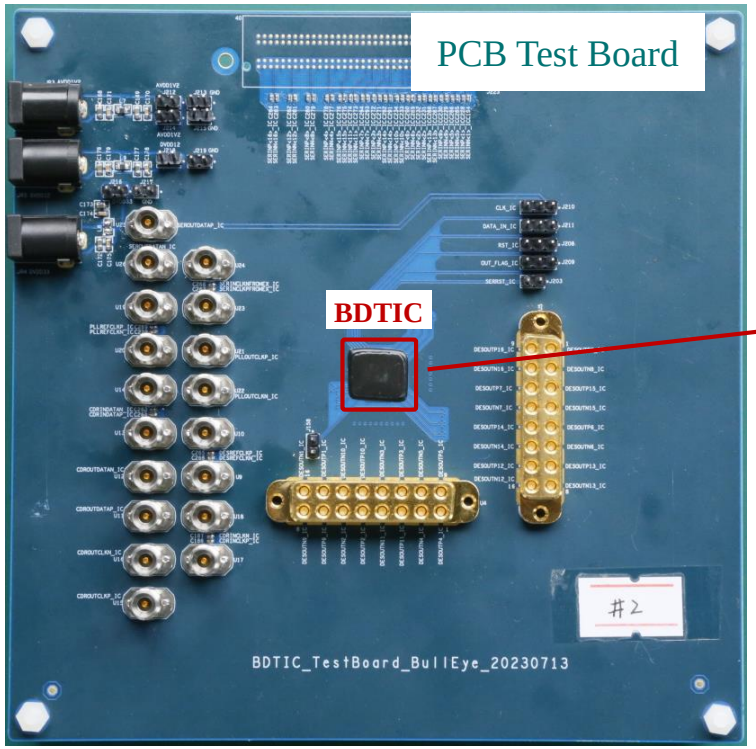
BDTIC芯片结构框图

- ✓ The Bidirectinal Data Transmission Interface Chip (BDTIC_v1) 双向数据传输接口芯片_v1
- ✓ 中芯国际SMIC 55nm, 166 pins
- ✓ 包括：5.12 G PLL, 2.56 GHz CDR, 10.24 Gbps Serializer, 2.56 Gbps Deserializer 、独立小型测试模块
- ✓ 不包括数字部分（编解码等）
- ✓ 2022年底流片，2023年6月测试



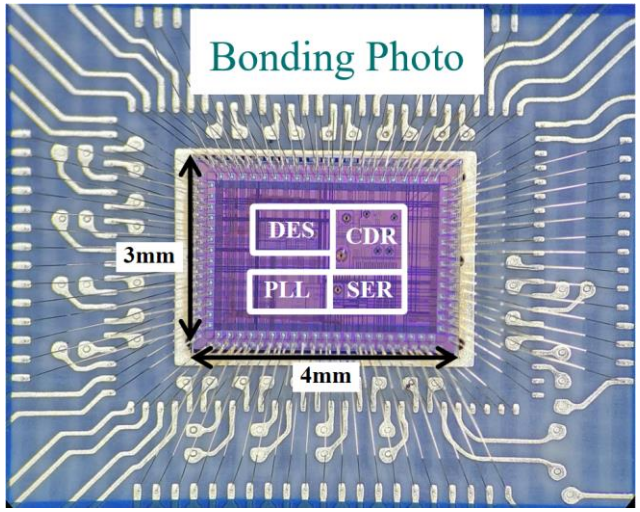
BDTIC芯片版图

BDTIC芯片



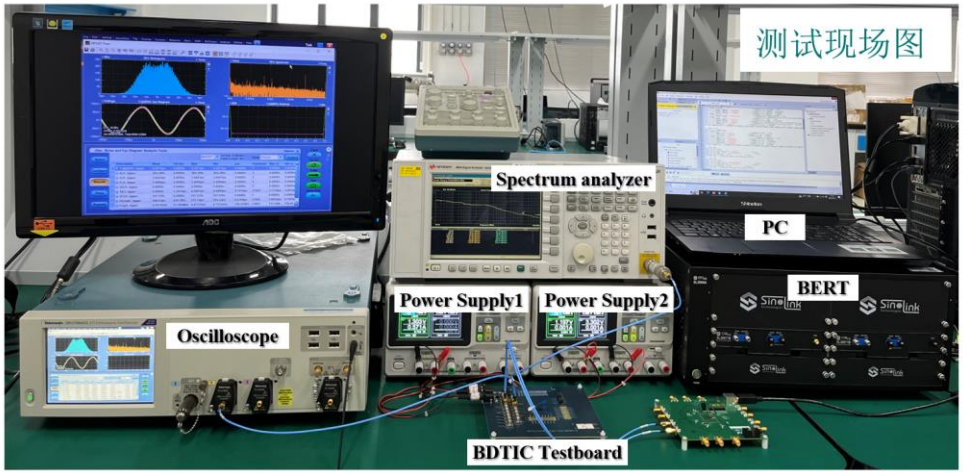
BDTIC芯片测试PCB板实物图

COB

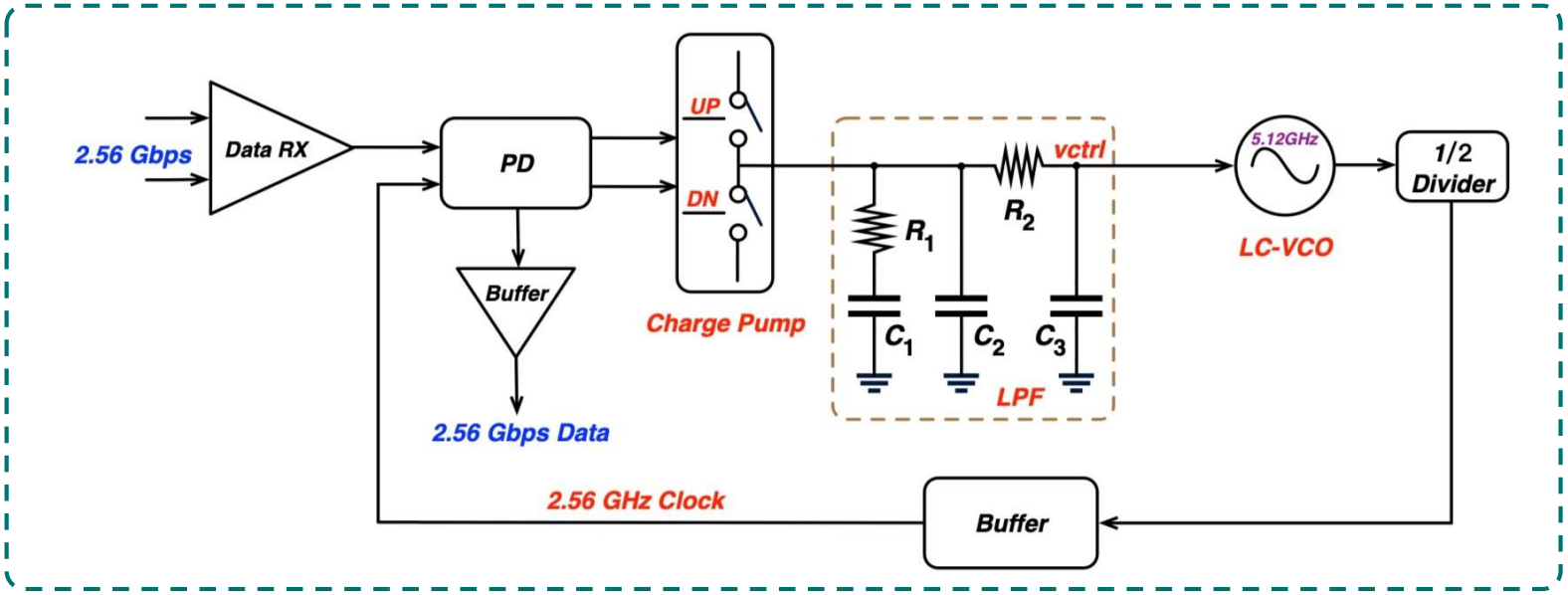


BDTIC芯片显微镜下bond线实物图

- ✓ 10 Gbps+, 40对+高速差分测试接口
- ✓ 166pin双层pad 打线、高密度高速信号扇出



BDTIC芯片中的2.56 Gbps CDR模块



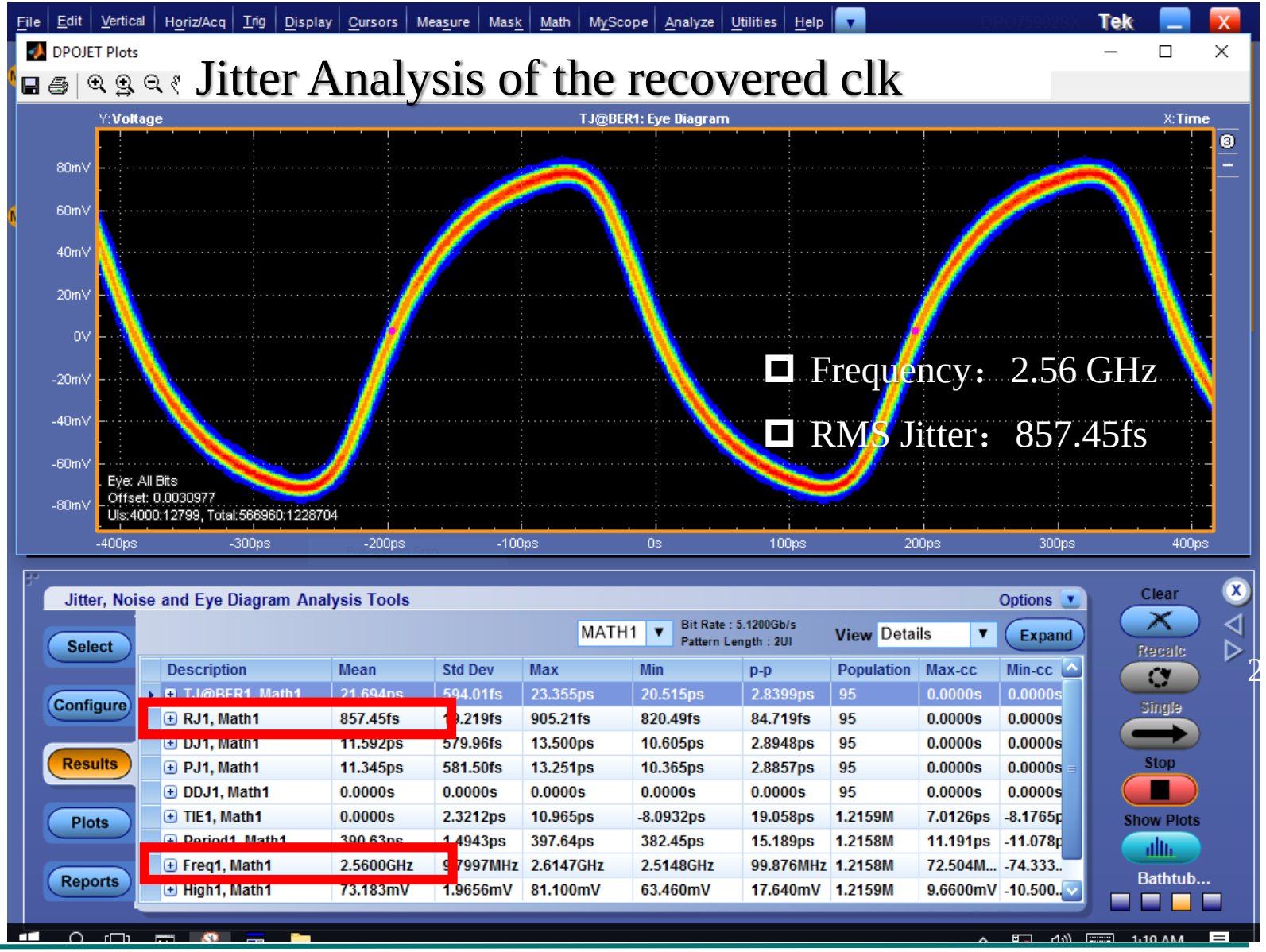
schematic block-diagram of the proposed CDR design

- ✓ PLL-based 单环路全速率CDR.
- ✓ 主要结构由：高速 Rx, Phase Detector (PD), Charge Pump (CP), Low-pass Filter (LPF) 和LC-based VCO组成

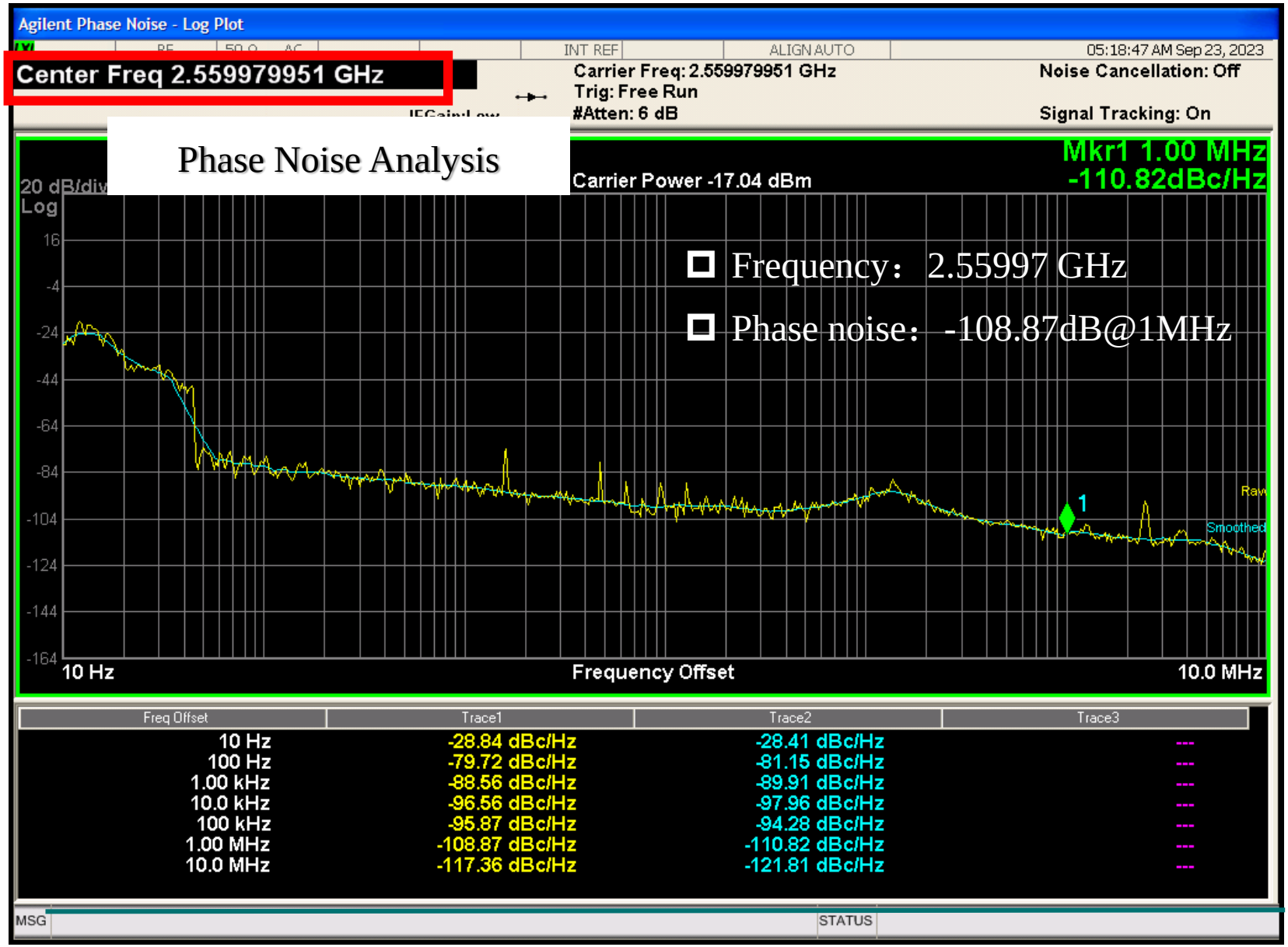
A 2.56 Gbps Clock and Data Recovery (CDR) ASIC Design for High-Energy Physics Experiments

The 2023 International Workshop on the High Energy Circular Electron Positron Collider, Nanjing, Oct 23-27

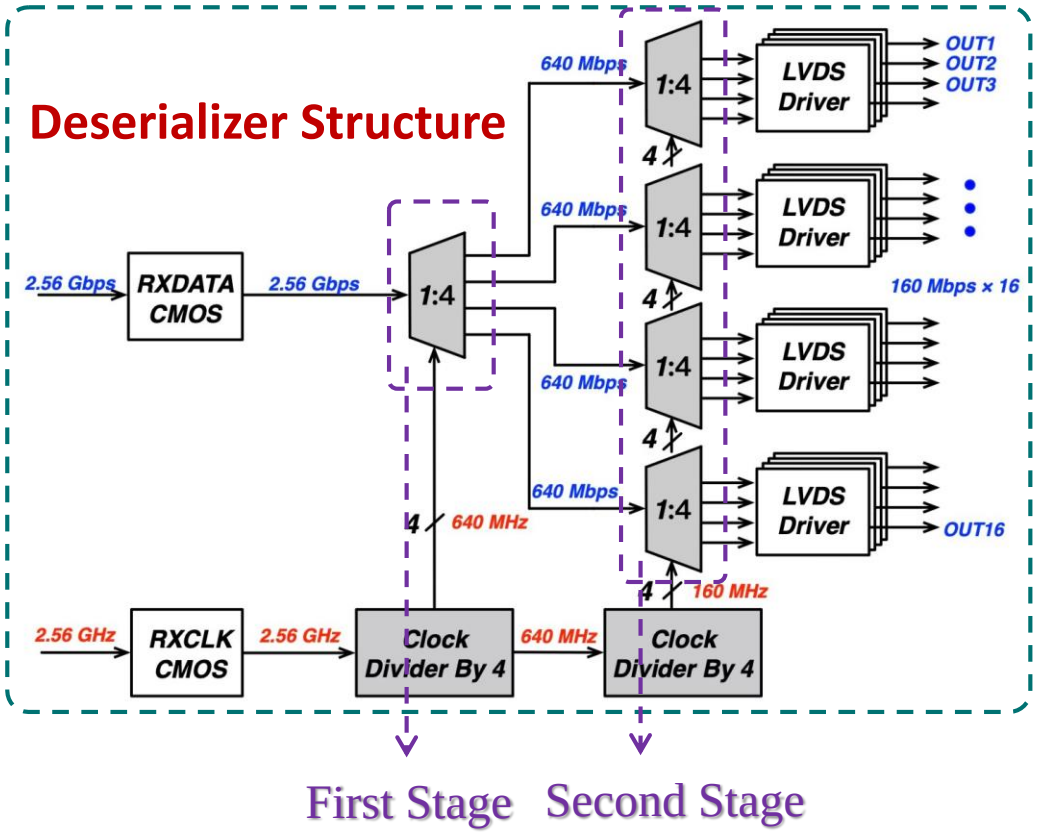
2.56 Gbps CDR模块测试



2.56 Gbps CDR模块测试



BDTIC芯片中的2.56 Gbps Deserializer模块



First Stage: 1→4

Second Stage: 4→16

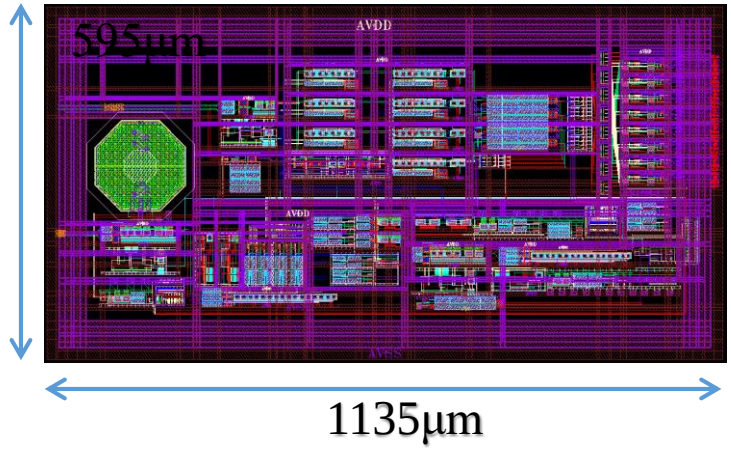
- ✓ 输入信号：2.56 Gbps串行数据
- ✓ 需要时钟：2.56 GHz时钟

（以上数据/时钟来自CDR模块）

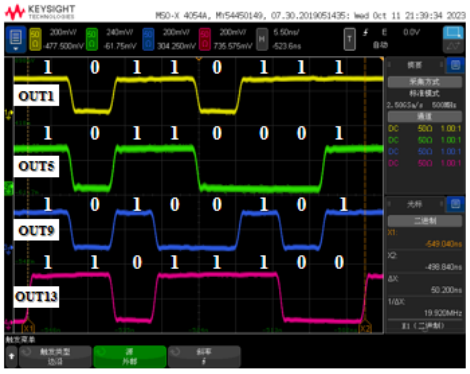
- ✓ 输出：16 x 160 Mbps/Ch

16路并行数据

- ✓ Deserializer core 大小: 1135μm ×

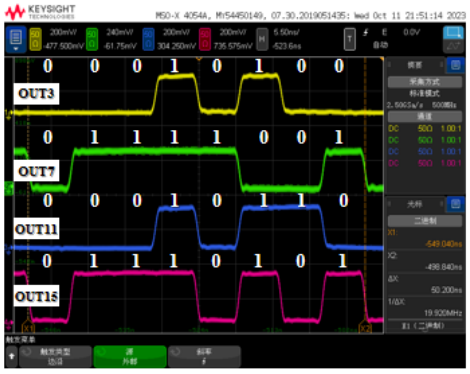


CDR + Deserializer 测试结果

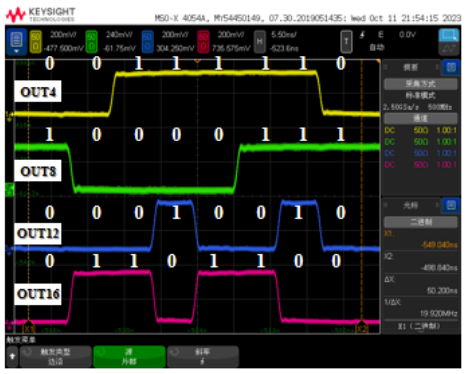


OUT1-OUT5-OUT9-OUT13

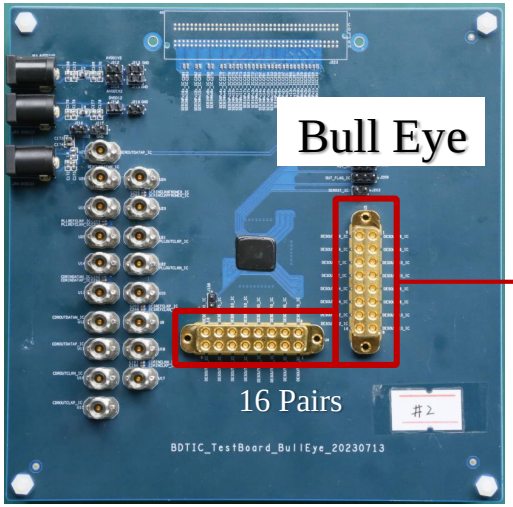
OUT2-OUT6-OUT10-OUT14



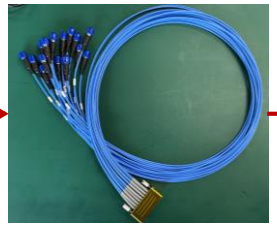
OUT3-OUT7-OUT11-OUT15



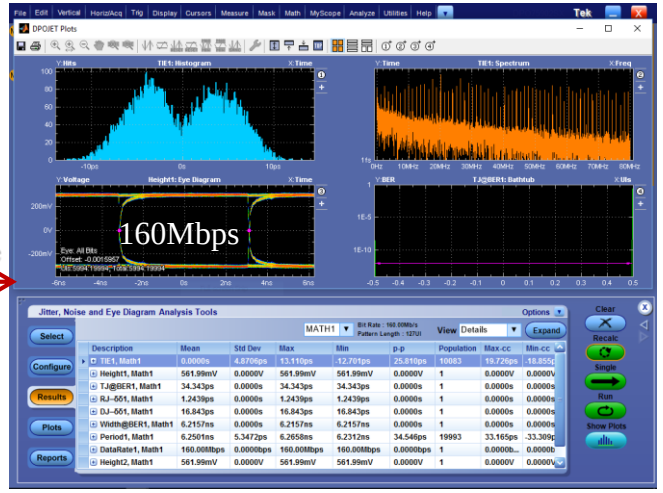
OUT4-OUT6-OUT12-OUT16



CDR + Drserializer



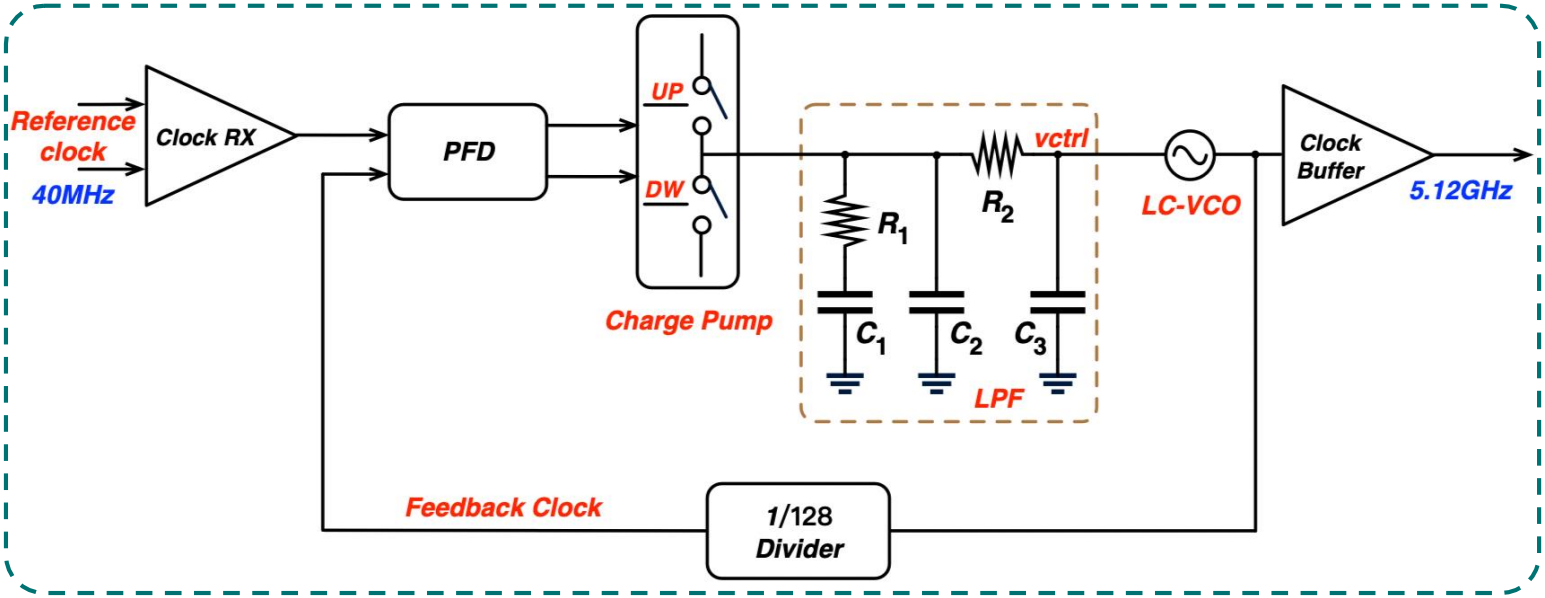
Connect to oscilloscope



Bull Eye to SAM

- ✓ 2.56 Gbps 1:16 Deserializer串并转换模块 + CDR模块联合工作
- ✓ 输出的16路并行数据（16 x 160Mbps/ch）逻辑正确，眼图清晰张开

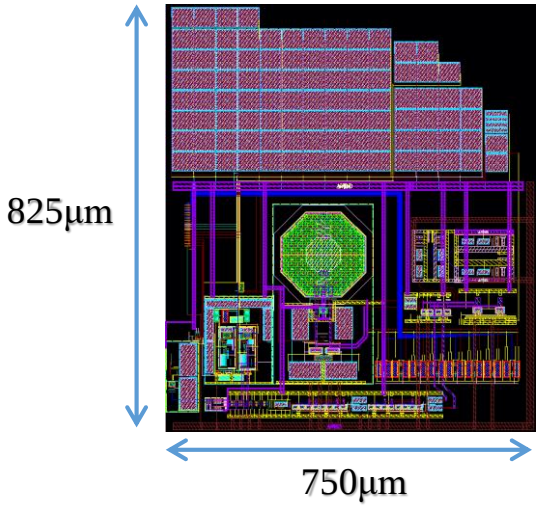
BDTIC芯片中的5.12GHz PLL模块



PLL结构框图

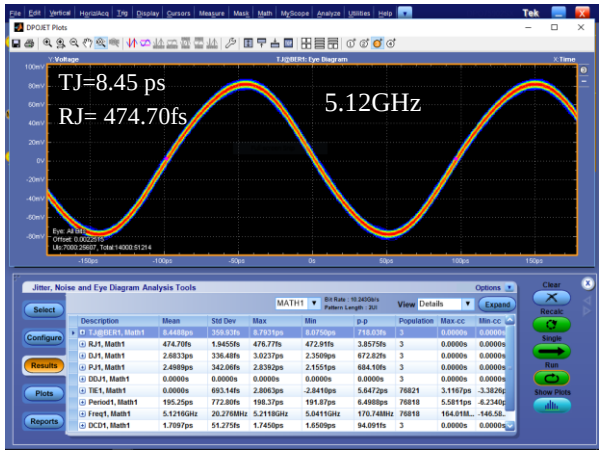
C. Zhao and D. Guo, A low noise 5.12 GHz PLL ASIC in 55 nm for NICA Multi Purpose Detector Project, Journal of Instrumentation, 2022_JINST_17_C09003*

- ✓ 该PLL子模块于2021年设计，2022年流片验证成功
- ✓ 进一步优化后使用于BDTIC芯片中

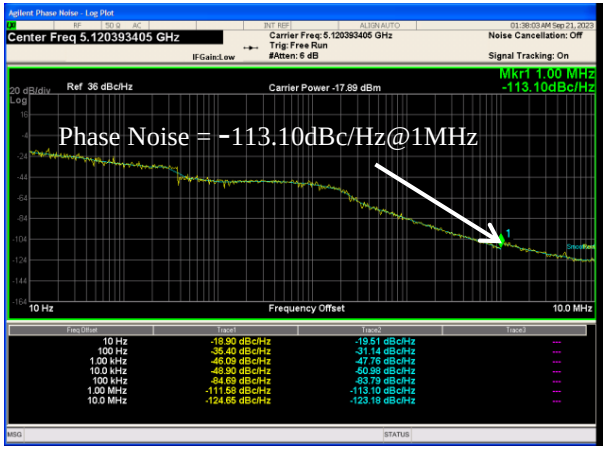


5.12GHz PLL模块测试结果

Jitter analysis



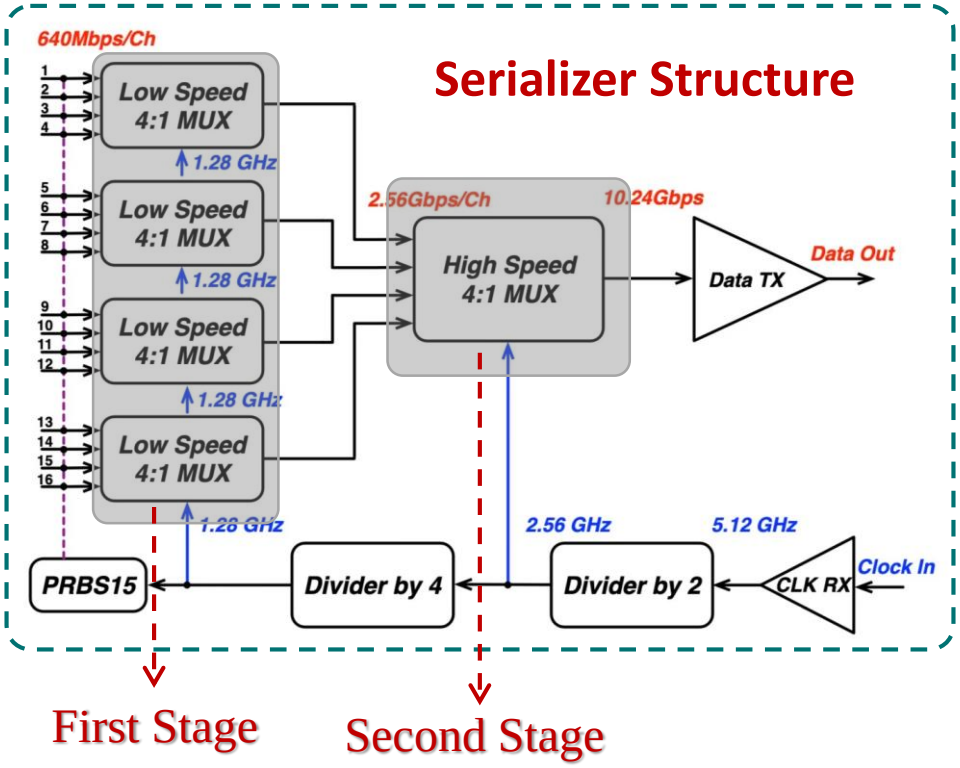
Eye Diagram



Phase Noise Curve

- ✓ Frequency：5.12 GHz
- ✓ RMS Jitter：474.70 fs
- ✓ Phase noise：-113dB@1MHz

BDTIC芯片中的10.24 GHz Serializer



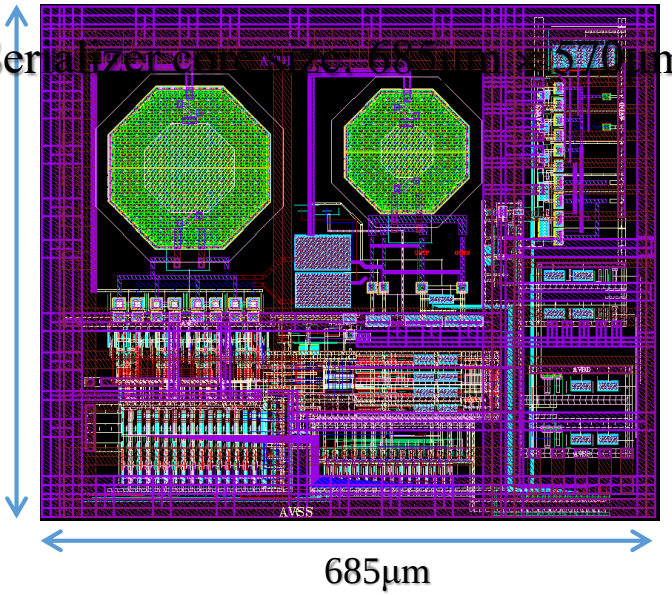
- ✓ 输入：来自PRBS15自检模块产生的16路 640 Mbps/Ch 信号
- ✓ 需要时钟：5.12 GHz

（该时钟来自于5.12 GHz PLL模块）

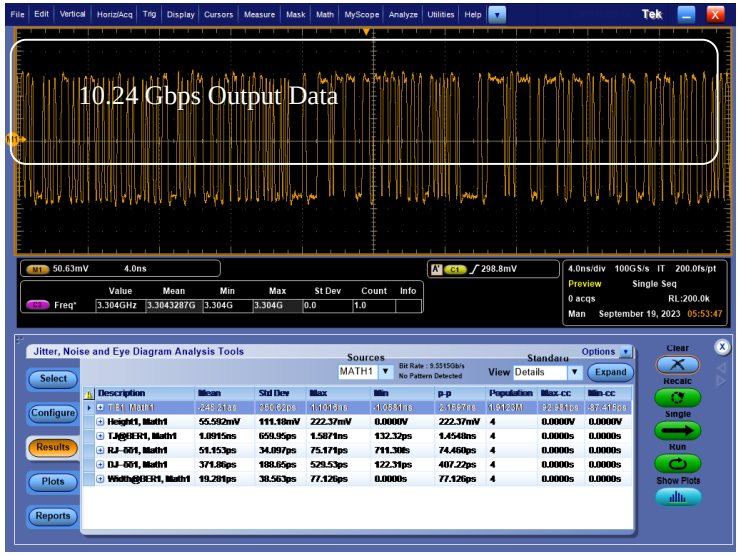
- ✓ 输出：10.24 Gbps高速串行数据
- ✓ Serializer Size: 685μm × 570μm

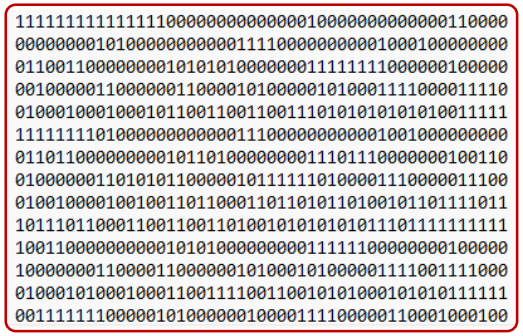
- ✓ First Stage: 16→4 （较低速使用CMOS逻辑）
- ✓ Second Stage: 4→1 （高速差分CML逻辑）

- ✓ PRBS15自检模块：产生16路 640Mbps/ch测试数据



PLL + Serializer 测试结果

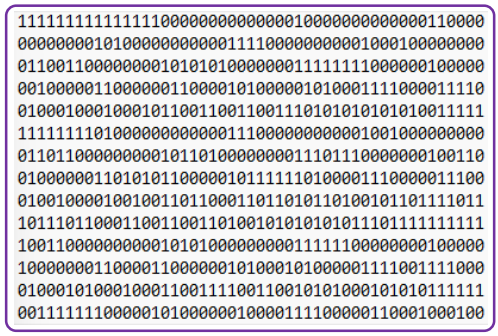




从实时示波器获取

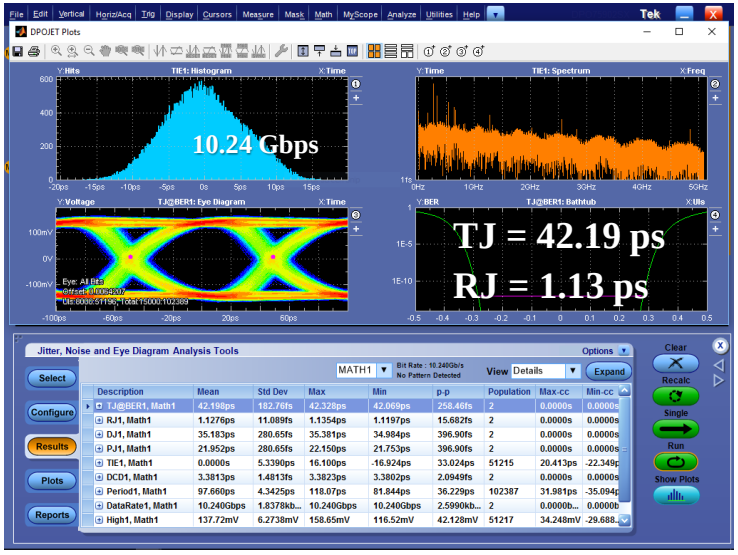
波形数据恢复出0/1

符合



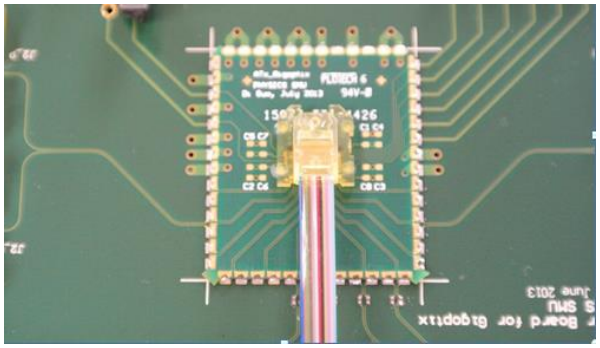
PRBS15序列

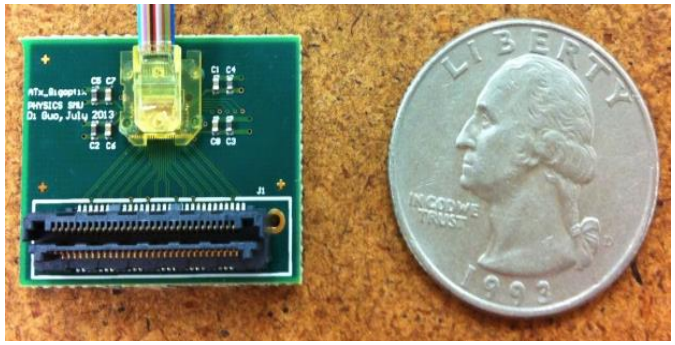
（15个1为种子）

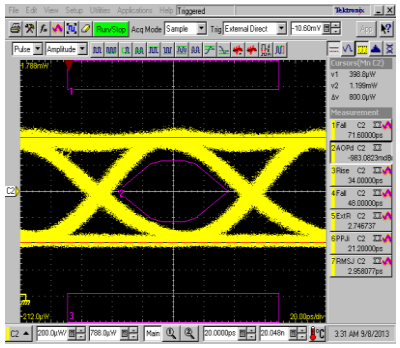


- ✓ 输出逻辑检测正确
- ✓ 输出的10.24 Gbps眼图
- ✓ Total Jitter = 42.19 ps
- ✓ RMS Jitter = 1.13 ps

光模块与其中芯片

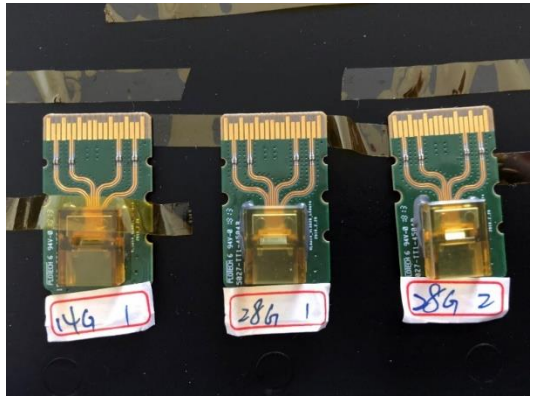






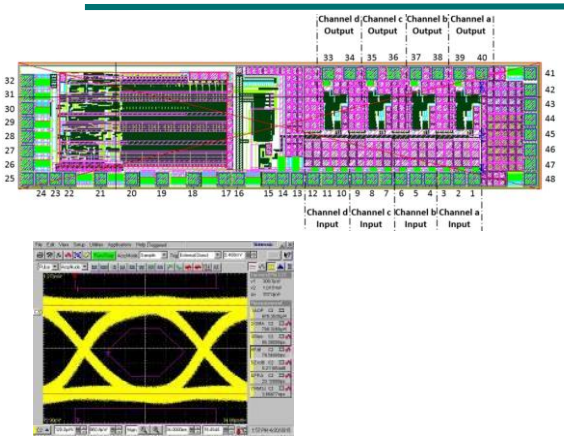
2014年 12通道阵列式光发送模块（ATx） TWEPP2013, TWEPP2014

- ✓ 研发了高能物理应用领域第一个12通道阵列式定制化光模块ATx（TWEPP2013,2014）
- ✓ CERN的VTRx+光模块沿用了ATx其中的光耦合方案
- ✓ 光耦合器件总剂量辐照验证
- ✓ 单通道形式/ 阵列式光模块均可定制
- ✓ 光耦合器件、组装等依靠光模块厂商
- ✓ 可靠性、耐用性待验证、完善
- ✓ 光纤的辐照测试选型有待进一步验证、测试

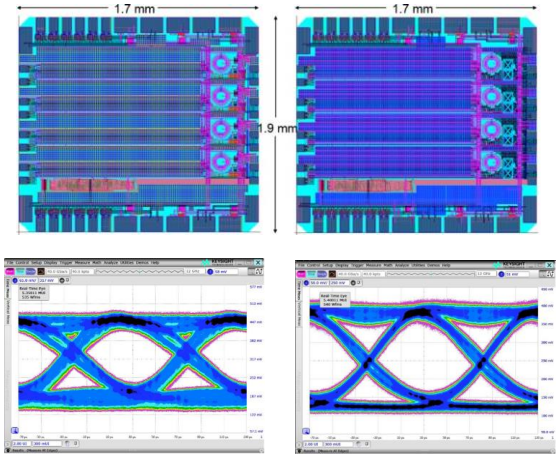


2022年4通道阵列式光发送模块

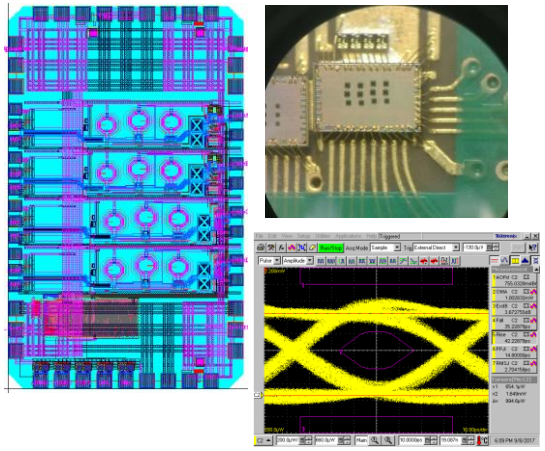
光模块与其中芯片



激光器驱动芯片 **5 Gbps/ch**
2014年 0.18um工艺



激光器驱动芯片 **4 x 10Gbps/ch**
2016年 TSMC 65nm工艺



激光器驱动芯片 **4 x 14Gbps/ch**
2022年 SMIC 55nm工艺

- ✓ 在SOS 0.18um, Global Foundry 65nm, TSMC 65nm, SMIC 55nm等工艺上成功设计验证过多款不同速率的激光器驱动芯片，有较成熟的经验积累。
- ✓ 抗辐照尚未测试验证
- ✓ 多通道性能尚要进一步验证优化
- ✓ 可靠性、良品率等尚未评估
- ✓ 功耗、面积优化
- ✓ TIA跨导芯片尚在初步设计验证阶段

THANKS!