

# HGCAL Module Assembly Center in Taiwan

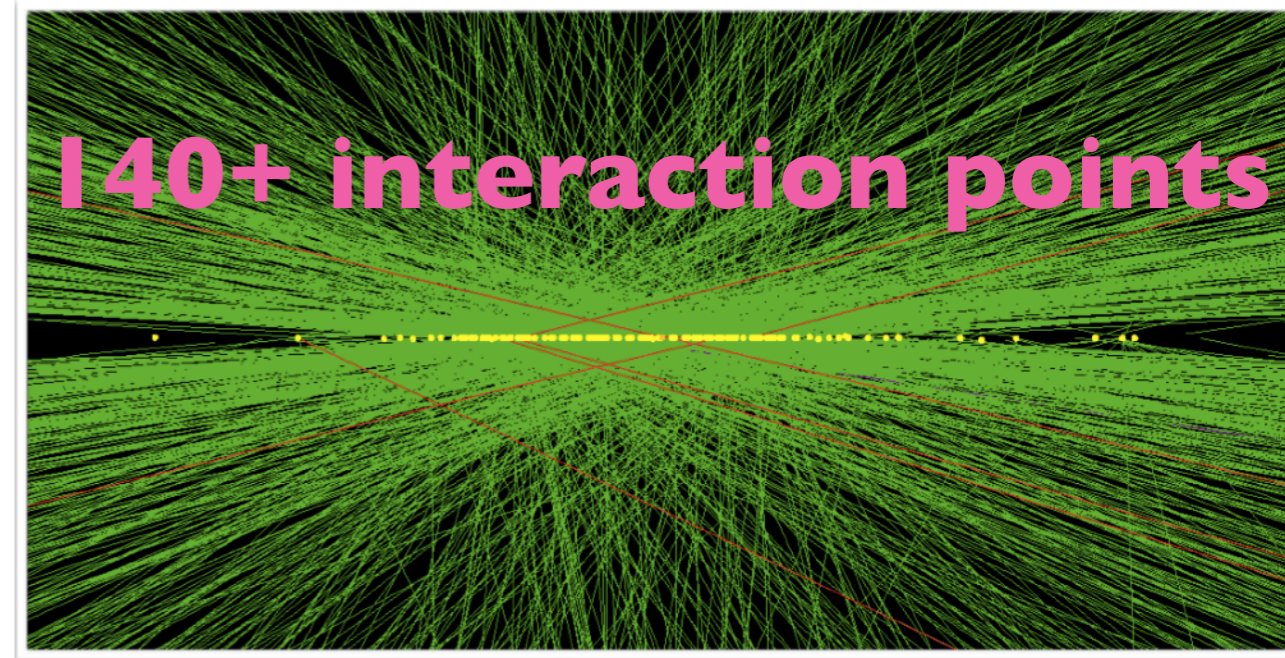
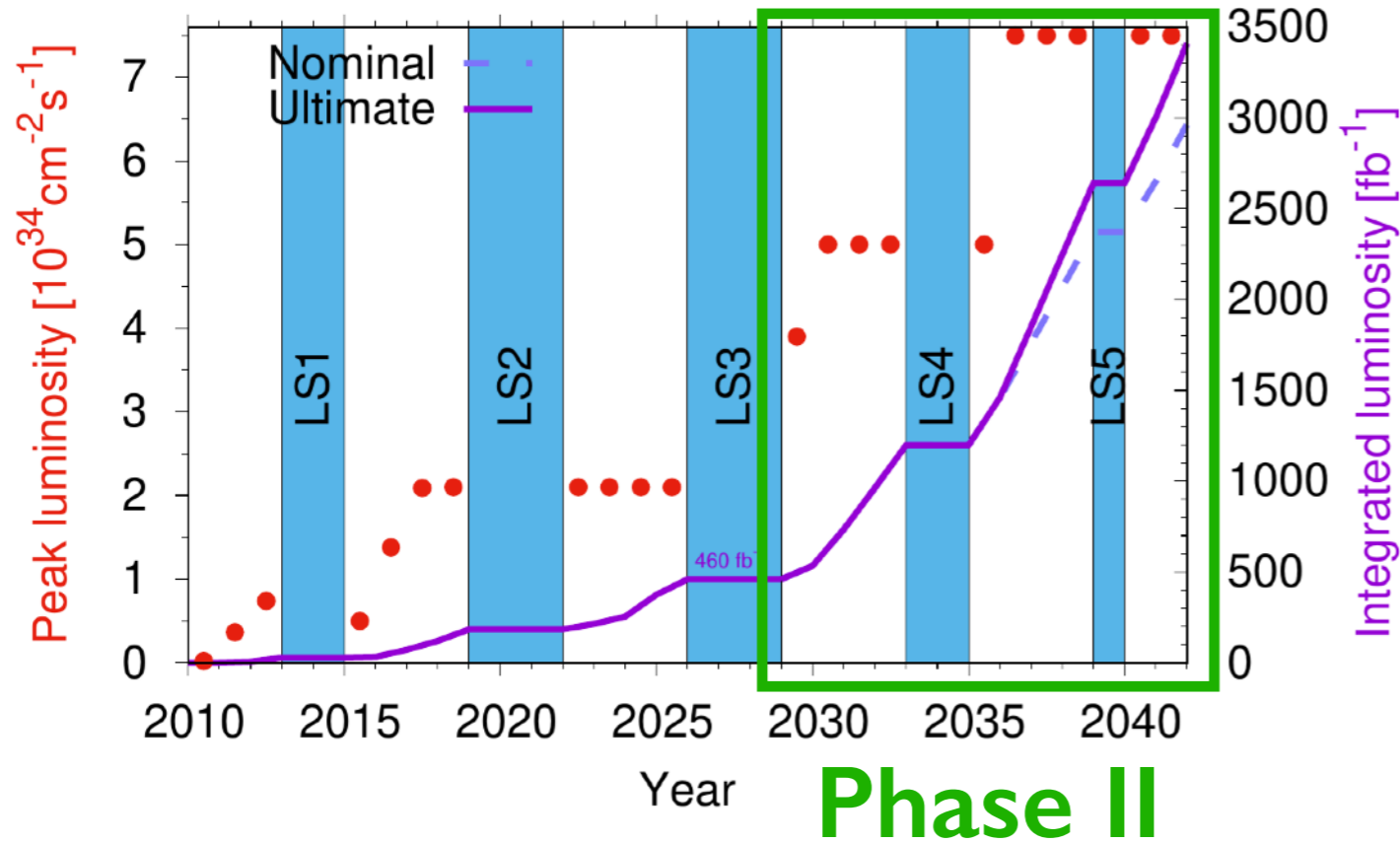
TIDC annual Meeting — November 22, 2024

You-Ying Li on behalf of Taiwan MAC

National Taiwan University

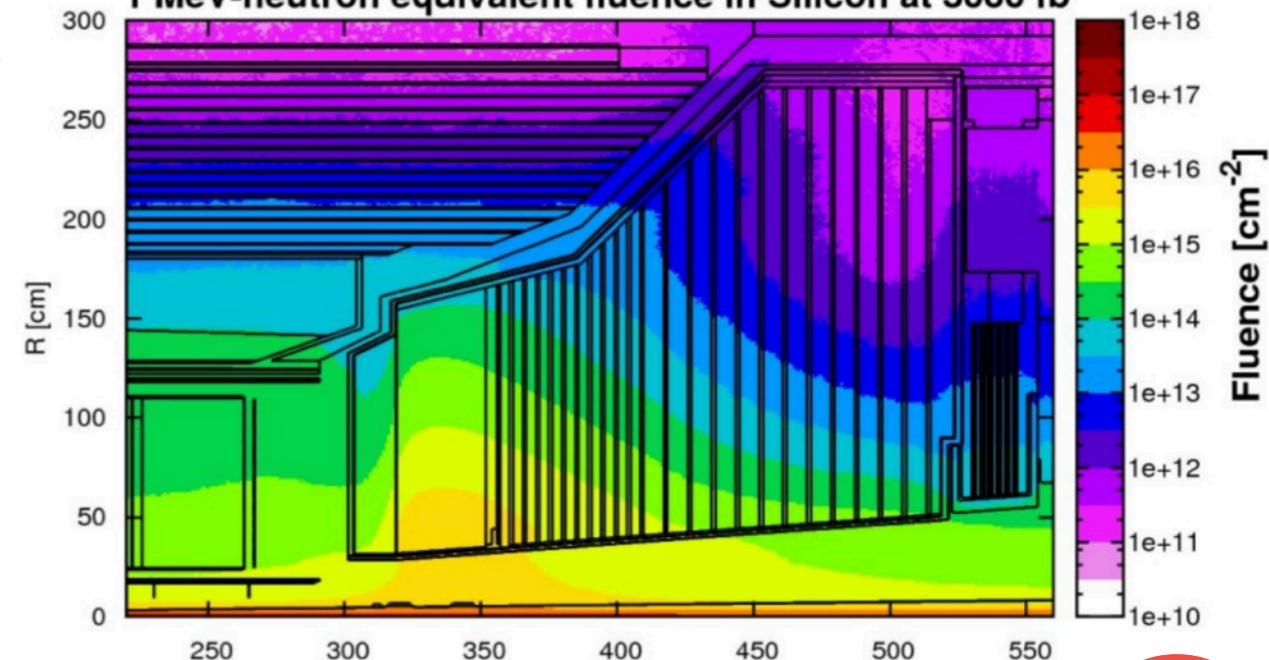


# HL-LHC project



CMS p-p collisions at 7 TeV per beam

1 MeV-neutron equivalent fluence in Silicon at  $3000 \text{ fb}^{-1}$



\* Integrated luminosity will be increased over  $3000 \text{ fb}^{-1}$  to get more data statistics for new physics search.

→ More radiation, more pile-up, higher density of tracks ...

\* Calorimeter endcaps with high radiation background is especially challenge ( $10^{14}$  current  $\rightarrow 10^{16} n_{\text{eq}} / \text{cm}^{-2}$  Phase II).

→ High radiation tolerance of sensors and electronics

→ Precise timing measurements and high granularity

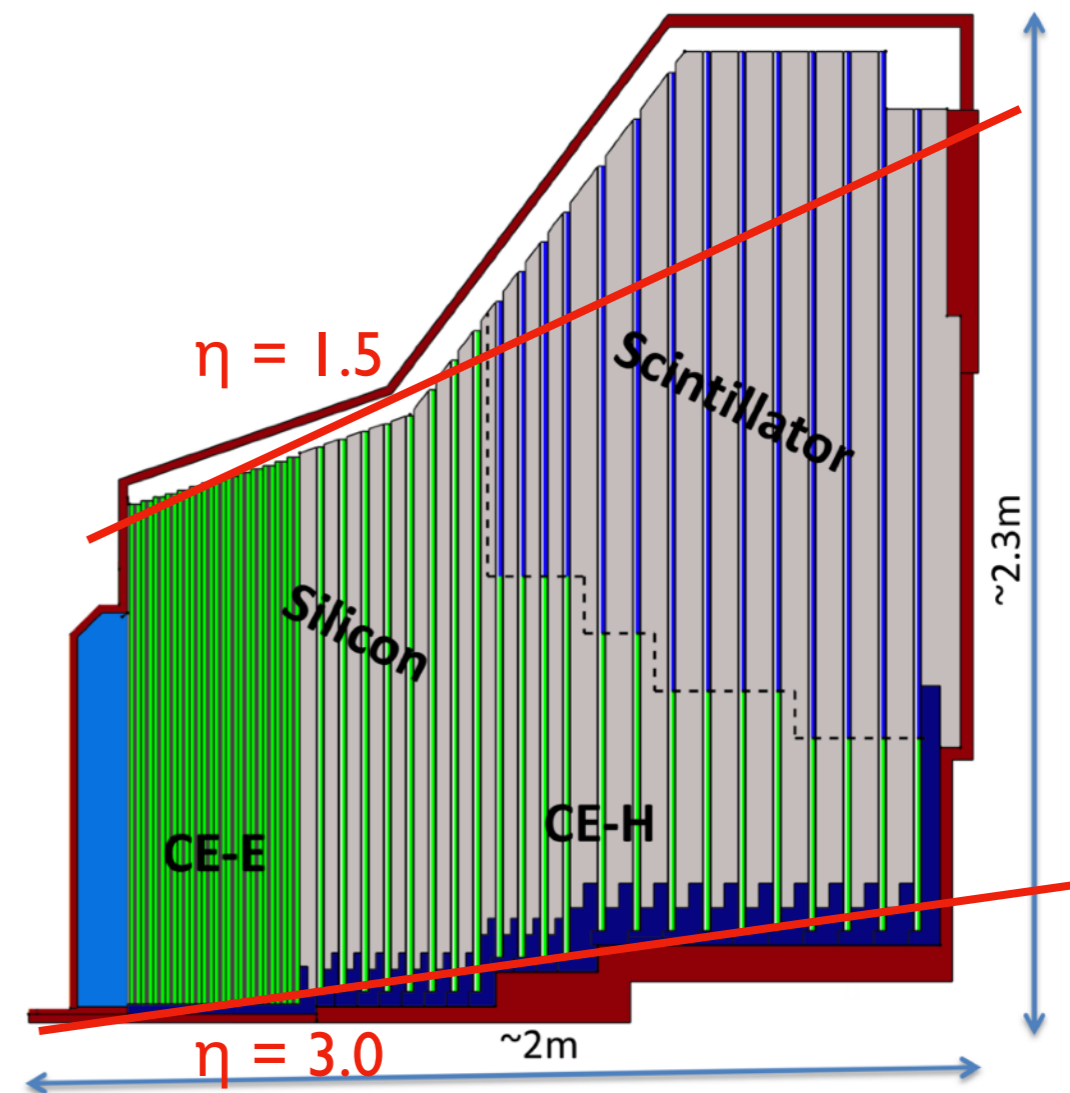
# HGCAL overview

- \* The HGCAL detector is CMS Phase II upgrade in the endcap calorimeter, replacing the ECAL and HCAL in endcap regions.
- \* A sampling detector with three parts:
  - CE-E : 26 layers of silicon modules with Cu/Pb absorbers.
  - CE-H : 21 layers of silicon modules with Cu and thick steel absorbers.
  - Scintillator : SiPM to tiles with Cu and thick steel absorbers.

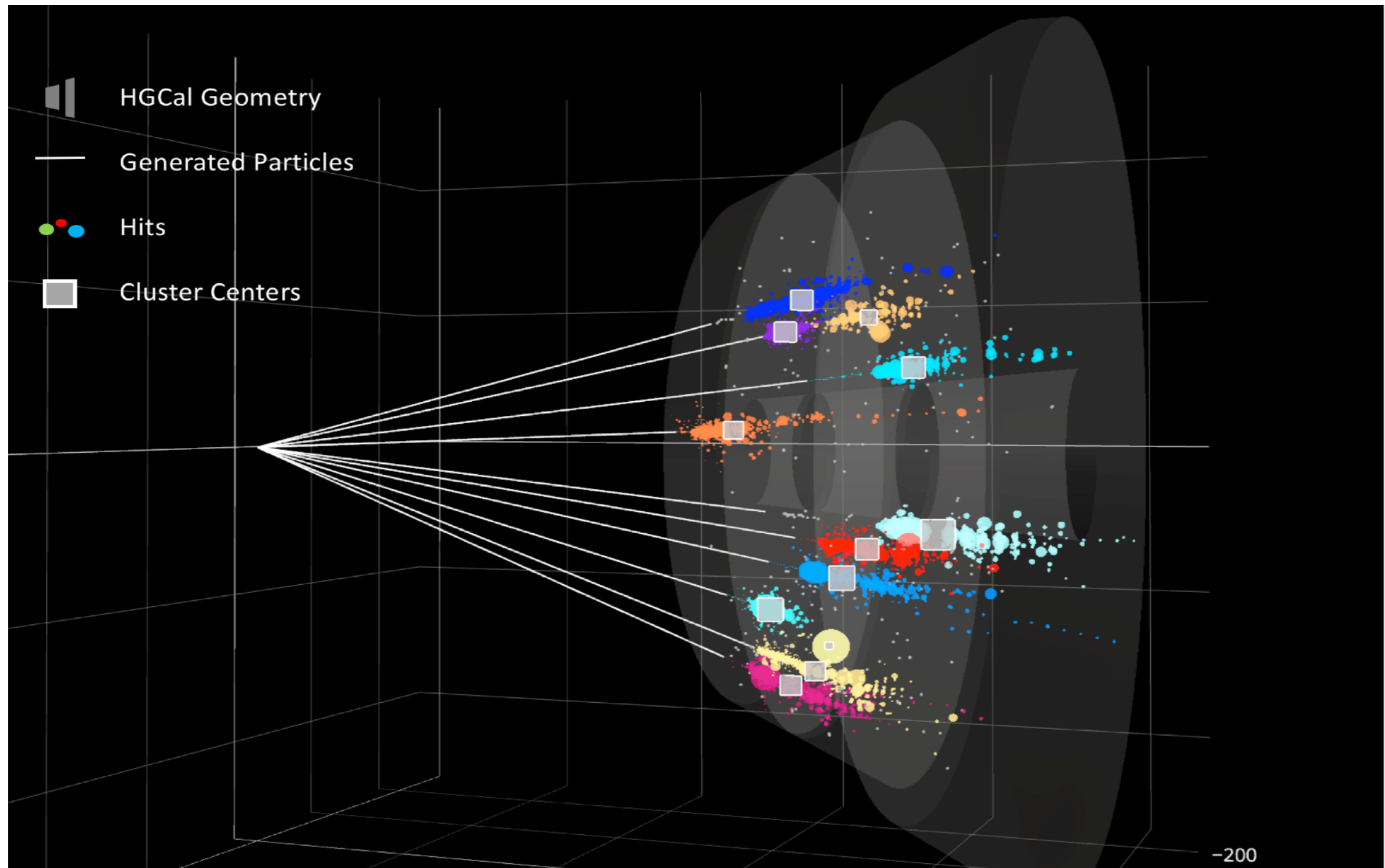
## Key parameter:

- Cover  $1.5 < |\eta| < 3.0$
- Full system maintained at  $-30\text{ }^{\circ}\text{C}$
- 6 M channels with 27 K silicon modules
- Silicon cells of size of **0.5** (HD) and **1.1** (LD)  $\text{cm}^2$

ECAL endcap is a size of **8.2**  $\text{cm}^2$  front-face



# HCGAL shower

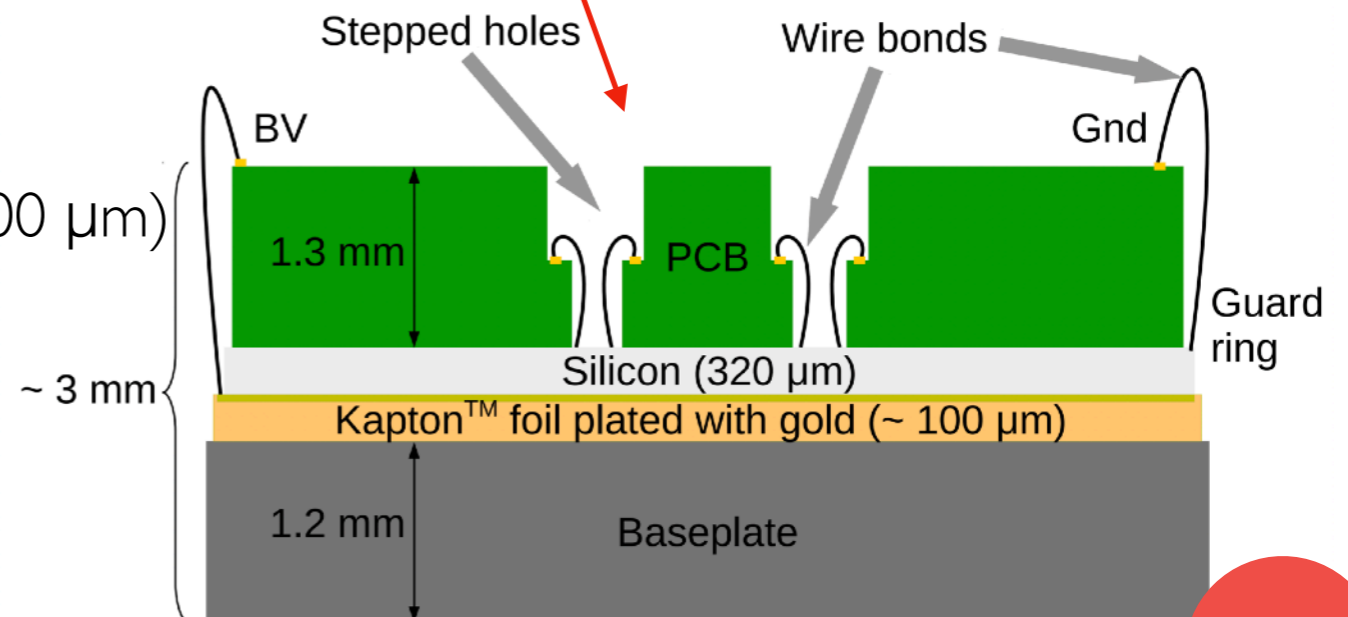
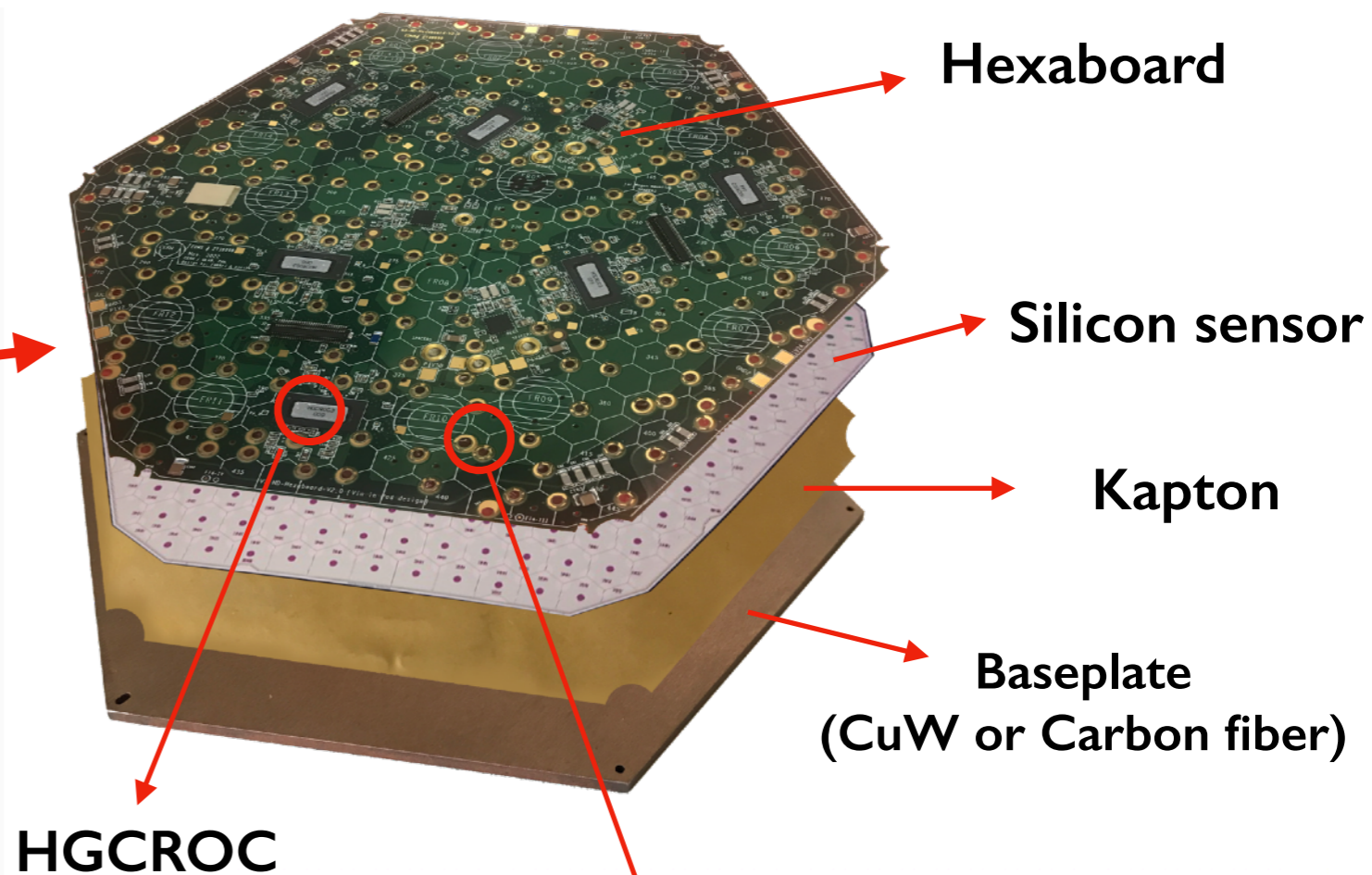
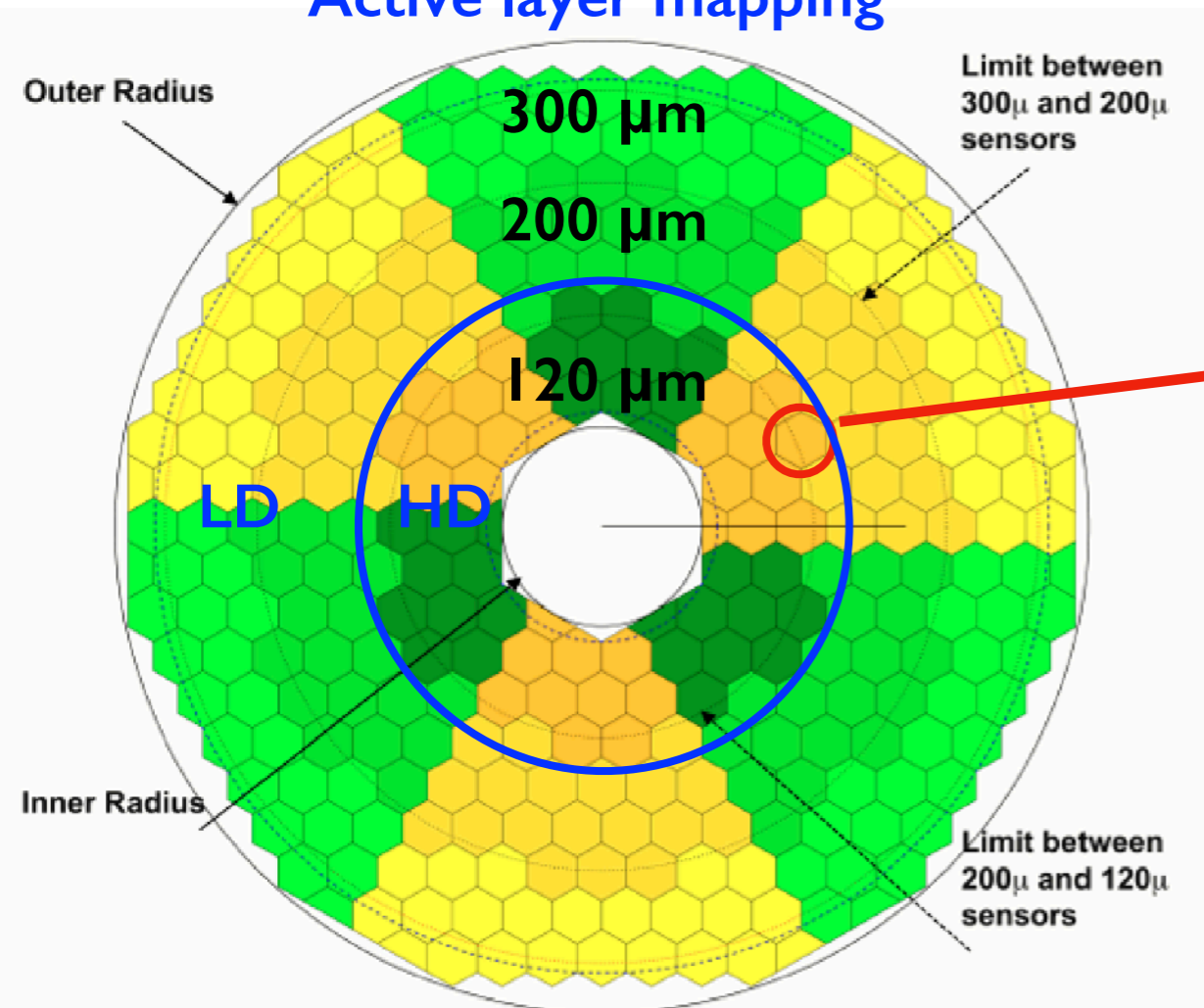


Precise 5D information (position, time and energy) for particle showers



# 8 inch Silicon Module

## Active layer mapping



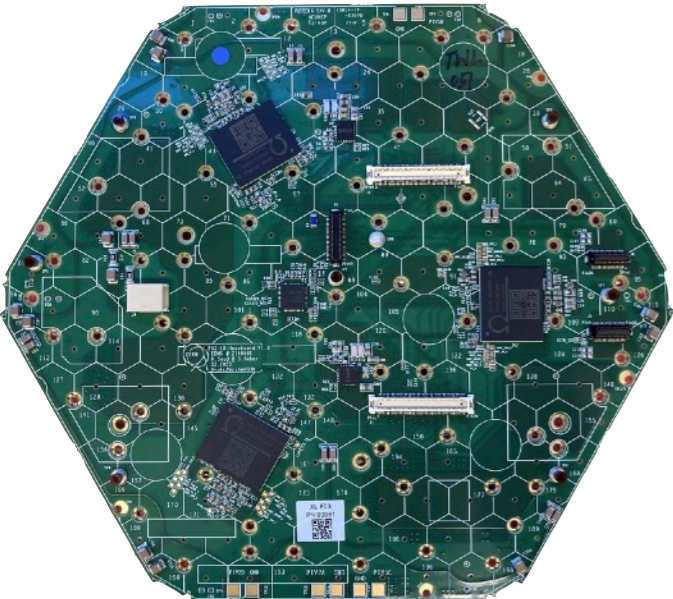
## Requirement

- ✓ Small offset between HB/Sensor/Baseplate ( $< 100 \mu\text{m}$ )
- ✓ High radiation tolerance ( $> 1.5 \text{ MGy}$ )
- ✓ 850 HV available for bias
- ✓ Low noise for each readout channel
- ✓ Temperature change tolerance ( $-40 \sim 20^\circ\text{C}$ )

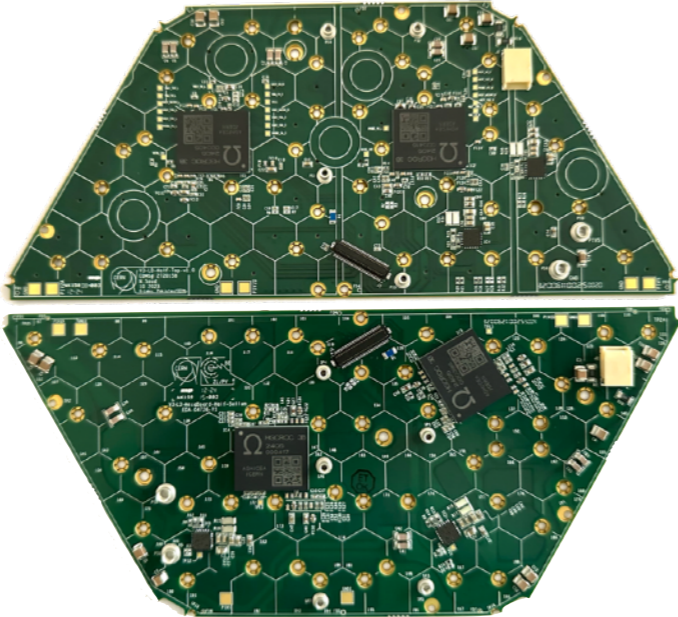


# More shapes

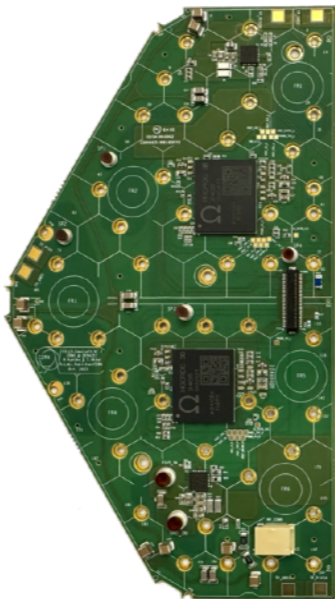
LD FULL



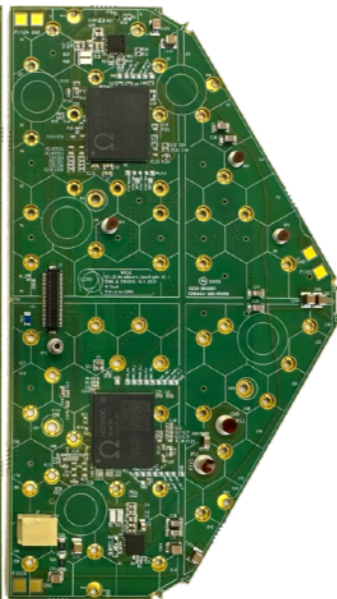
LD TOP



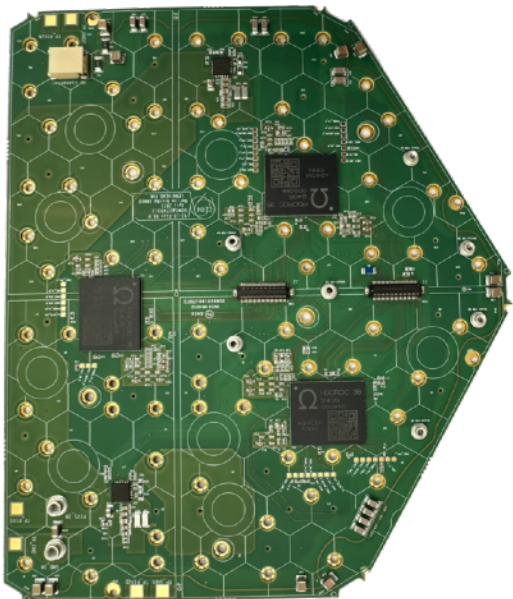
LD LEFT



LD RIGHT

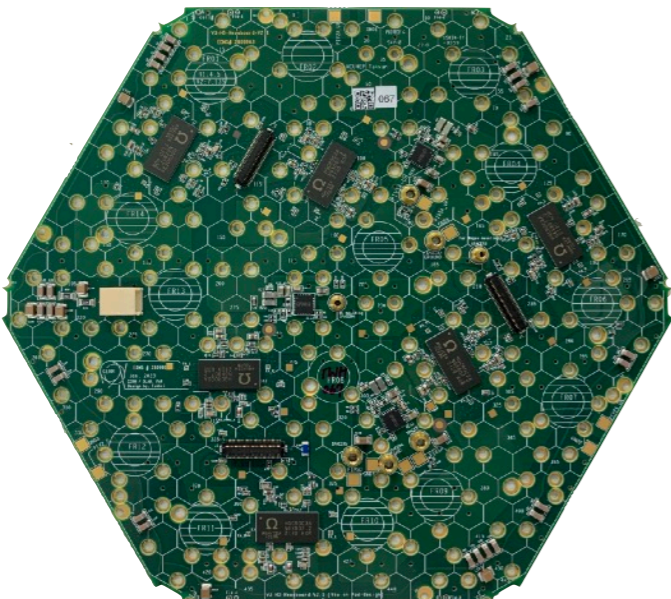


LD FIVE

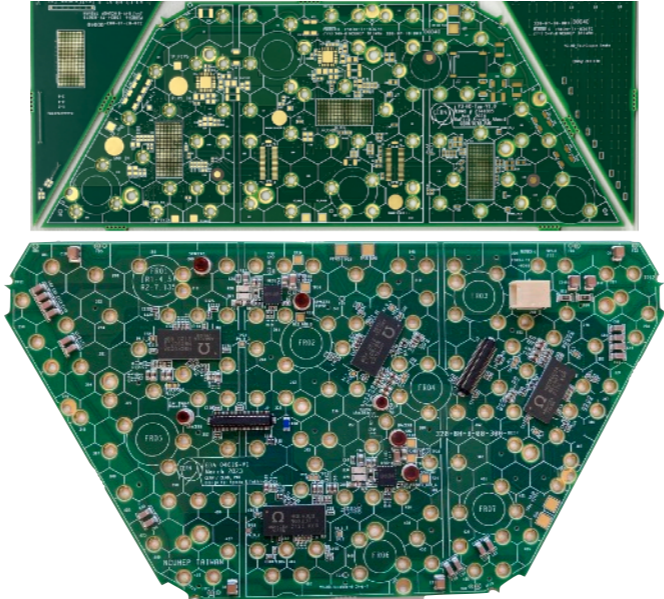


LD BOTTOM

HD FULL



HD TOP

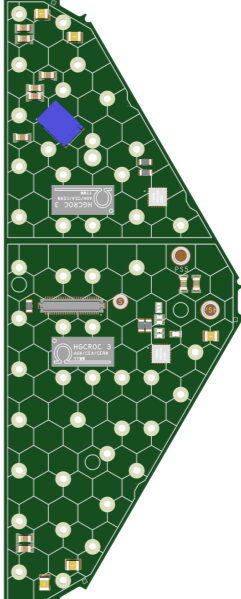


HD BOTTOM

HD LEFT



HD RIGHT

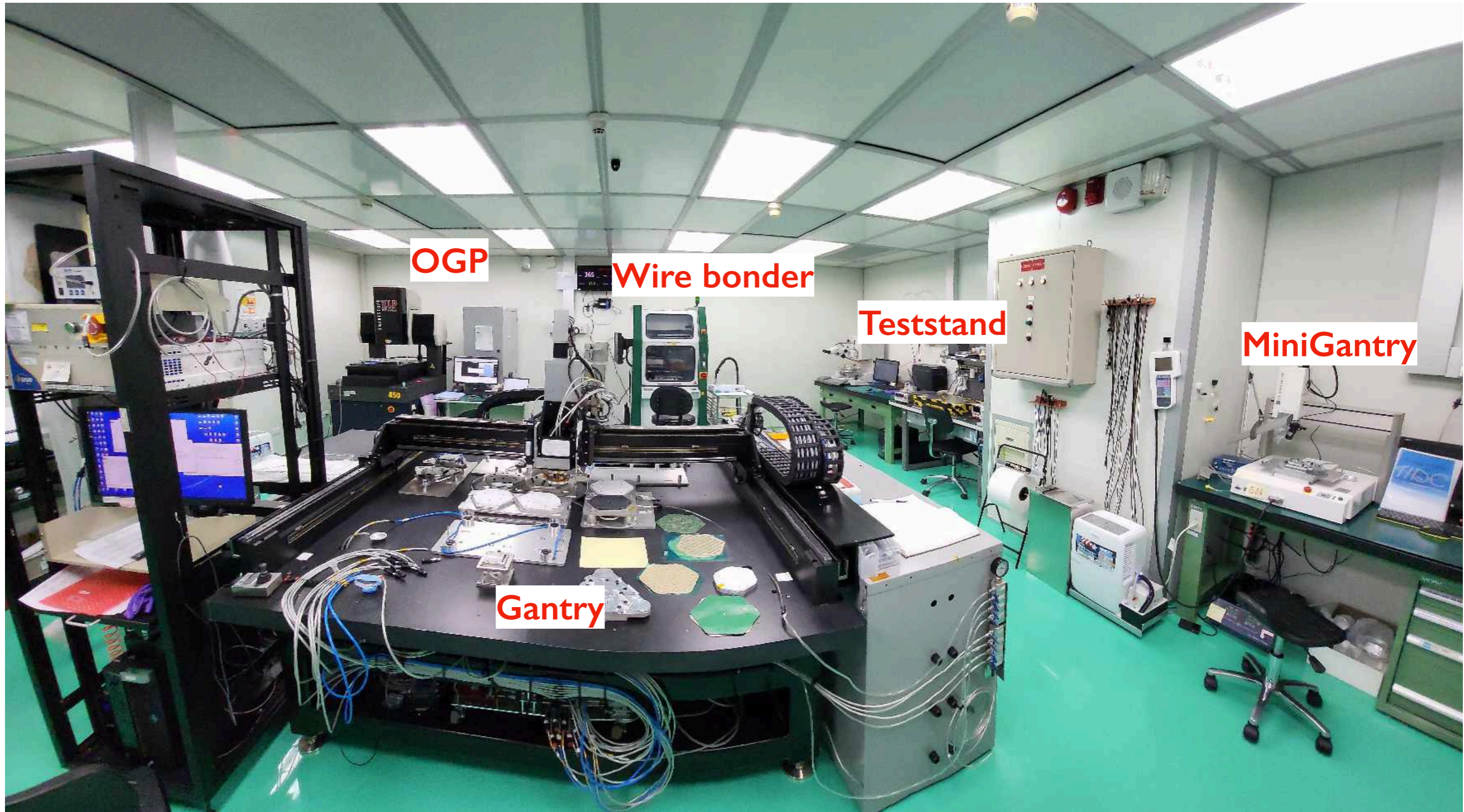




# Taiwan HGICAL MAC overview

- \* The HGICAL MAC in Taiwan are established in 2018.
- \* Taiwan MAC (NTU+NCU) is one of 6 HGICAL MACs (NTU+NCU Taiwan, IHEP China, TIFR India, UCSB US, TTU US, CMU US)
- \* Hosts main module assembly and shipping and contact Ploteck for hexaboard fabrication.
- \* Around 5000 pieces of silicon modules need to be made in two years.

# Clean room for Taiwan MAC

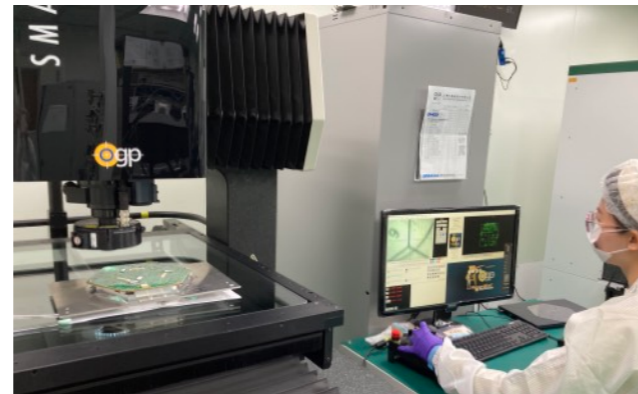




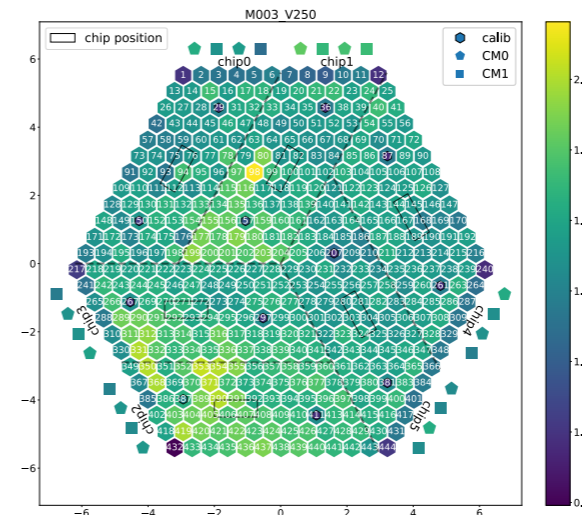
# MAC : From material to module

Material

Assembly



OGP QC



Electronic test



Thermal cycle

Wire bonding



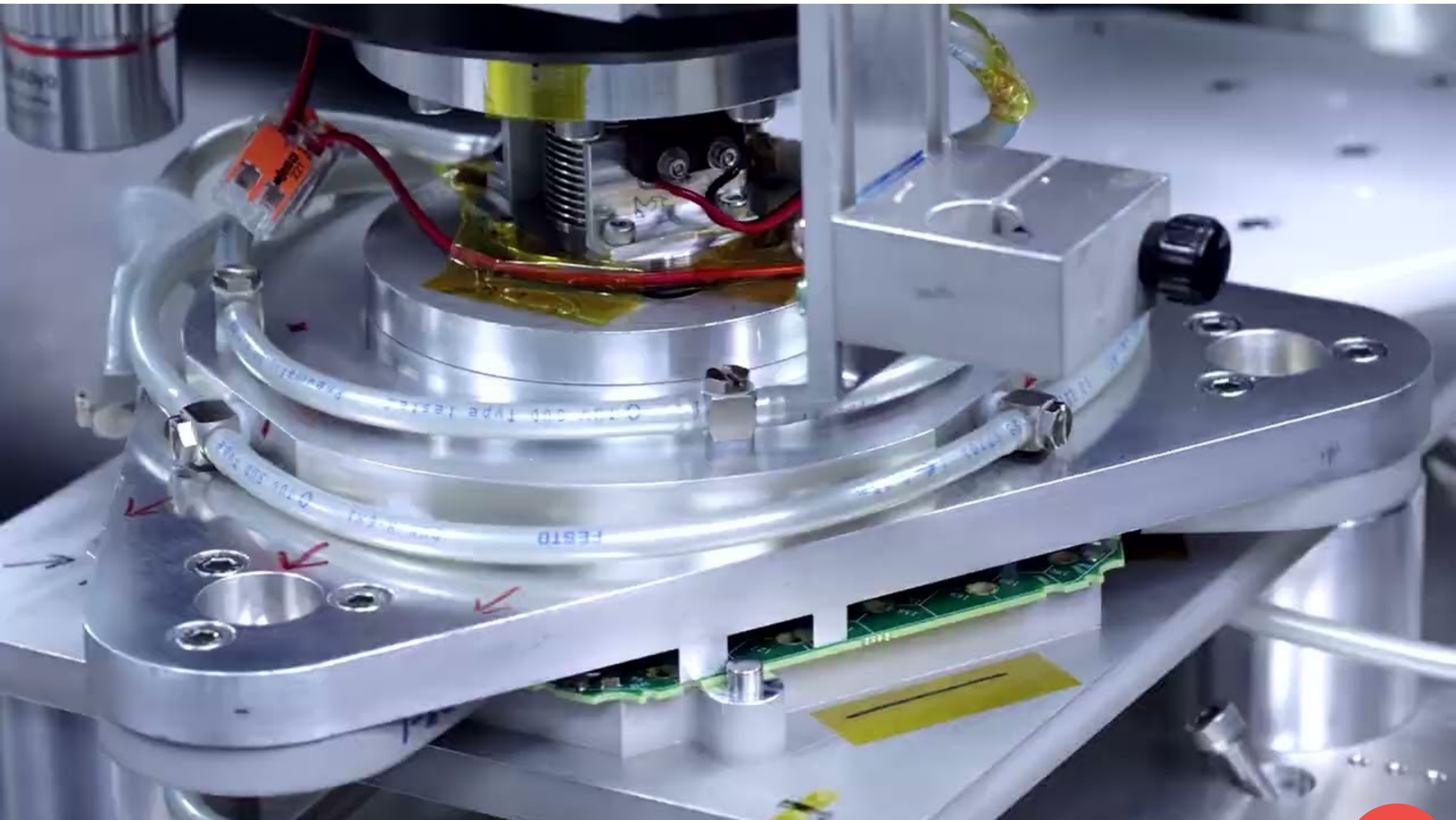
Encapsulation



Module

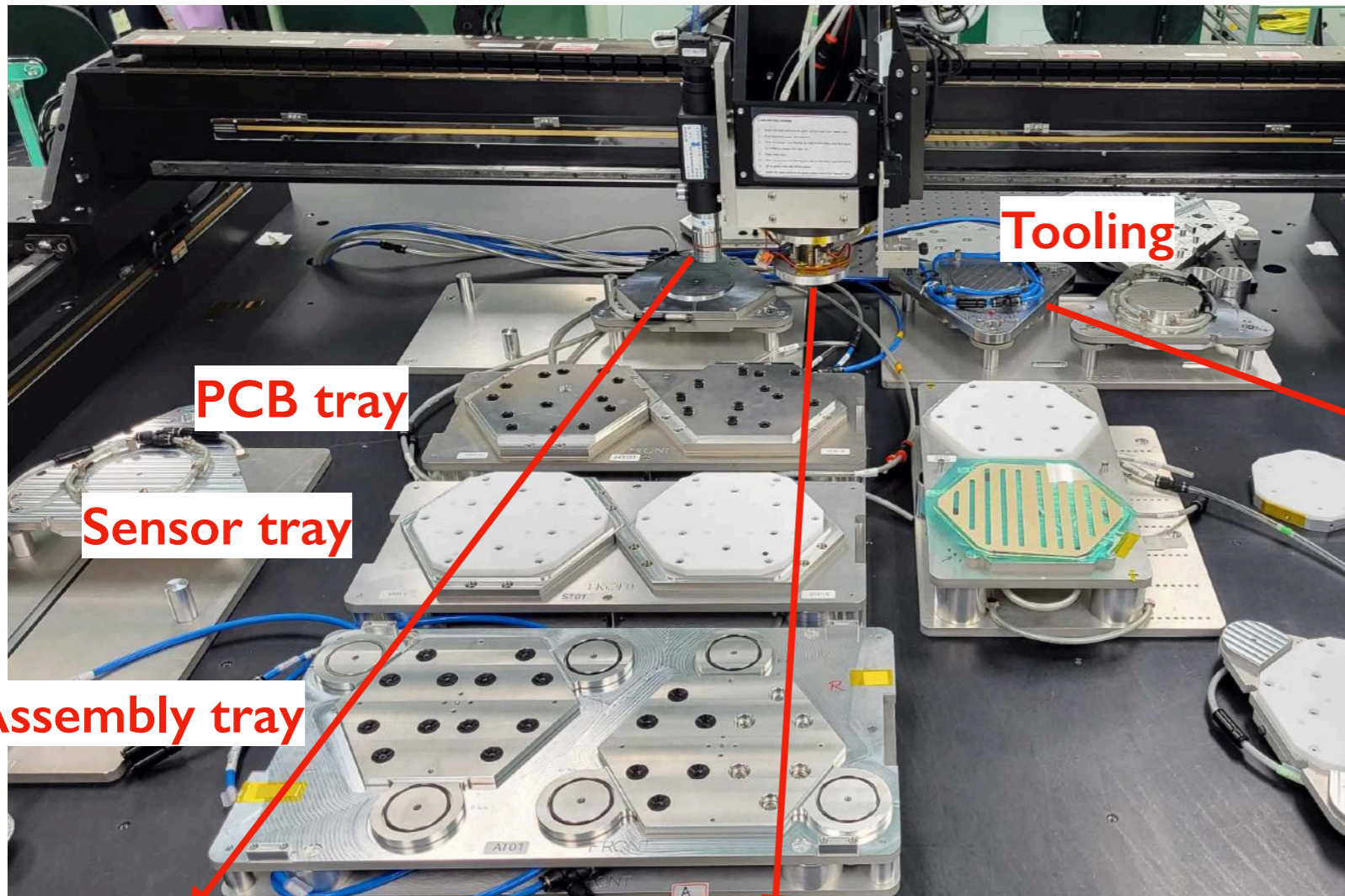


# Module assembly step





# Gantry overview



PCB tray

Sensor tray

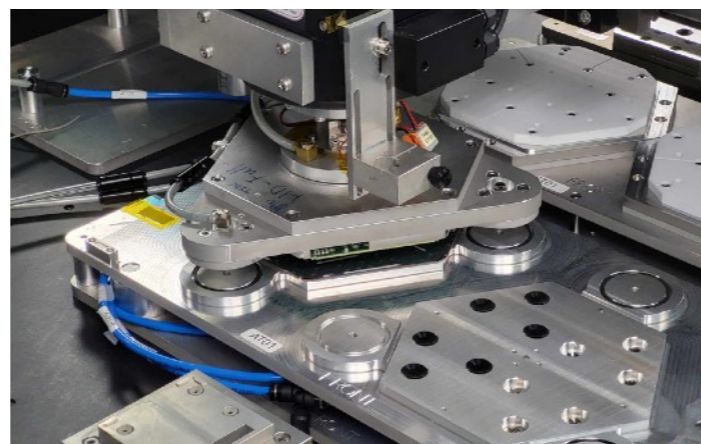
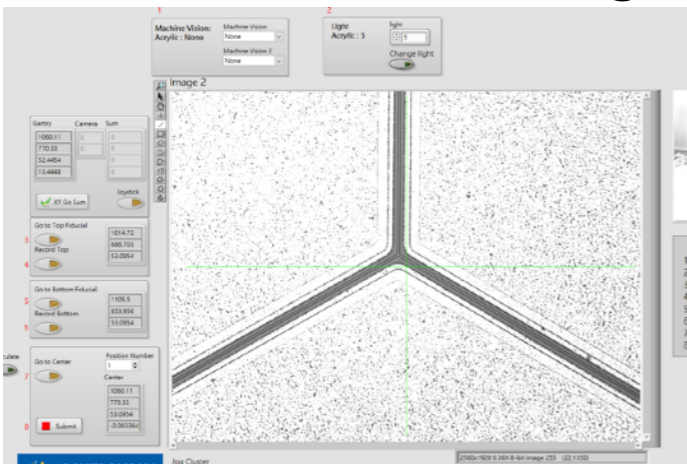
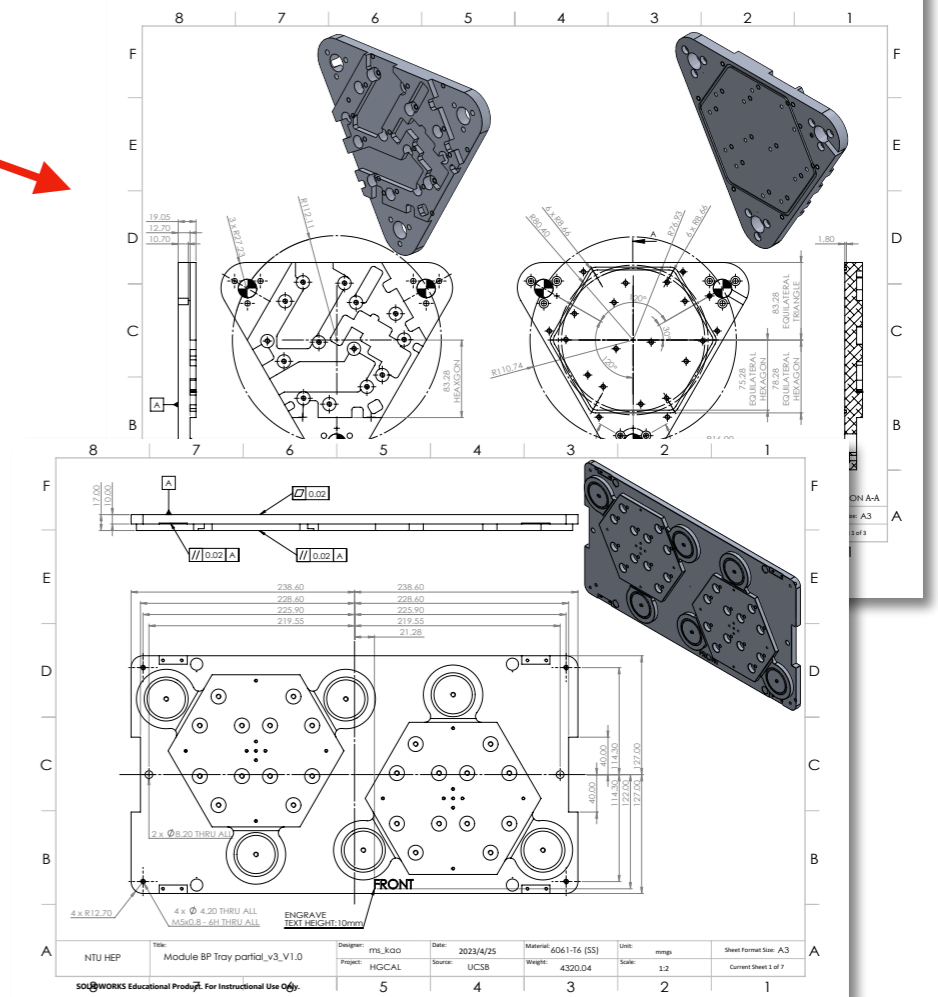
Assembly tray

Tooling

Camera for locating

Pick and place by vacuum

Assembly jigs designed at NTU and fabricated at AS





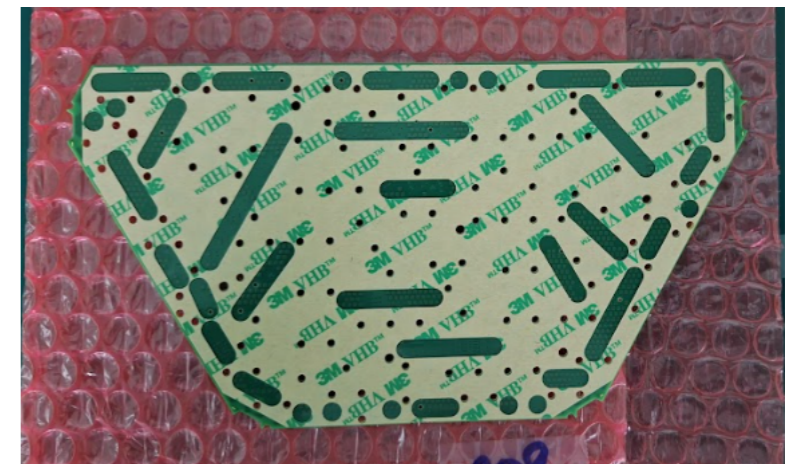
# Module assembly method

- \* Module assembly method combines Araldite and double sided tapes methods to be the hybrid one with the glue patten matching to the tape' hollow.
- Araldite : High radiation tolerance but inefficiency (1 day).
- Double sided tapes : High efficiency (20 mins) but low radiation tolerance.
- \* The dedicated transfer tapes are made by our laser cutting machine with an efficiency of 3 min/per piece

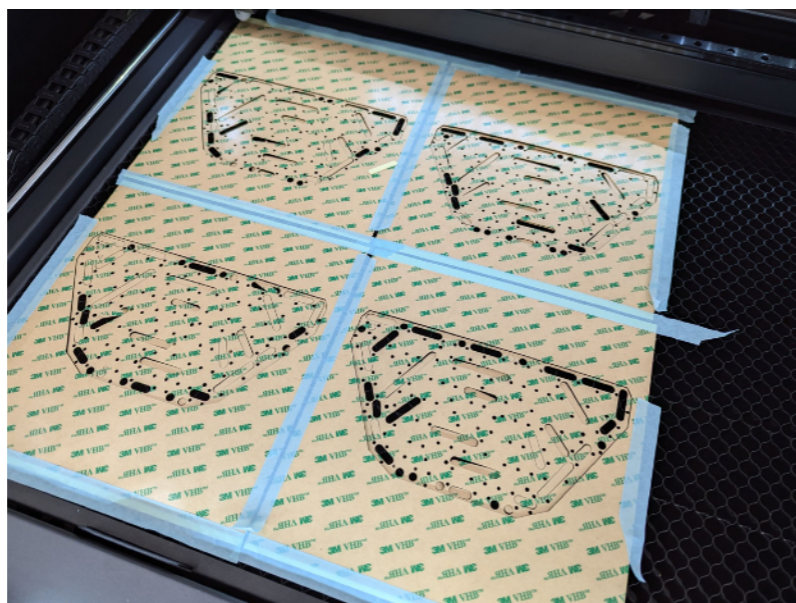
Araldite



Double sided tape



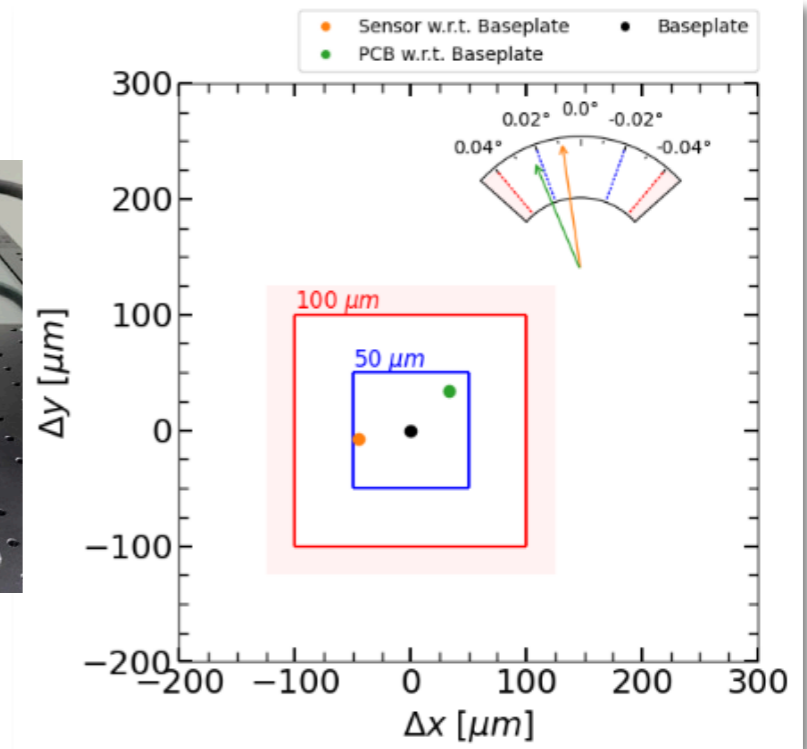
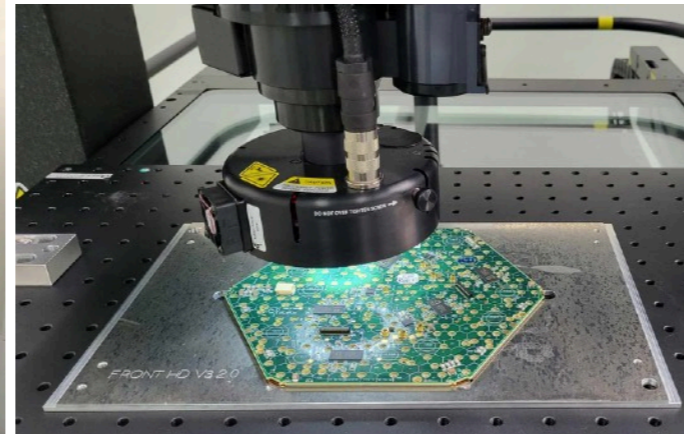
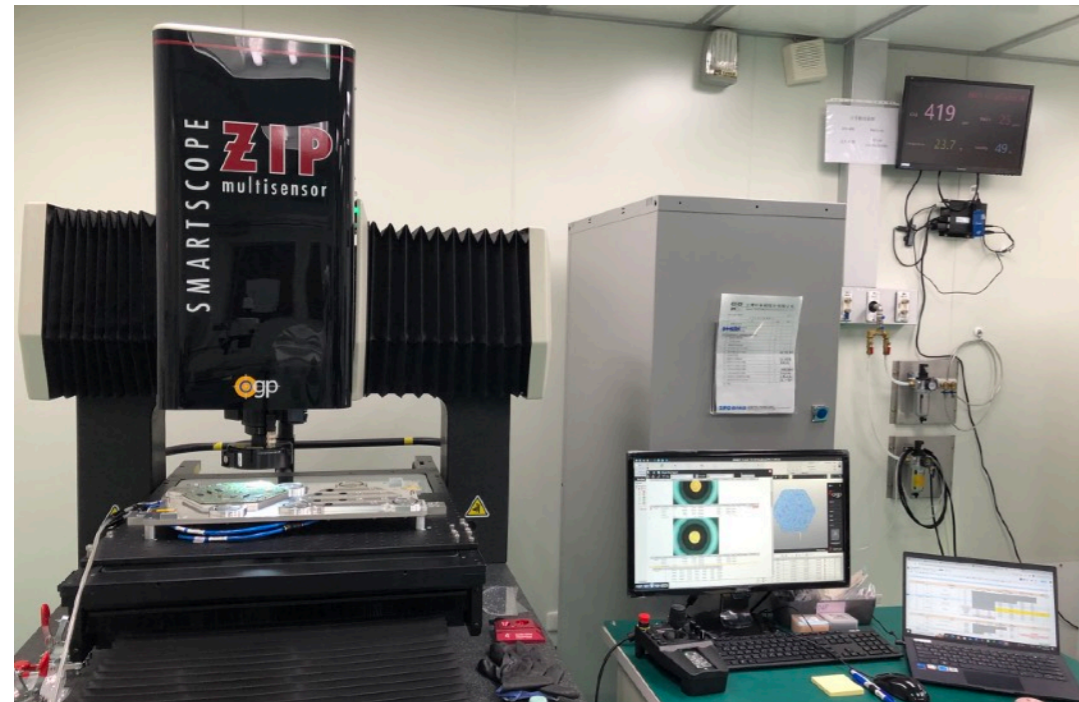
Laser cutting





# QGP QC

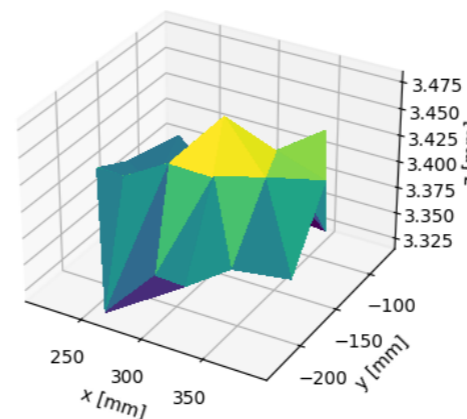
## Alignment



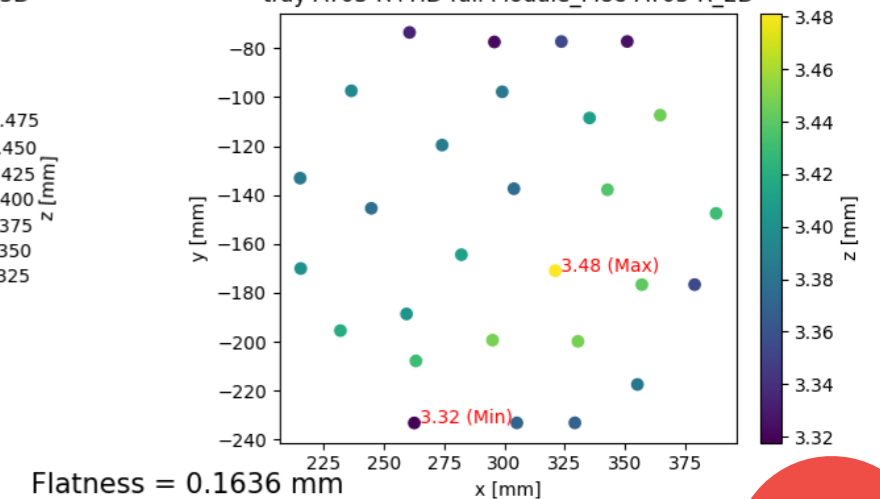
- \* OGP provides optical high-precision ( $\sim\mu\text{m}$ ) locating and image processing for modules to measure modules' quality indicators.
- \* Alignment information such as offset between baseplate/sensor/HB and flatness.
- \* Measurement result visualization by python.

## Flatness

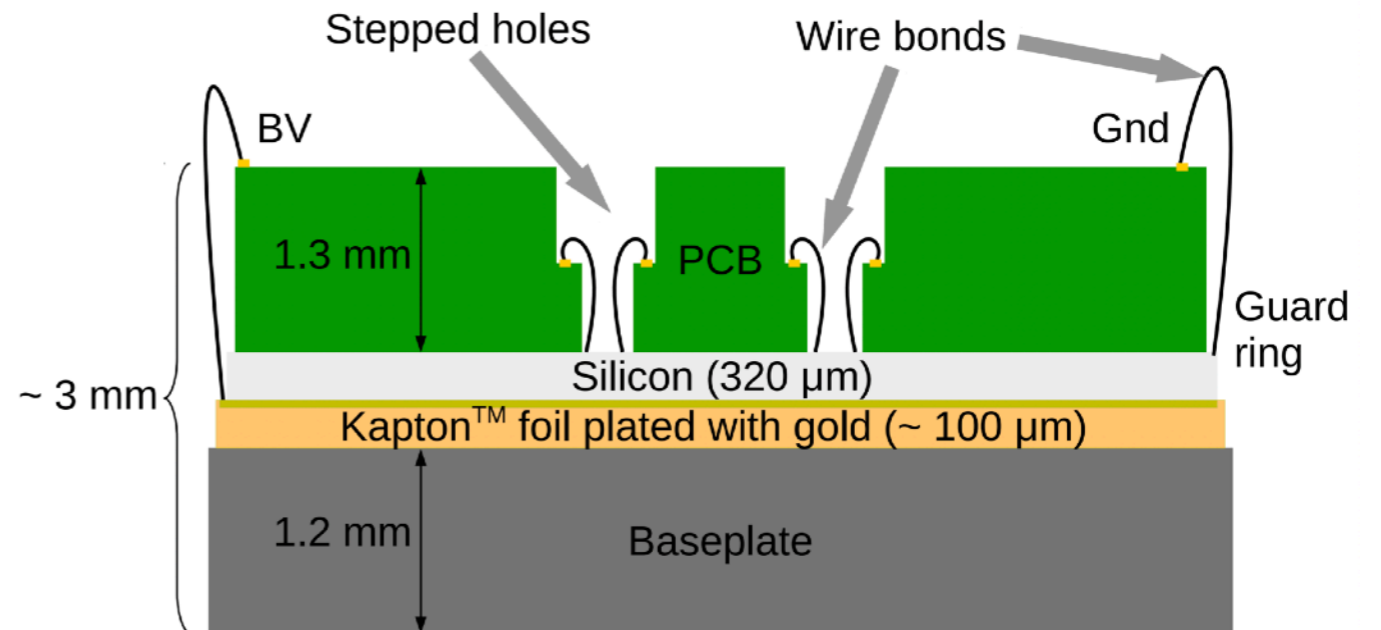
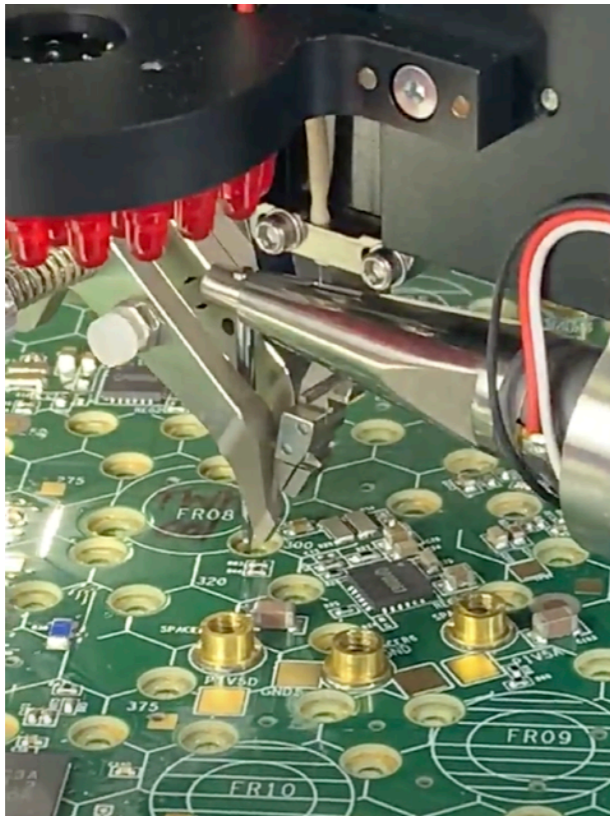
ray-AT03-R+HD full Module\_M88-AT03-R\_3D



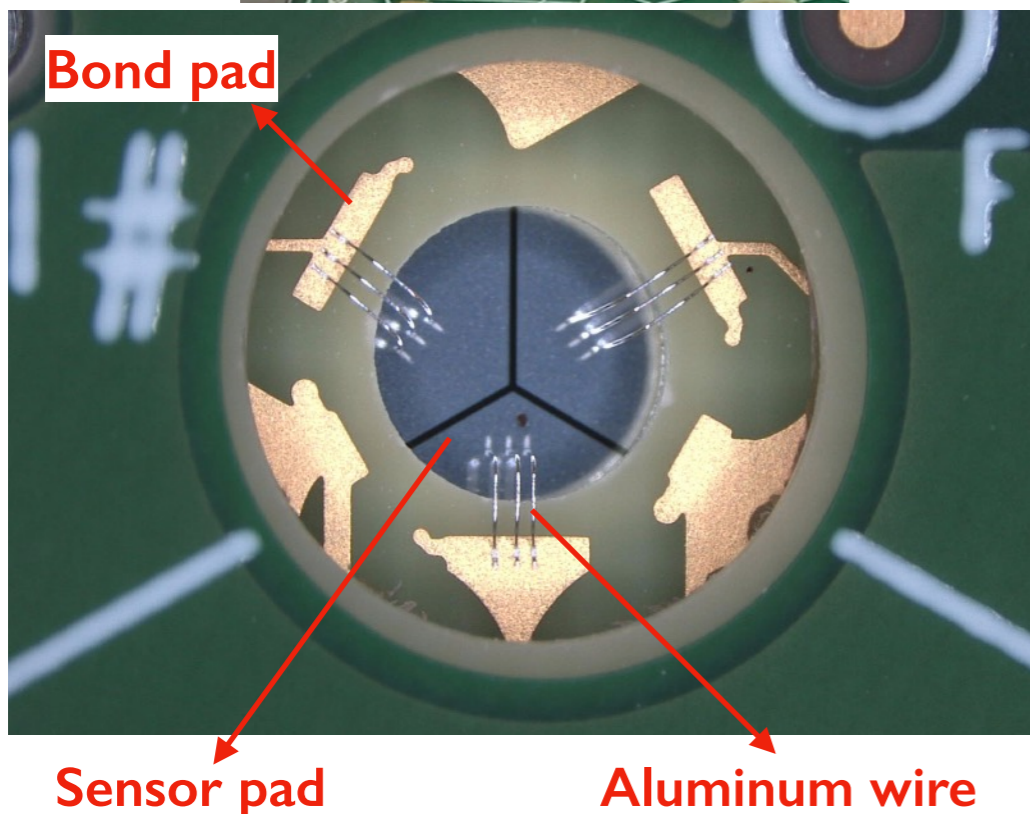
tray-AT03-R+HD full Module\_M88-AT03-R\_2D



# Wire bonding

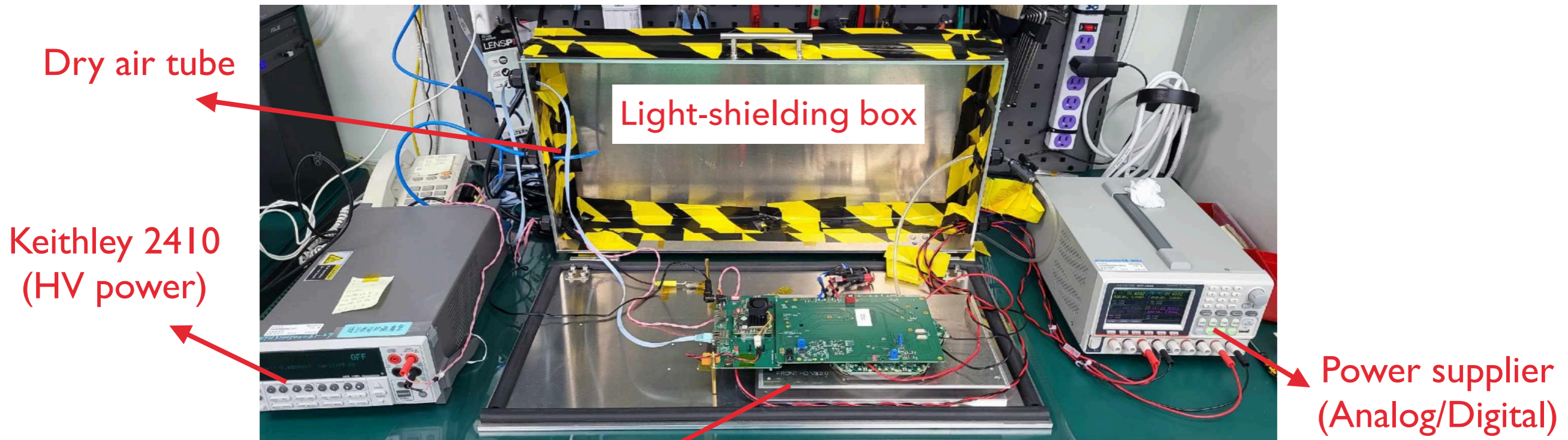


- \* Connect the silicon sensor to pads on the hexaboard through aluminum wire for signal readout and HV/GND.
- \* 15 mins can finish a module with 432 bond pads.
- \* Use OGP to snapshot bond pads and sensor to check the failure of wire bonding.
- \* Consider vision recognition (machine learning by ourselves) to identify the failure of wire bonding in future.

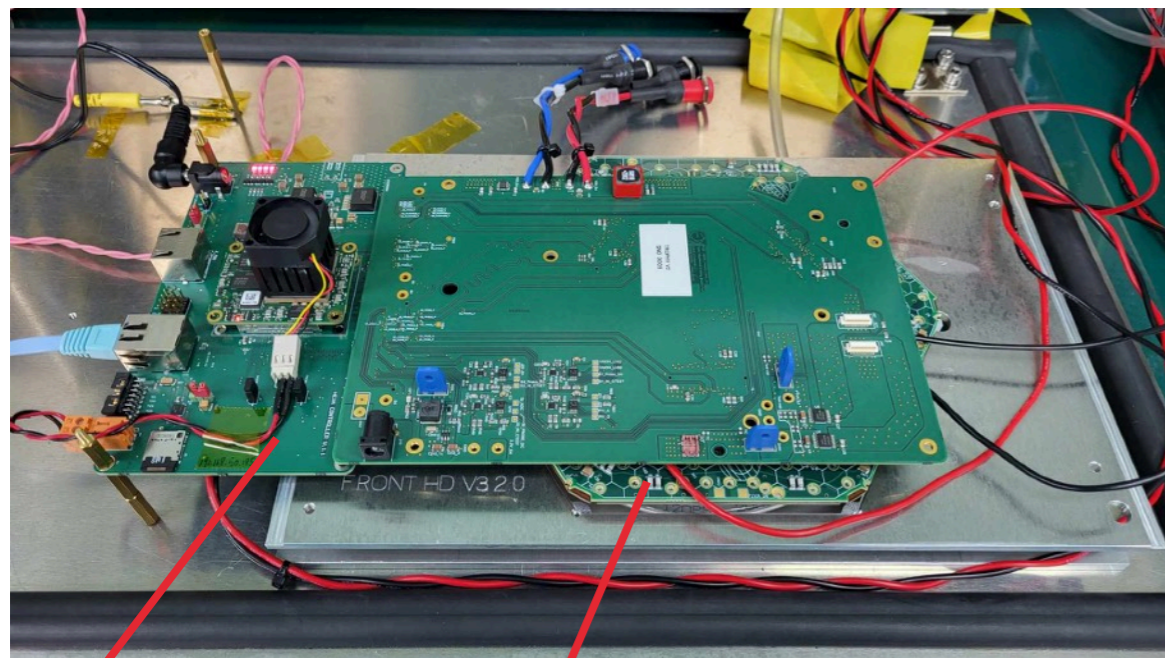




# Electronic test setup



## Teststand



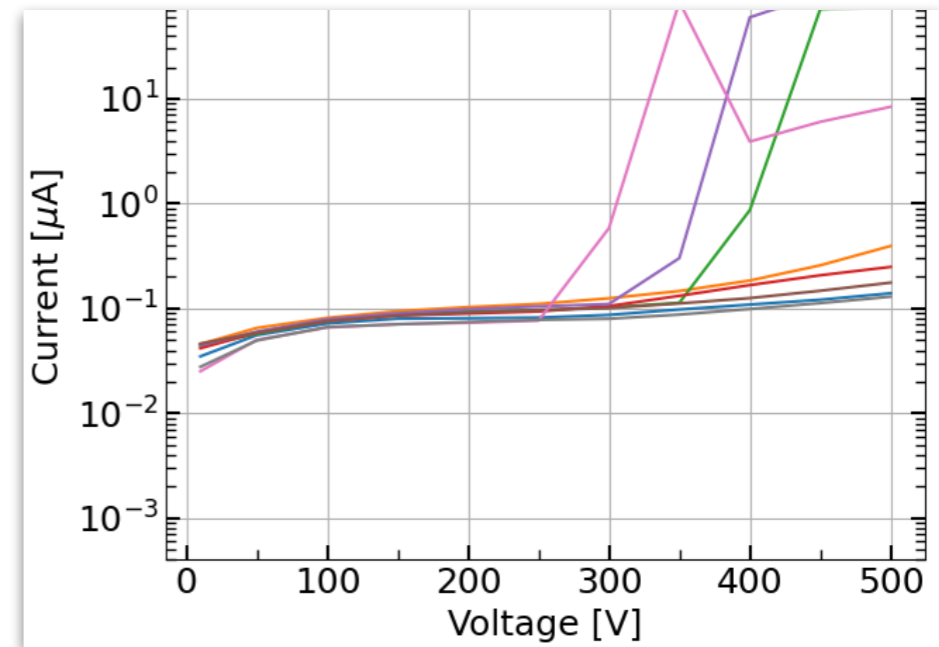
- \* HV (up to 300 V) as bias voltage is applied to tested module to achieve full depletion.
- \* The test stand is placed in the light-shielding box with injected dry air to avoid high leakage current; vacuum system is applied to hold the module position for stability.
- \* Hexacontroller controls DAQ and HGCROC through i2c.
- \* Python module controls HV power supplier.



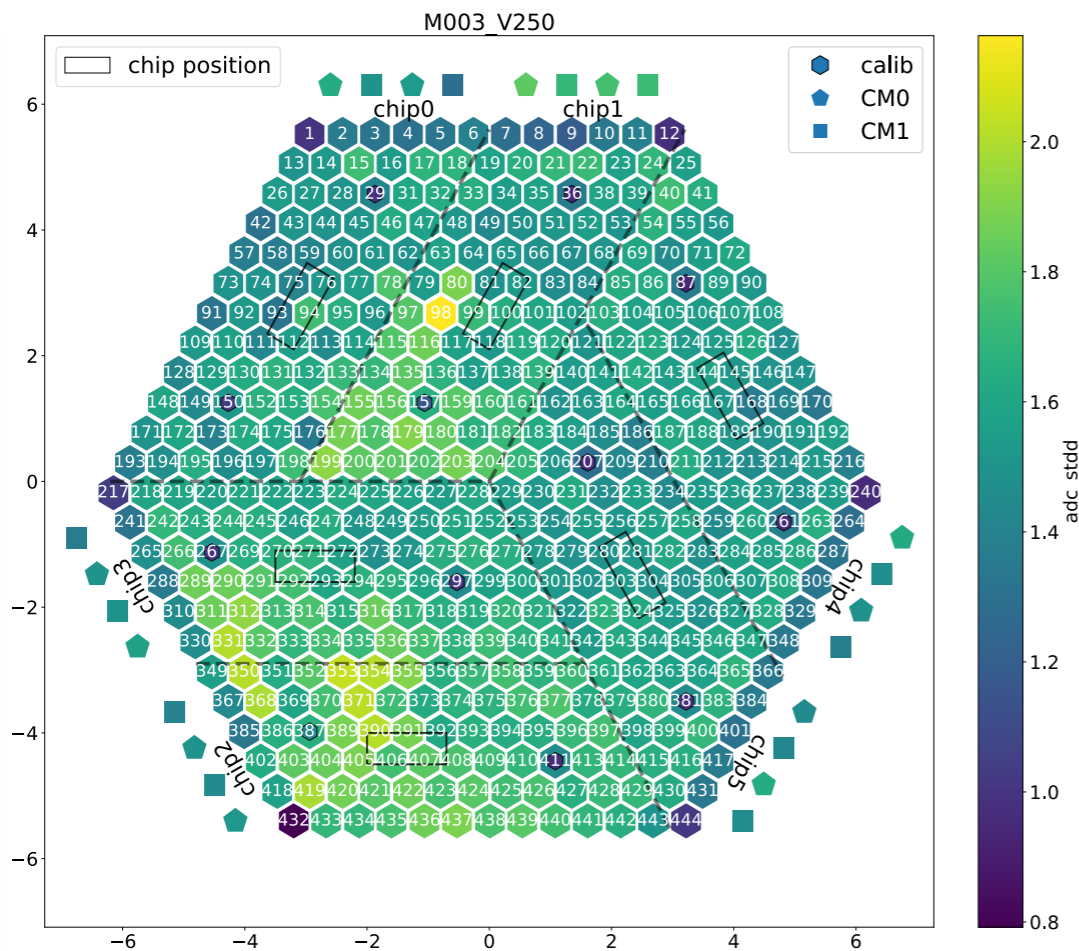
# Electronic functionality

- \* IV curve checks damage of sensor after assembly.
- \* Noise mapping provides quality of HGCRROC, PCB design and wire bonding.
- \* Phase scan test gives pedestal stability (16 phase = 25 ns)

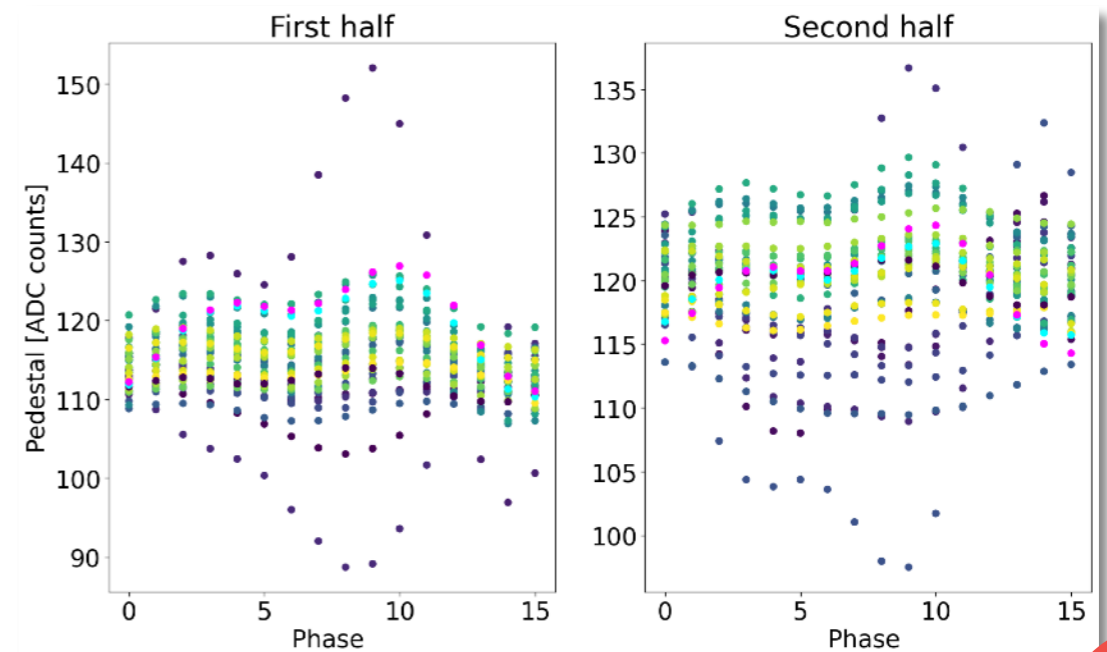
IV curve



Noise mapping



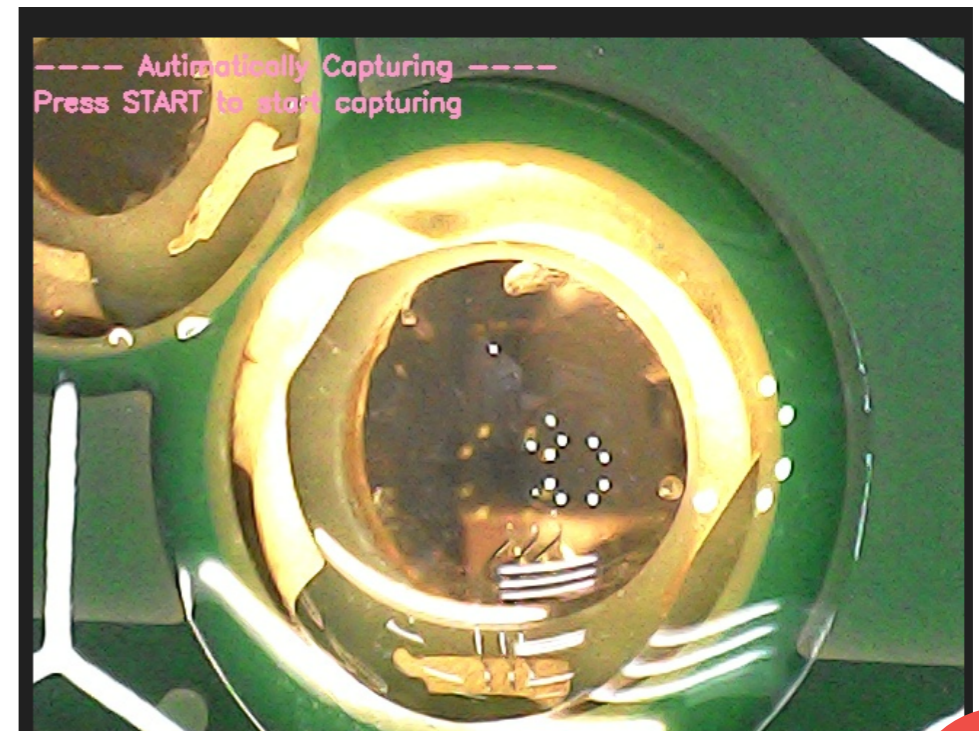
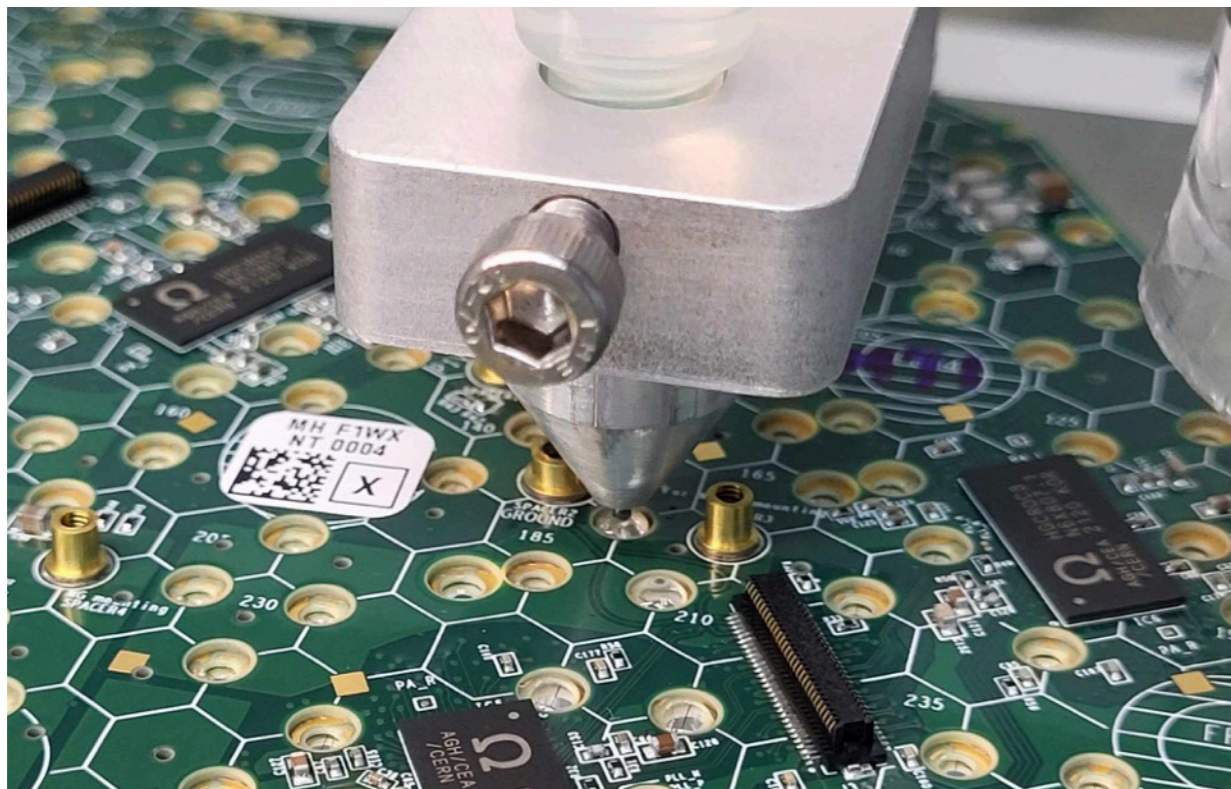
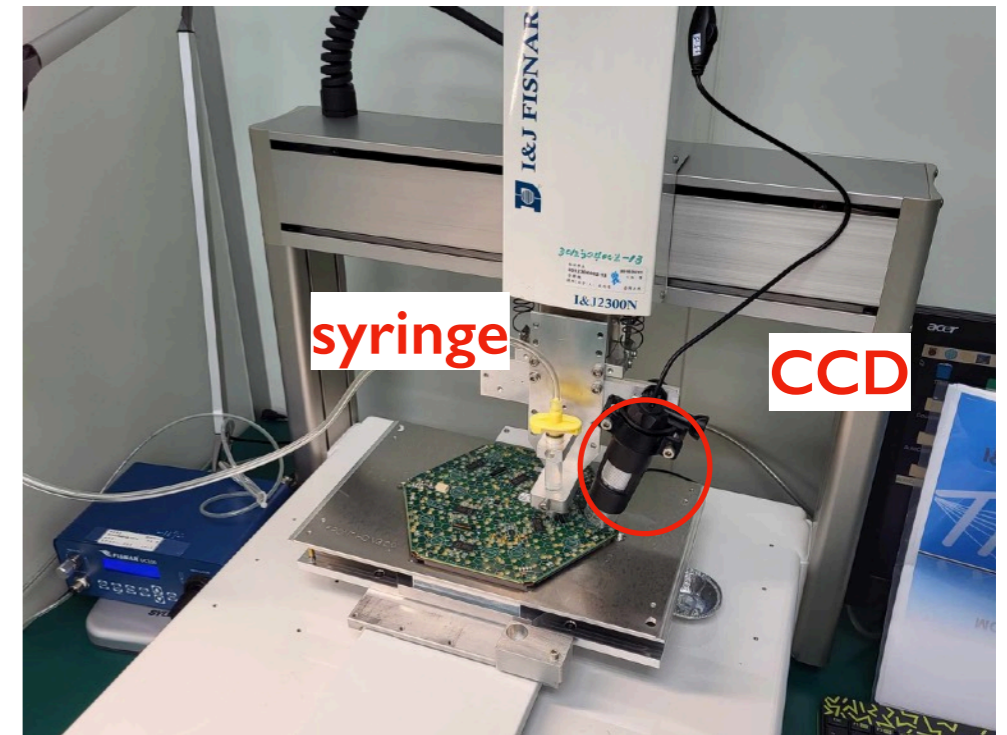
Phase scan



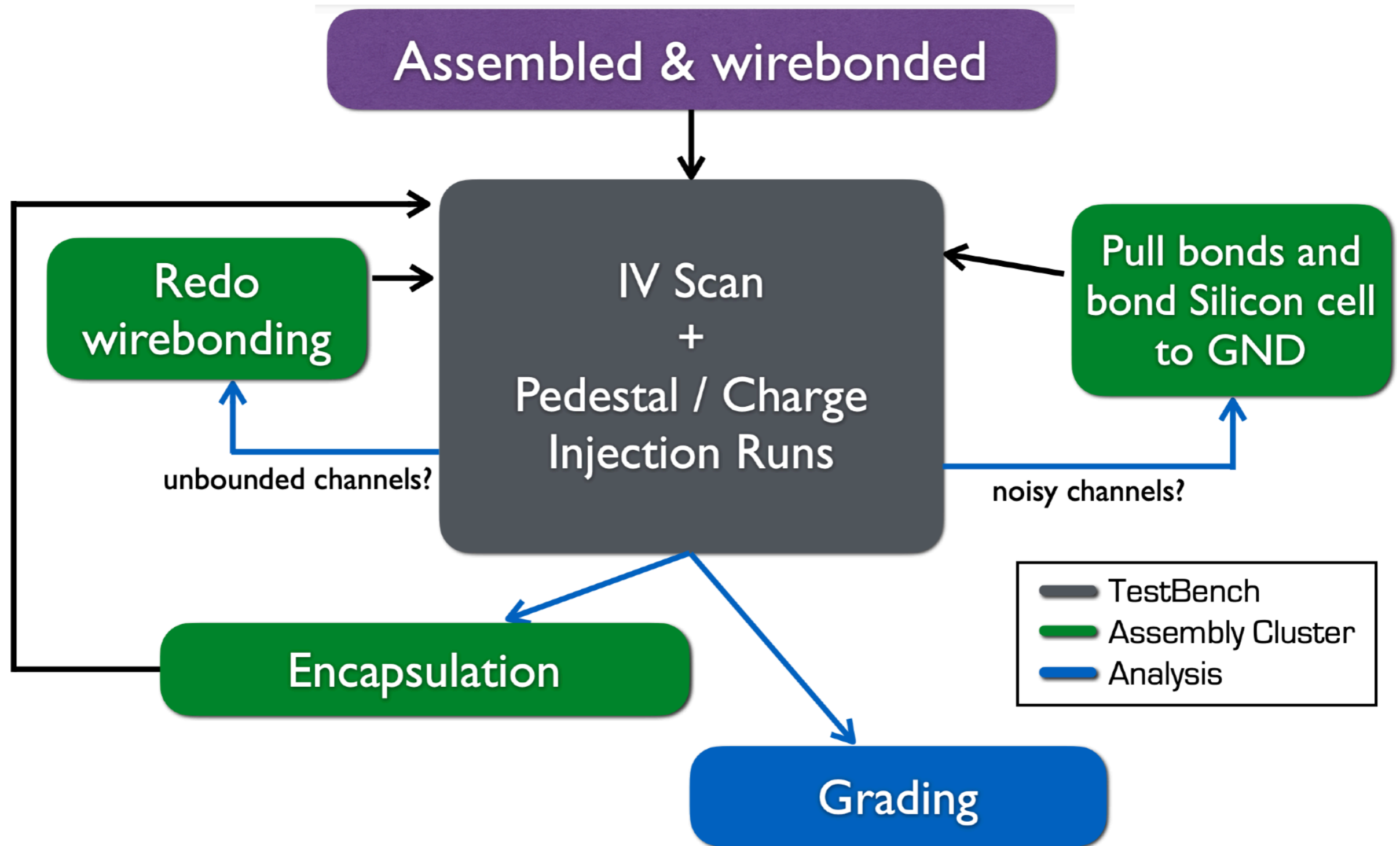


# Encapsulation

- \* Wire encapsulation is performed using glue coverage to avoid dust to touch wires and cause short.
- \* Programmable miniGantry and air jets are automatically controlled for syringe position and the timing of glue squeezing.
- \* CCD camera scans all step holes to check the status of like bubble or glue overflow.



# Electronic functionality



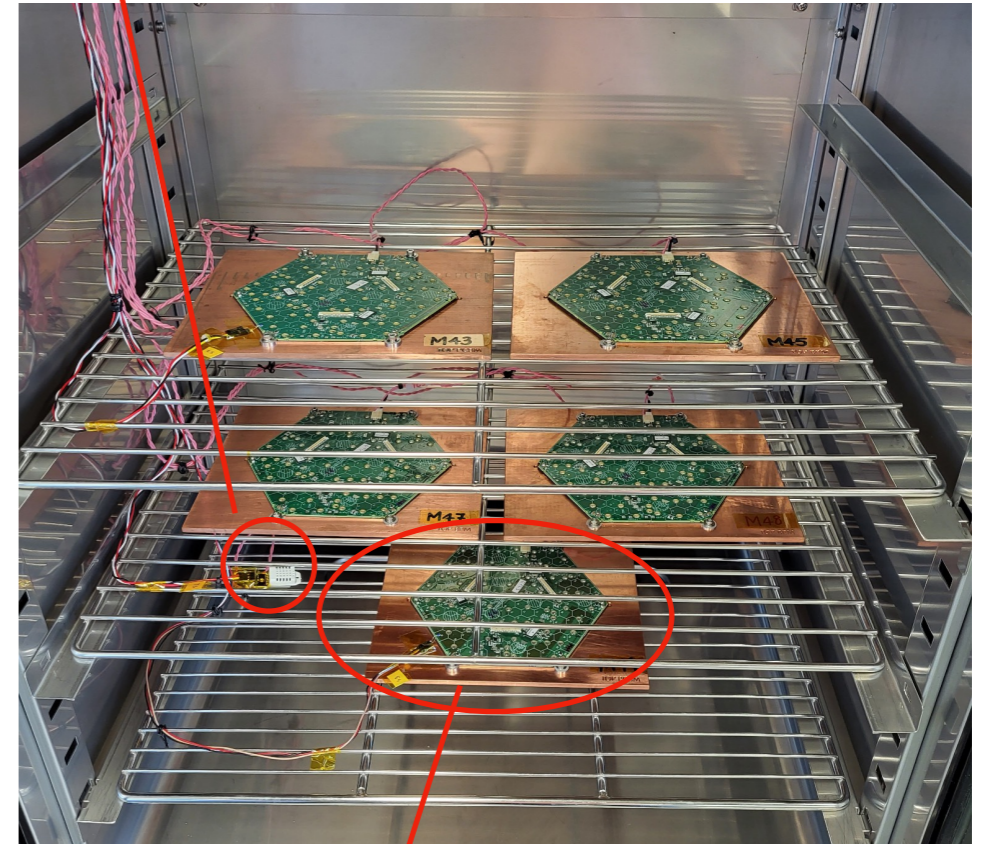


# Thermal cycle test setup

- \* Test of module structure damage or electronic functionality glitch during temperature raising/lowering.
- \* Tested modules mounted on copper plates to simulate modules on cooling plates through dedicated screws.
- \* HV cables are also extended into the chamber to test IV curve.

Temperature/Humidity sensor

Inside the chamber



Mmodule mounted on copper plate

Overview



Keithley 2410

HV wires

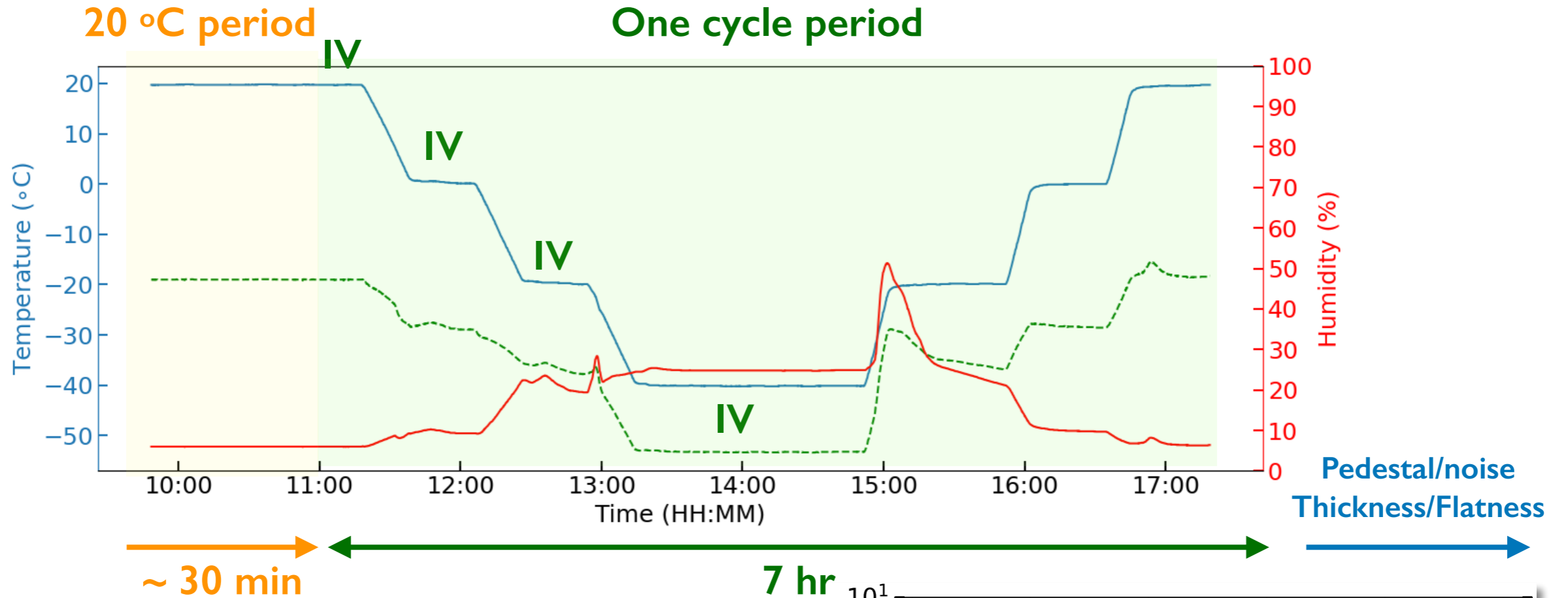
Raspberry Pi

Macbook

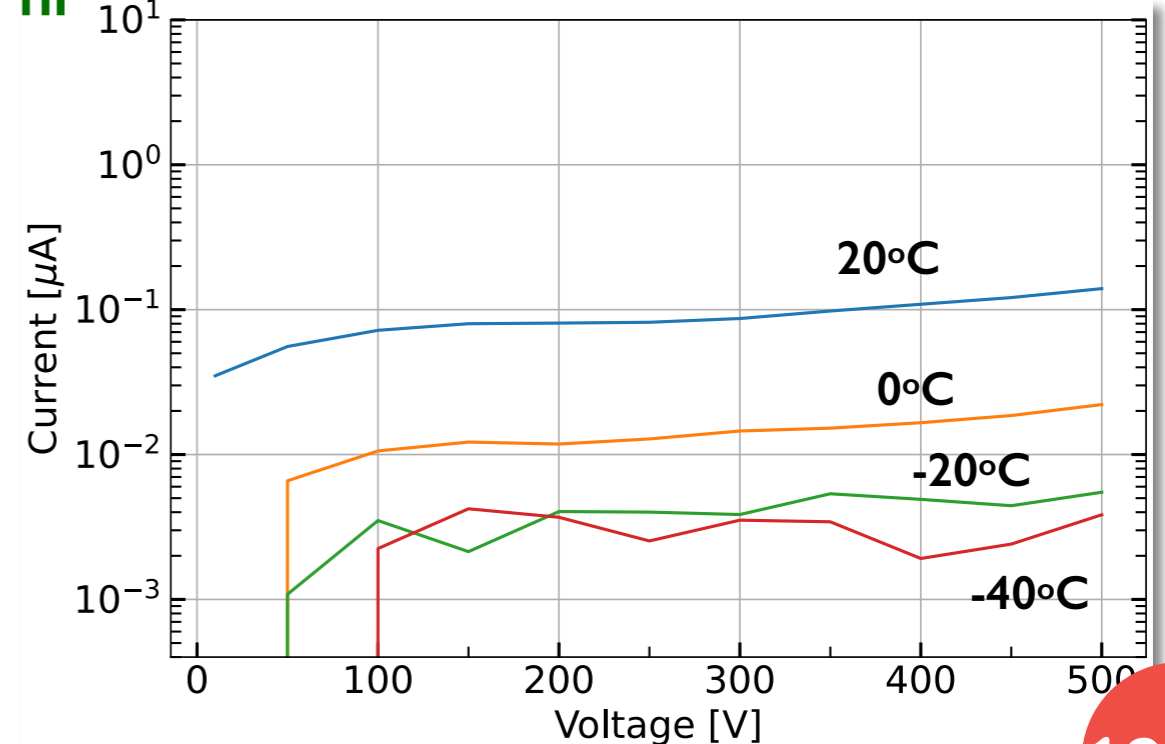
HITACHI chamber



# Thermal cycle test



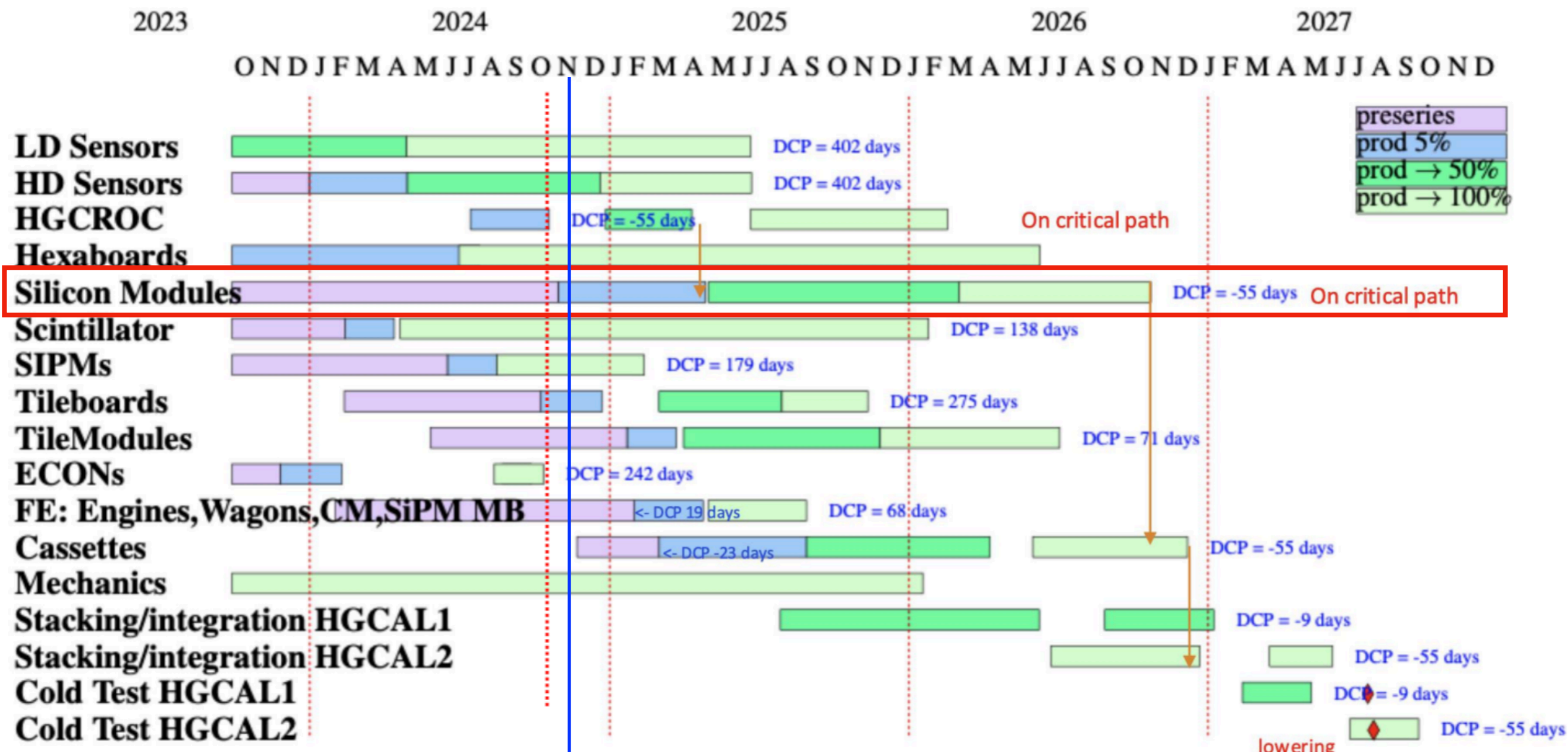
- \* Temperature range of -40 ~ 20°C at least 10 cycles.
- \* IV curve is measured during thermal cycle.
- \* OGP QC and electronic functionality test is redone after thermal cycle.
- \* Humidity inside the chamber needs to be taken care to avoid water droplets on modules.





# Schedule

## HGCAL schematic schedule V30 October 2024



We are here



# Production Ramp-up

October 2024

S M T W T F S

Expect to receive 45 to 50 hexaboards early November (CMU, IHEP, TTU) ...UCSB, NTU HD/partials not shown

November

S M T W T F S

Build 16 modules November

Practice "mini ramp up" with one tray

December

S M T W T F S

1 2 3  
8 9 10  
15 16 17  
22 23 24  
29 30 31  
5 6 7

Build 32 modules December/January

Practice with 1 tray in 2<sup>nd</sup> region on gantry, 2 trays if possible

January 2025

S M T W T F S

29 30 31  
1 2 3 4  
8 9 10 11  
15 16 17 18  
22 23 24 25  
30 31 1  
6 7 8

Ideal: "mini ramp up" with two trays

February 2025

S M T W T F S

Cycles of 2 weeks on within a month  
Build 4 per day x 2 weeks

2 3 4 5 6 7 8

March

S M T W T F S

Build 8 per day x 2 weeks

23 24 25 26 27 28 1

30 31 1 2 3 4 5

April

S M T W T F S

Build 12 per day x 2 weeks

30 31 1 2 3 4 5

27 28 29 30 1 2 3

4 5

May

S M T W T F S

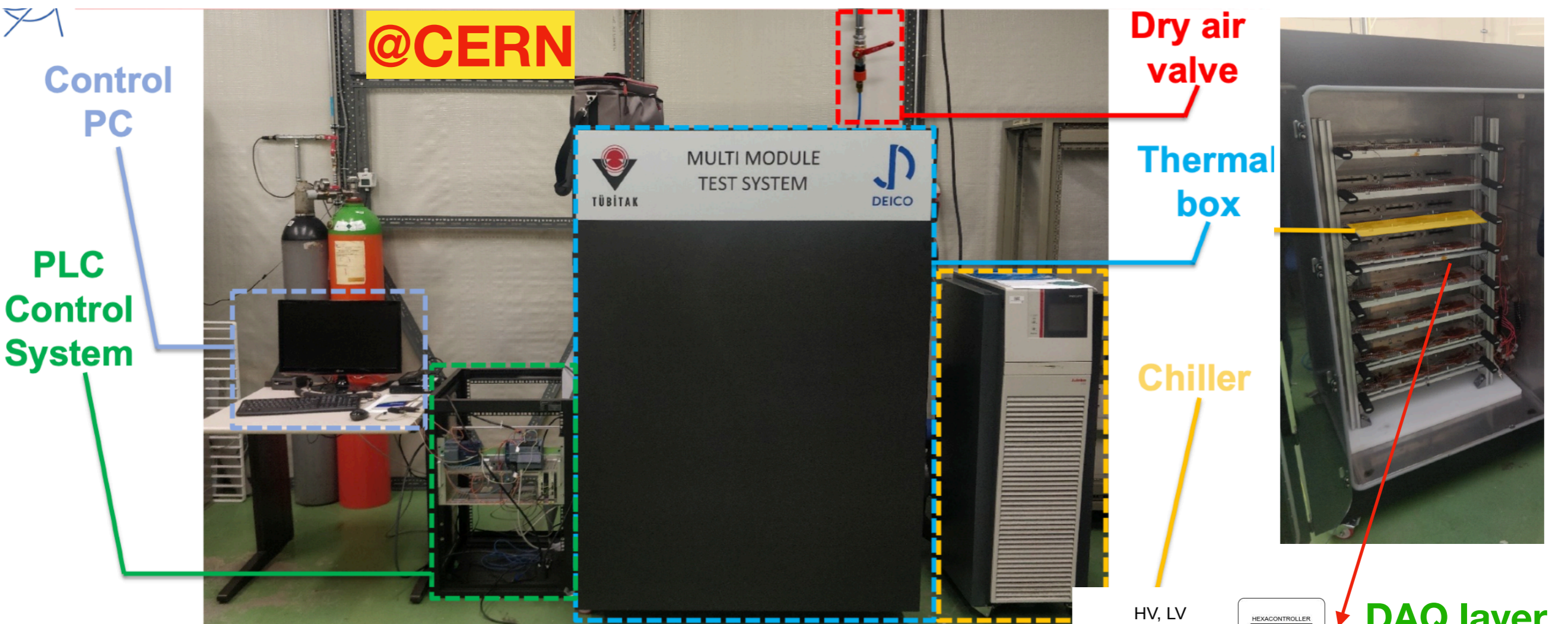
Build 16/day x 2 weeks

27 28 29 30 1 2 3

Reaching 16/MAC-day Spring 2025



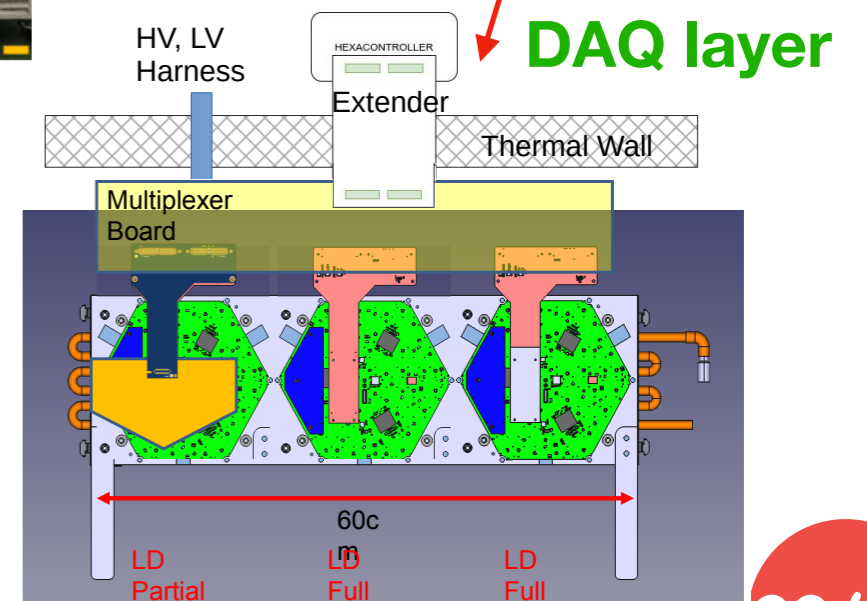
# Multi-Module test system



Multi Module Test System for Silicon Modules

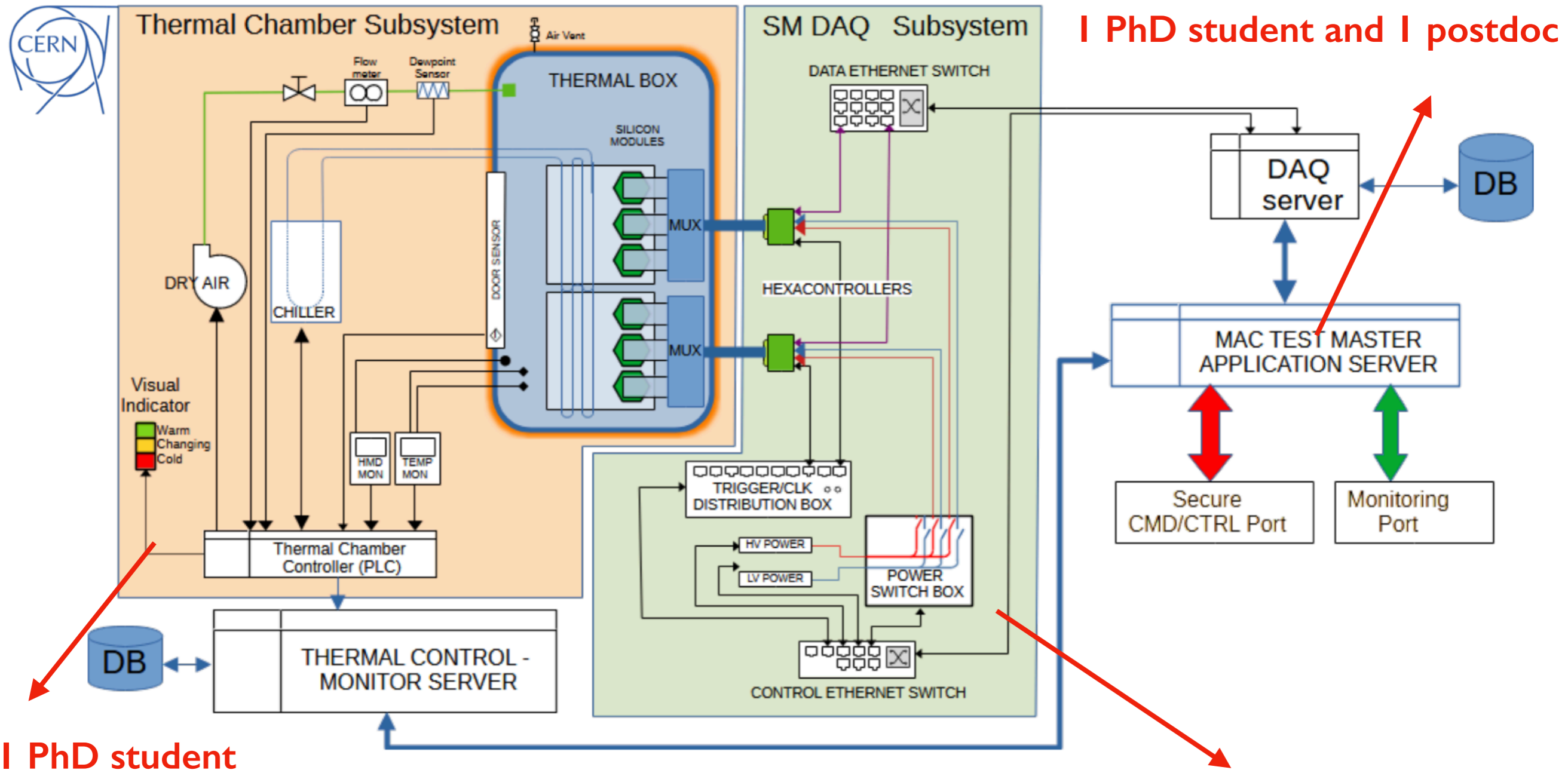
Build a multi-mode test system that synchronizes electronic test, IV measurement and thermal cycle together.

- \* DAQ system, Power supplier (normal and HV), ColdBox, Chiller, Dryair system, PLC.
- \* There can be 24 hexaboards within the coldbox and 3 hexaboards for data taking at the same time





# Multi-Module test system



I PhD student and I postdoc

I PhD student

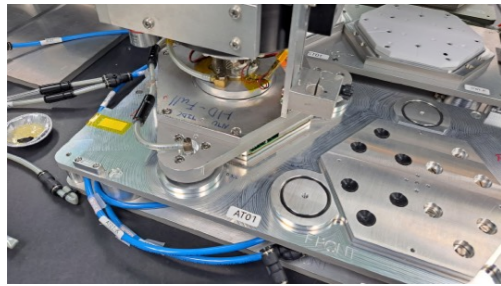
I postdoc

Multi Module Test System for Silicon Modules

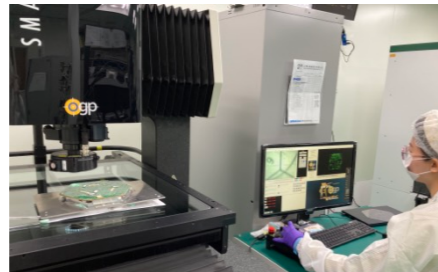


# GUI and Database

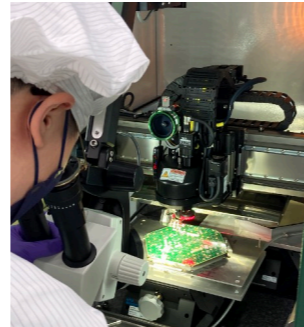
Assembly



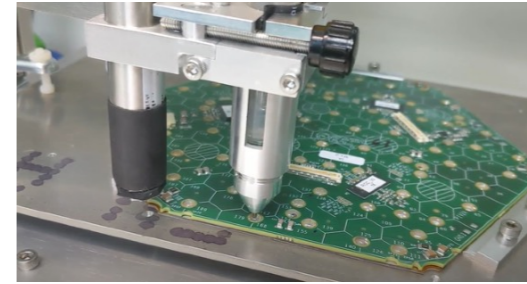
OGP QC



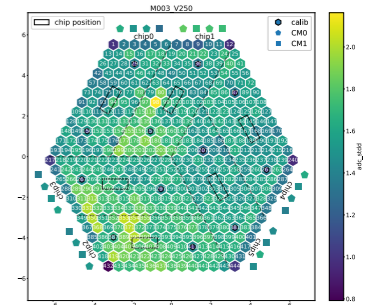
Wire bonding



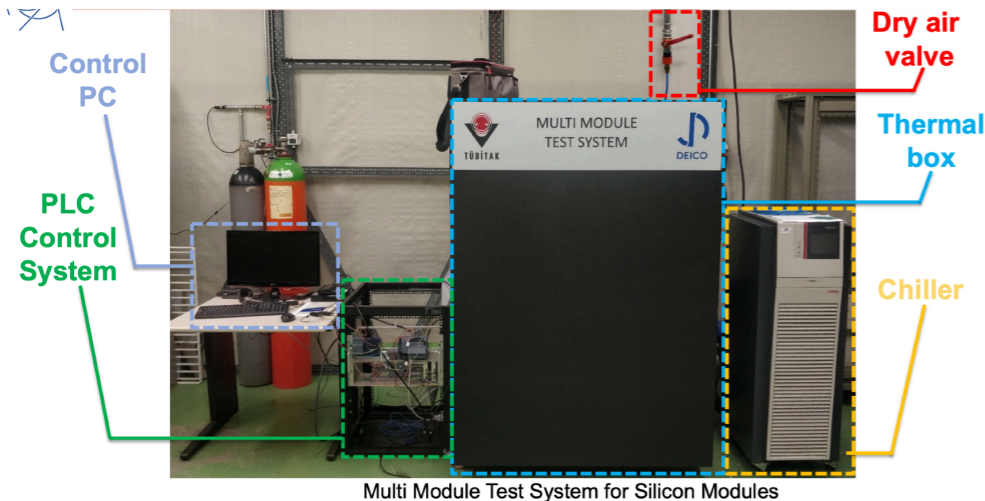
Encapsulation



Electronic test



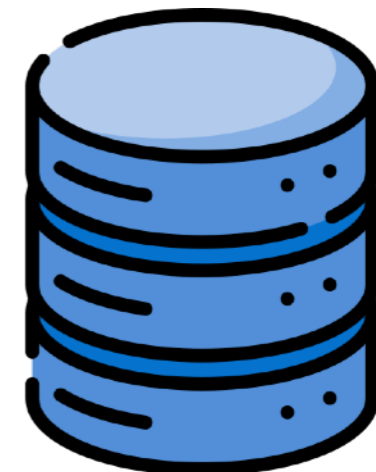
MMTS



Multi Module Test System for Silicon Modules



Local DB



CERN DB



# Summary

- \* Overall procedure from materials to modules in Taiwan MAC gradually becomes mature.
- \* Some important steps like multi-mode test stand and GUI is still under development.
- \* It's expected that the Taiwan HGICAL MAC will transform into production stage.