Operational Experience and Performance with the ATLAS Pixel detector at the Large Hadron Collider at CERN

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HSTD 14 - 17.11.2025

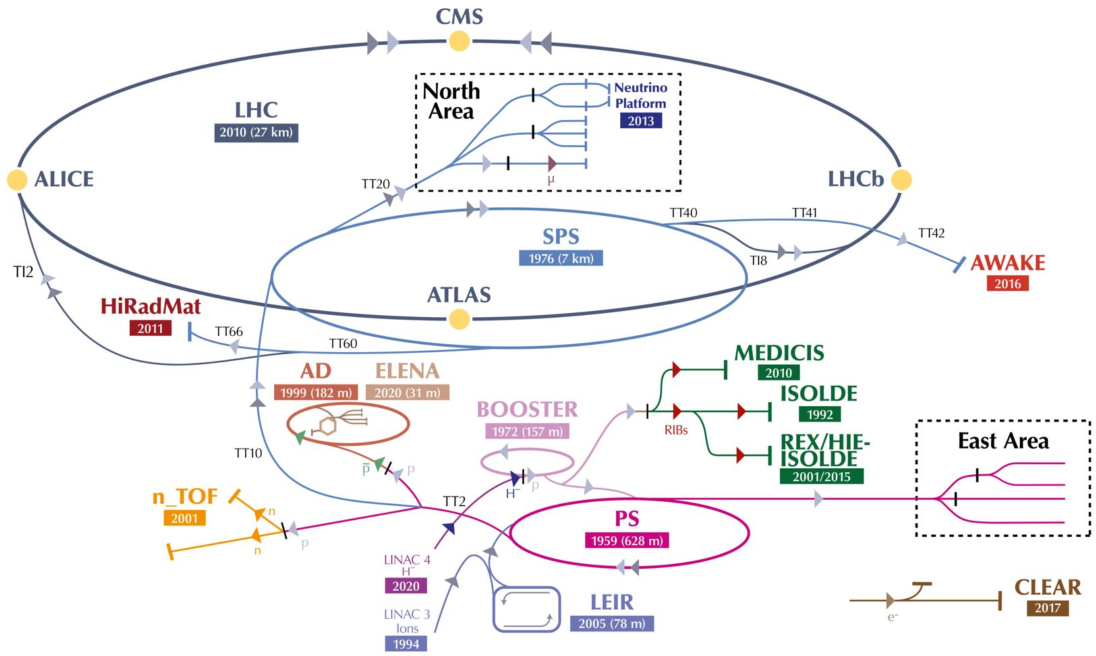
technische universität dortmund

ATLAS EXPERIMENT

FSP ATLAS

Gefördert durch:
Bundesministerium für Forschung, Technologie und Raumfahrt

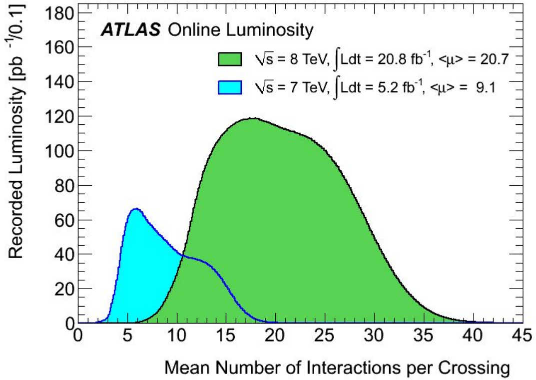
The LHC



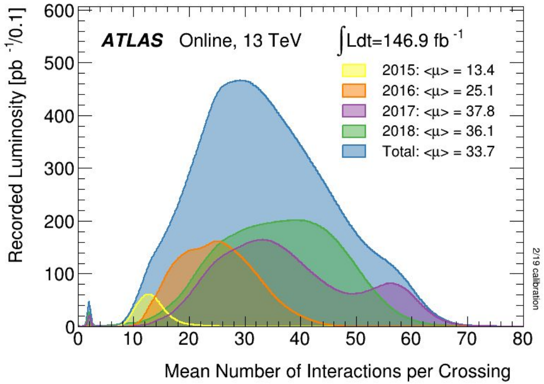
- The Large Hadron Collider at CERN
- Largest and most energetic hadron collider
- Nominal proton-proton collisions, but also heavy ion operation
- Operating at a centre of mass energy of 13.6 TeV
- Bunch structure with 25 ns spacing
- Houses several large (multi-purpose) experiments: ALICE, **ATLAS**, CMS, LHCb

LHC & Luminosity

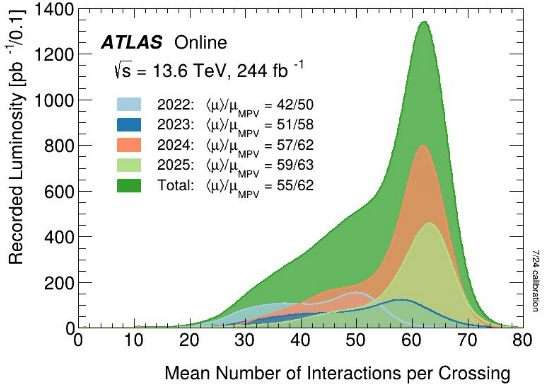
Run 1: del. 5.5/22.8 fb^{-1} and rec. 5.2/21.3 fb^{-1}



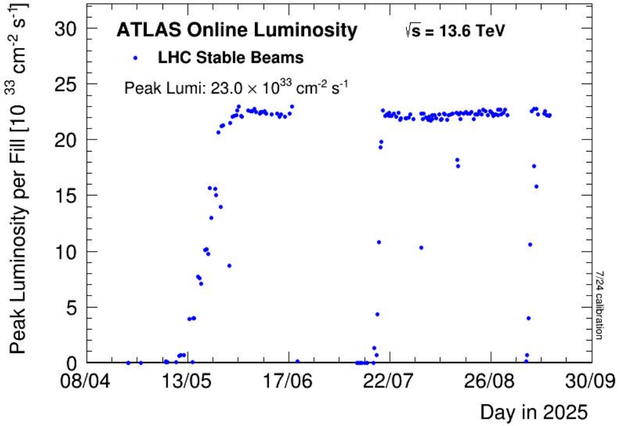
Run 2: del. 156 fb^{-1} and rec. 147 fb^{-1}



Run 3: del. 264 fb^{-1} and rec. 249 fb^{-1}

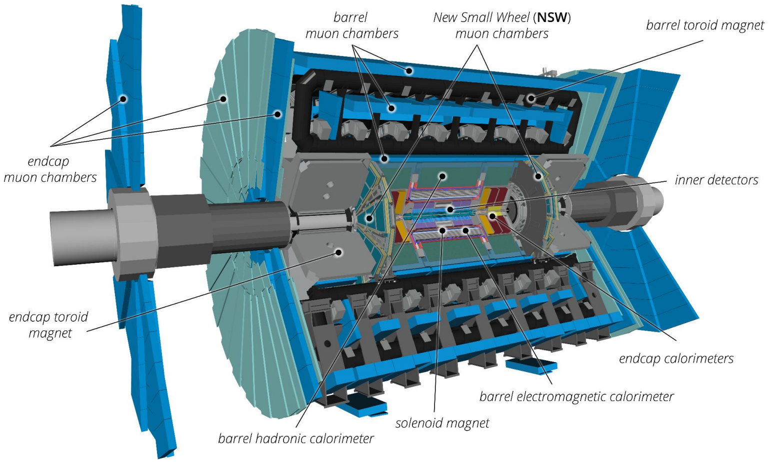


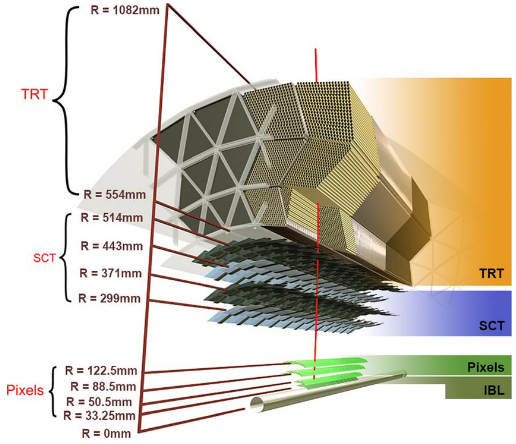
- LHC Peak Luminosity [cm^{-2}sec^{-1}]
  - TDR: 1x10^{34}
  - Today: **2.3x10^{34}**
- LHC <μ>
  - TDR: ~ 20ish
  - Today: **64** (while levelling)
- In addition: long levelling periods with a very good control of pile-up (μ)



The ATLAS Detector

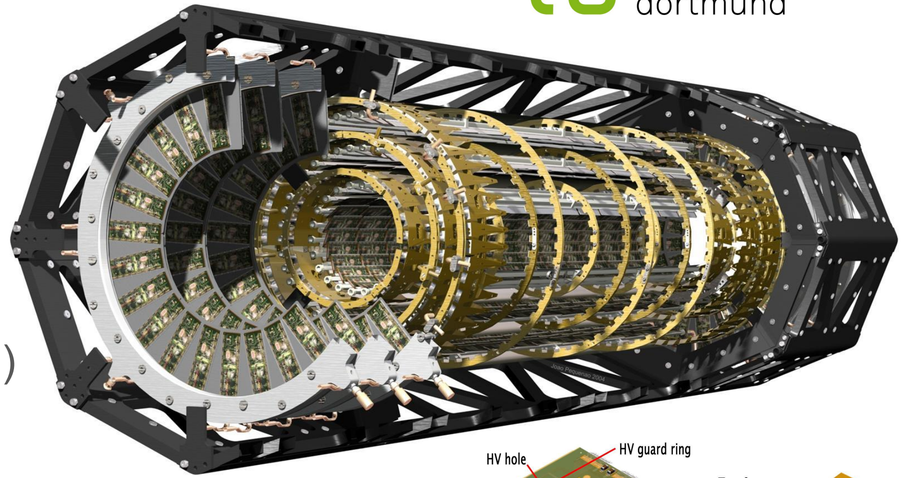
- Typical HEP detector with muon systems, calorimeters and tracking and vertexing detectors
- The ATLAS Inner Detector constituted of transition radiation tracker (TRT), silicon strip modules (SCT), and pixels (IBL+PIX)
- Innermost layers are pixellated silicon detector → ATLAS Pixel and IBL detector
- Collisions in ATLAS since 2009



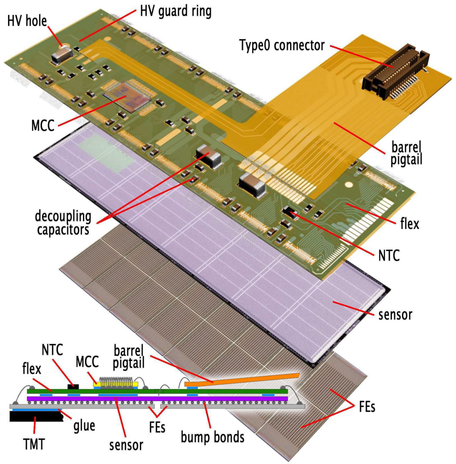


The Pixel Detector

- The ATLAS Pixel detector
  - 1.7 m^2 of silicon
  - 80 million channels
  - Three barrel layers (5 cm to 12 cm) and three disks on each side
  - $|\eta|$ coverage up to 2.5
  - C_3F_8 evaporative cooling
  - Innermost barrel layer: **B-Layer**
- Pixel modules
  - Planar n-in-n sensors with 400 μm x 50 μm pixellated matrix
  - 250 nm CMOS read-out chip
  - Radiation hard up to $1\times10^{15}\ n_{eq}cm^{-2}$

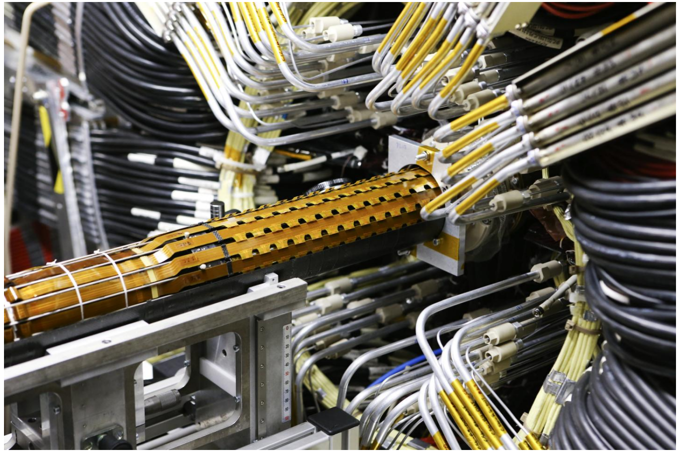


In ATLAS since the start of operation in 2009 and designed for a <μ> of 23!

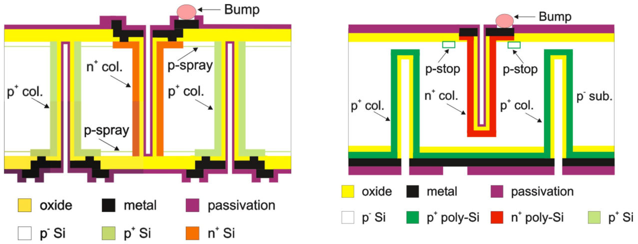


The IBL Detector

- The IBL detector (“*insertable B-Layer*”)
  - 0.2 m^2 of silicon
  - 12 million channels
  - Single layer at 3.3 cm radius
  - CO_2 evaporative cooling
- IBL modules
  - Mostly planar n-in-n sensors with 250 μm x 50 μm pixels
  - n-in-p 3D sensors in forward region
  - Read-out chip in 130 nm CMOS
  - Radiation hard up to $5\times10^{15}\ n_{eq}cm^{-2}$



Installed for operation from 2015 onwards!

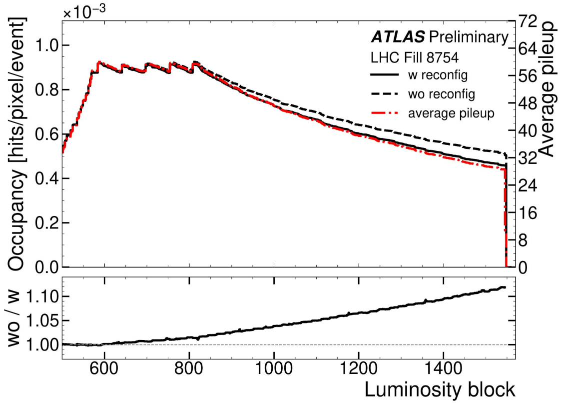


IBL 3D sensor designs (different vendors)

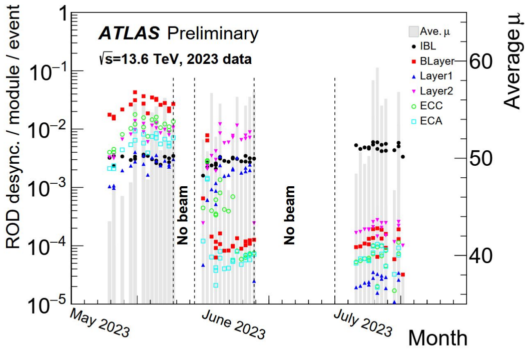
Publication on Production and Integration: [2018 *JINST* **13** T05008]

Operations in Run 3

- High <μ> and long periods of LHC levelling make Run 3 conditions very challenging
- Work on the system to improve stability and resilience due to high hit rate and radiation
- E.g. mitigation of single-event-upsets in the read-out chips
    - SEU will cause misconfiguration of chip
    - Dead-time free reconfiguration of read-out chips
- Or reduction of desynchronisation with the help of a novel read-out firmware
    - Reduction of desynchronisation by orders of magnitude



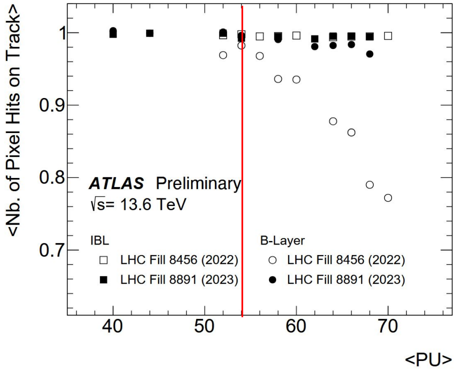
Induced noise due to SEU

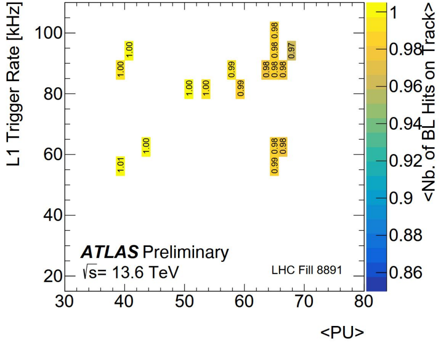


Desynchronisation over time

Operation in Run (2+)3

- Very good performance, especially for a detector in operation since start of LHC
- While the first years in Run 2 were dominated by read-out limitations we are now in the era of radiation damage
- Analogue thresholds given in table

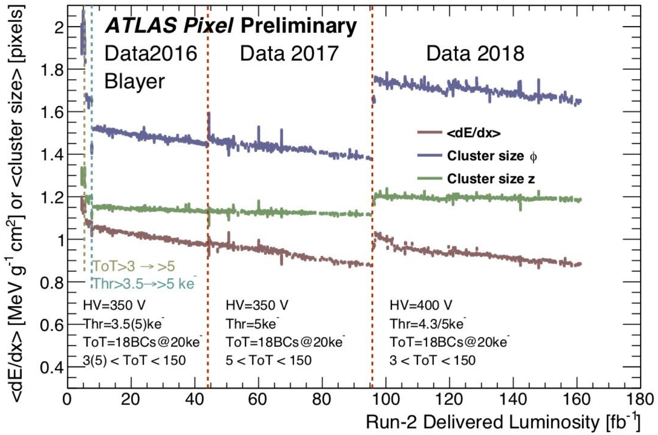




read-out limitations

Layer	2015	2016	2017	2018	2022	2023
IBL	2500	2500	2500	2000	1500	1500
B-Layer	3500	5000	5000	4300*	3500*	4700
Layer 1, 2	3500	3500	3500	3500	3500	4300
Disks	3500	3500	4500	3500	3500	4300

increasing and **decreasing** thresholds



effects of radiation damage: c.f. next slides

Performance in Run 3

mid-2025 numbers

- Working fraction of detector kept high
- Recently issues which require modules to be disabled seem to increase a bit
- However, we are several years and twice the expected dose above our design for the original pixel detector
- Some issues can be mitigated by increase in digital supply voltage, but we are approaching (power) limits there as well
- The IBL detector still in good shape and only single read-out chips with issues
- Performance of individual modules less important than overall data quality
- Data quality efficiency in Run 3 for Pixel was 99.7% or higher

Disabled modules		2018		2024		2025	
		Disabled/Total	[%]	Disabled/Total	[%]	Disabled/Total	[%]
Pixel	B-Layer	18/286	6.2	21/286	7.3	22/286	**7.7**
	Layer 1	29/494	5.8	18/494	3.6	19/494	**3.8**
	Layer 2	33/676	4.8	50/676	7.4	61/676	**9.0**
	Disk	15/288	5.2	16/288	5.2	15/288	**5.2**
	Total	95/1744	5.4	105/1744	6.0	117/1744	**6.7**
IBL (Front End)		3/448	0.7	5/448	1.1	5/448	**1.1**
Total		98/2192	4.5	110/2192	5.0	122/2192	**5.6**

Overall good enabled fraction, but the detector is aging and the situation is getting worse

ATLAS pp Run-3: August 2025 Update

Trigger	Inner Tracker			Calorimeters		Muon Spectrometer					Magnets		Global	
L1+HLT	Pixel	SCT	TRT	LAr	Tile	MDT	RPC	TGC	MM	sTGC	Solenoid	Toroid	Lumi. calib.	Other
99.6	100	99.7	99.9	99.9	100	98.9	99.8	99.9	100	100	100	100	99.5	99.5

Good for physics: 97.0% (40.5 fb^{-1})

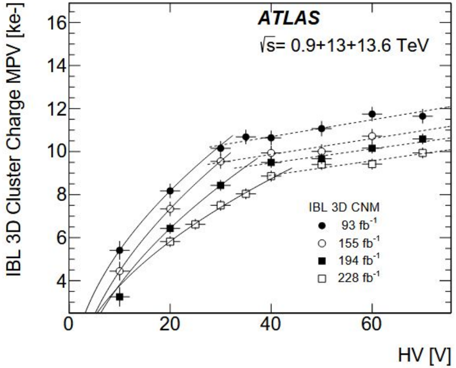
Radiation damage in IBL 3D modules:
[2024 *JINST* **19** P10008]

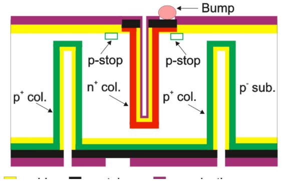
Radiation Damage - Depletion Voltage

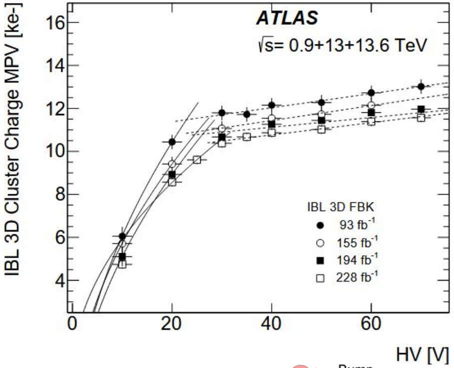
- Radiation to sensor bulk introduced deep defects → change in the effective doping concentration → higher voltage for full depletion
- Regular scans where voltage is stepped through to measure response (IV-curves or collected charge)
- In particular also investigating IBL 3Ds which are of interest for the ATLAS ITk upgrade (innermost ITk layer)

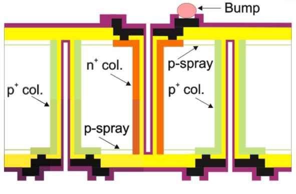
expected/received non-ionising dose in 10^{15} 1 MeV n_{eq} cm^{-2}

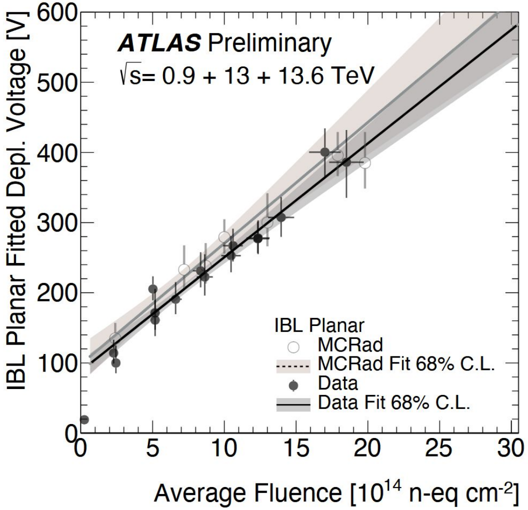
	end of 2025	end of Run 3	design
IBL	3	3.5	5
B-Layer	1.8	2	1





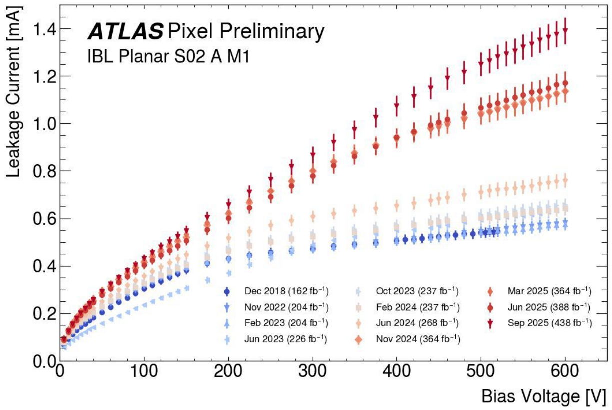


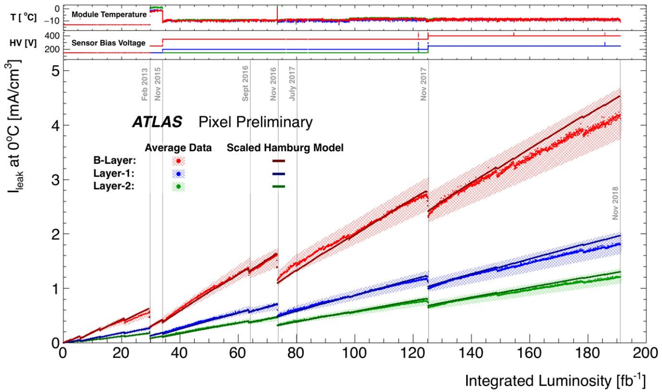




Radiation Damage - Leakage Current

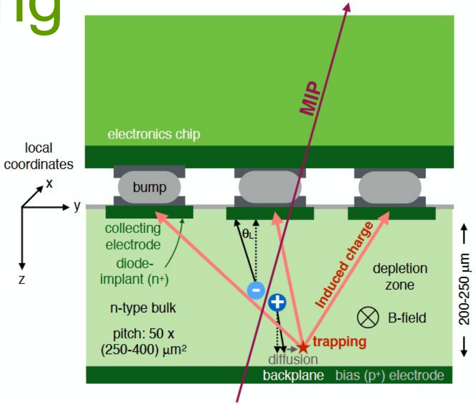
- Aside from depletion voltage, leakage current important to monitor and predict
- Increase in leakage current could hit power supply limit or thermal runaway
- Modules kept at low temperature to prevent annealing
  - Decreasing the temperature would reduce leakage current, but not much headroom in cooling
  - Beneficial annealing would also reduce leakage current, but not foreseen except a few days when cooling maintenance
- Predictions with the Hamburg model, need scaling factors, but overall good prediction
- Leakage current not expected to be an issue even at end of Run 3

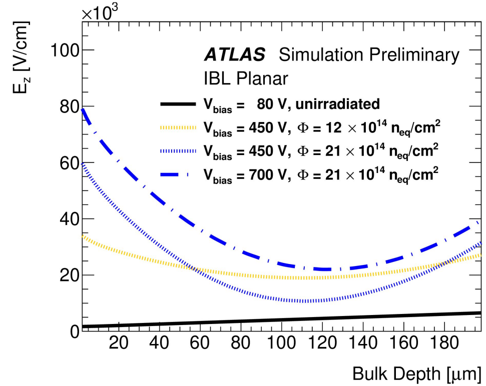


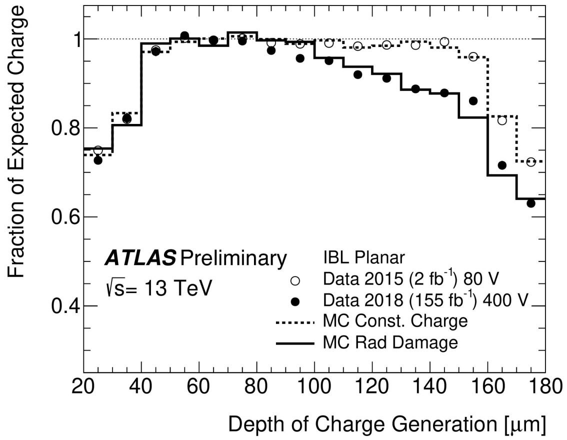


Radiation Damage - Modelling

- As radiation damage becomes more and more dominant - modelling of it is more important
- The radiation damage digitiser has been implemented and is used in ATLAS Monte-Carlo production since Run 3
- Model uses E-fields from TCAD, computed Ramo-potential maps and trapping constants as input
- Publication: [JINST 14 (2019) P06012]

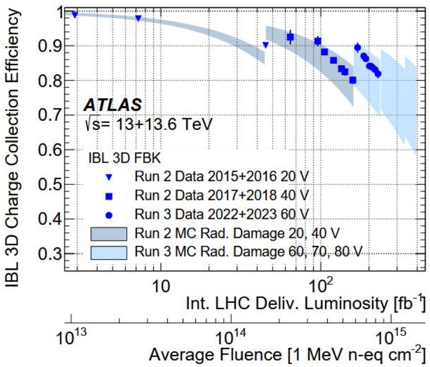


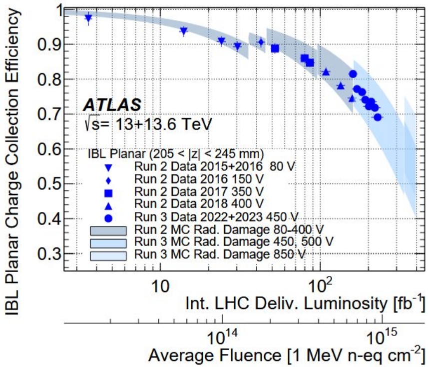


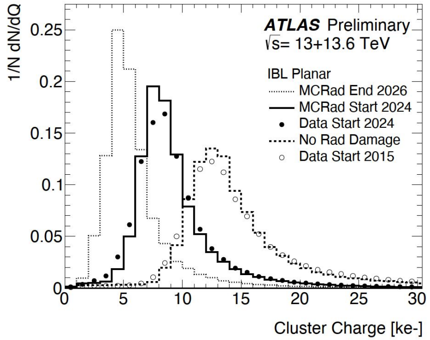


Radiation Damage - Charge Collection Efficiency

- Decrease of charge collection efficiency (CCE) due to trapping because of radiation damage
  - CCE in IBL planar (and B-Layer) will drop to about 30% and only partially recovered by increase in bias voltage
  - IBL 3Ds retain better CCE - shorter charge collection distance and p-type bulk
- However, hit-on-track performance deteriorates significantly less and we only expect a loss of up to 3% hits-on-track due to this
- Closely monitor these effects, we do not anticipate the need to reduce the thresholds: IBL at 1.5 ke threshold, expect 16 ke at 100% CCE for a MIP



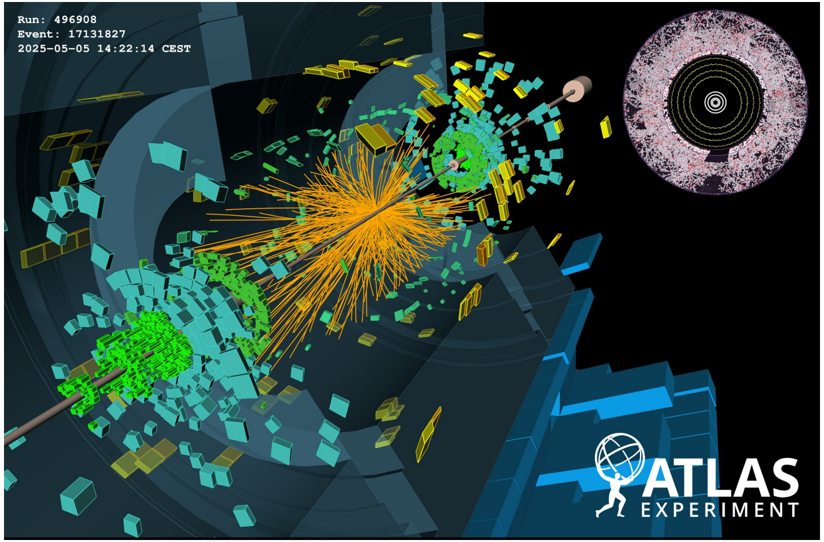




IBL planars 200 μm thick → 16 ke/MIP in unirradiated case will drop to 4.8 ke/MIP (1.5 ke threshold, 100 e noise) at 30% CCE

Summary

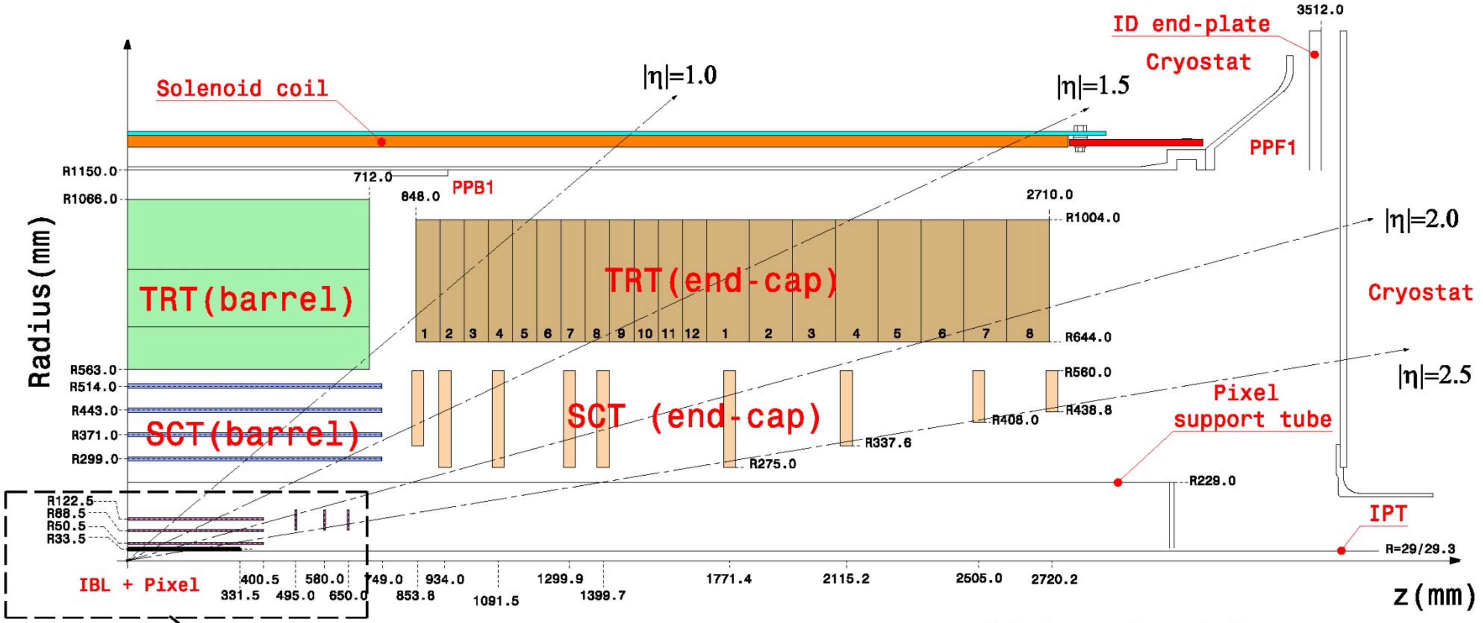
- The ATLAS Pixel detector is the most irradiated pixellated semiconductor detector we have at a collider based experiment
- As we are approaching the end of Run 3 and hence the end of lifetime, some parts have exceeded their design values by a substantial amount
- While certain parts are aging, anticipatory planning (e.g. installation of IBL, read-out upgrades) improved the resilience and allows good operation up to today
- Good performance in recording efficiency and data quality despite challenging conditions in Run 3

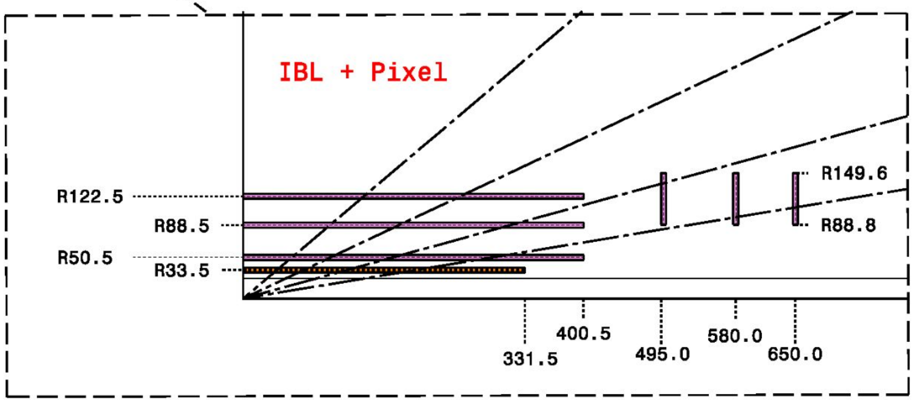


recorded pp-event in ATLAS

Thank you for your attention!

BACKUP

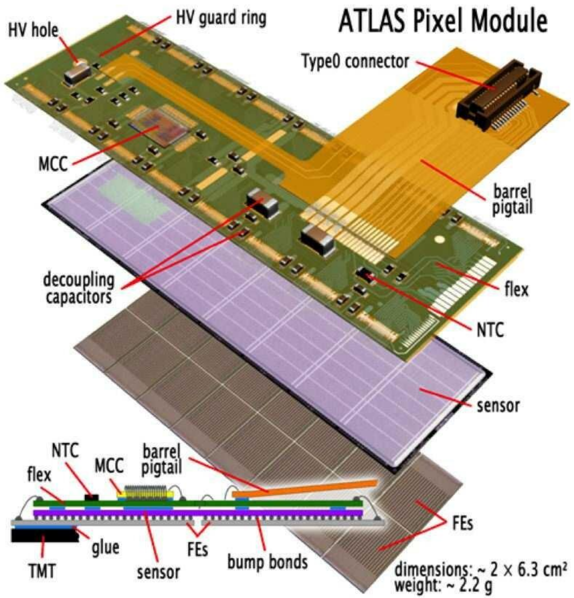


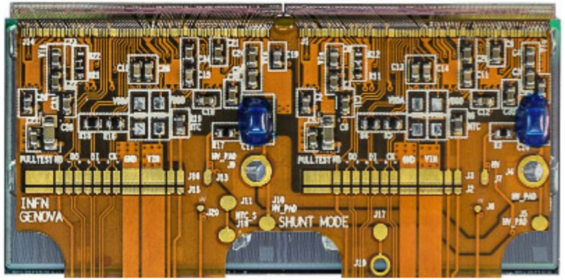


Detector envelopes (mm)

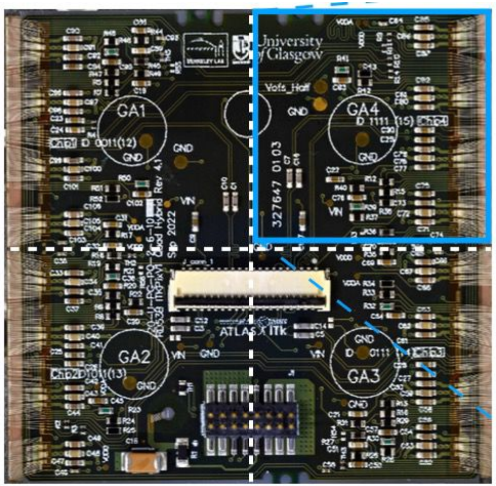
IBL	31<R<40
Pixel	42.5<R<242
SCT barrel	255<R<549
SCT end-cap	251<R<610
TRT barrel	554<R<1082
TRT end-cap	617<R<1106

Pixel Modules



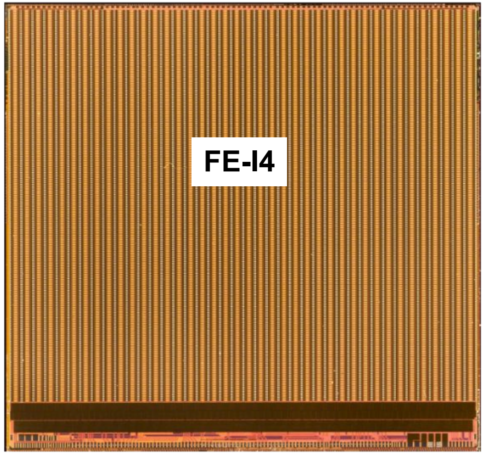


- Original Pixel system
  - 16 FEs per module
  - One MCC to control and aggregate data (HCCStar for ITk strips)
  - Planar n-in-n sensor
- Insertable B-Layer (IBL)
  - (mostly) 2 FEs per module
  - (mostly) n-in-n planar
  - (few) n-in-p 3D sensors in forward region
- ITk
  - In the barrel 3x1 or 2x2 FE modules
  - Innermost layer 3D
  - Outer layers planar n-in-p sensors

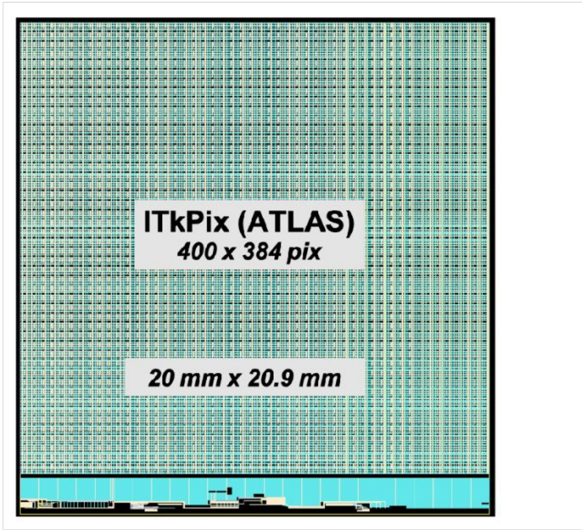


ATLAS Pixels: The Readout Chips

- 250 nm CMOS
- 7.6 mm x 10.8 mm chip size
- 160 x 18 pixel matrix
- FE output 40 Mbps (MCC output at 2x80 Mbps)
- Hit rate 200 MHz cm^{-2}
- 74% active area



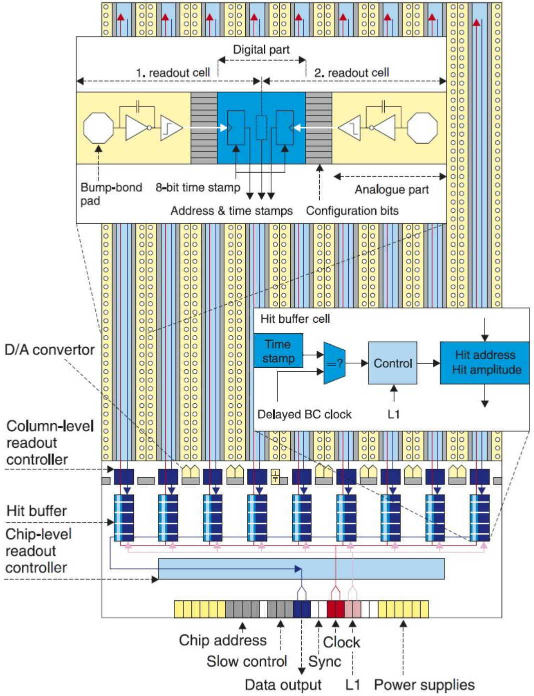
- IBM 130 nm CMOS
- 20.2 mm x 19.0 mm chip size
- 336 x 80 pixel matrix
- Each FE outputs at 160 Mbps
- Hit rate 400 MHz cm^{-2}
- 89% active area



- TSMC 65 nm CMOS
- 20.0 mm x 20.9 mm chip size
- 384 x 400 pixel matrix
- Four lanes output at up to 1.28 Gbps each
- Hit rate 3 GHz cm^{-2}
- FE-to-FE data aggregation

FE-I3 vs. FE-I4 Digital Architecture

FE-I3 schematic view



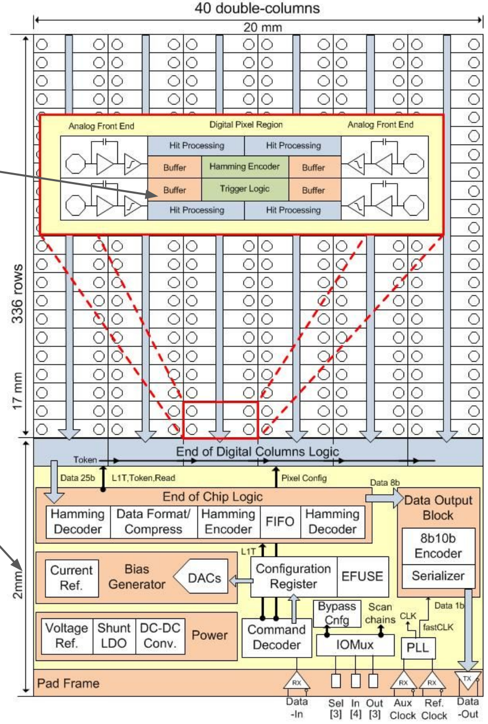
Redesign of the digital part going from FE-I3 to FE-I4

Local hit buffer was introduced, only hits which are triggered are sent to end-of-column (EOC)

→ only about 0.25 % of the hits are transferred to EOC, much reduced rate on DC bus

On FE-I3 this bus activity can only be reduced by increasing analogue threshold

FE-I4 schematic view

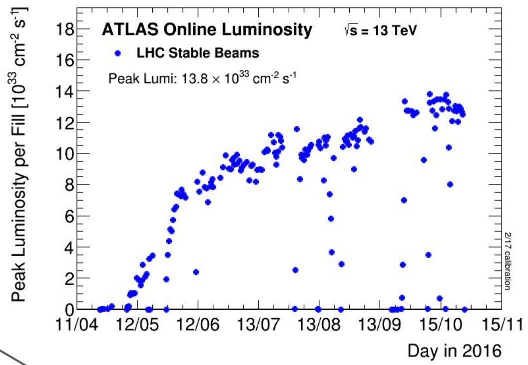


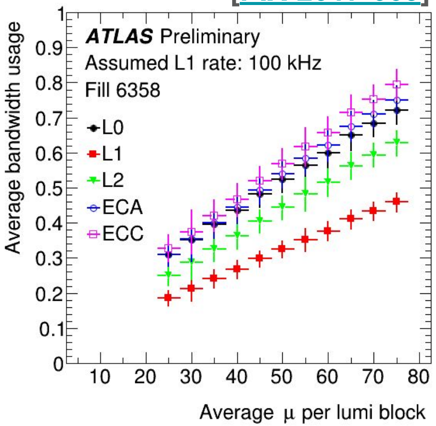
Run 2: Read-Out Limitations

At the intensity ramp up in 2016, the Blayer thresholds had to be increased in order to cope with high bandwidth usage as LHC inst. luminosity was exceeding 1x10^{34} cm^{-2}sec^{-1}

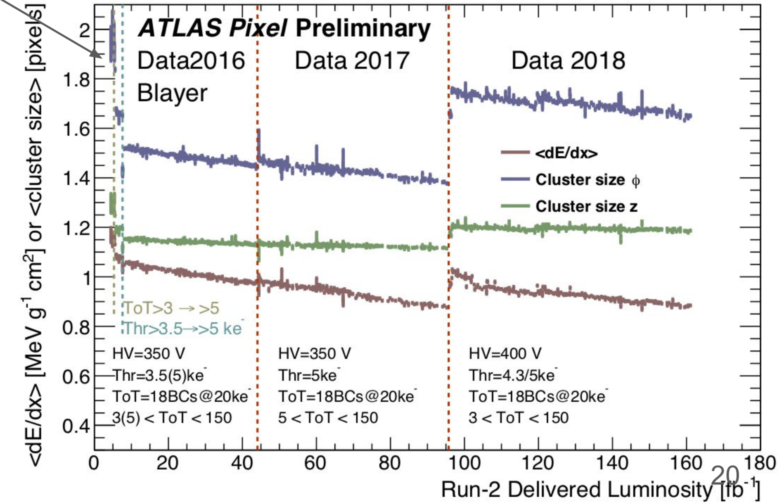
Subsequent upgrade of the off-detector read-out system for all layers reduced desynchronisation and recovered physics signal

[PIX-2017-009]

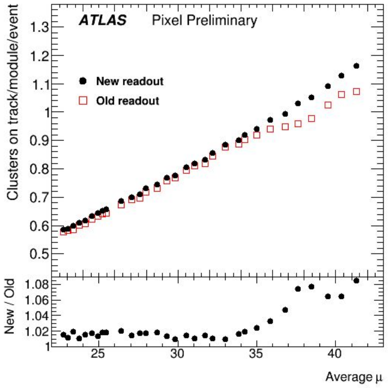




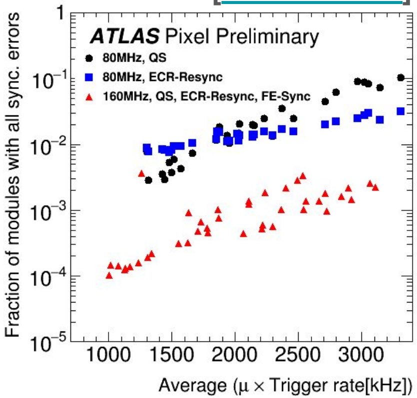
[PIX-2018-011]



[PIX-2017-001]



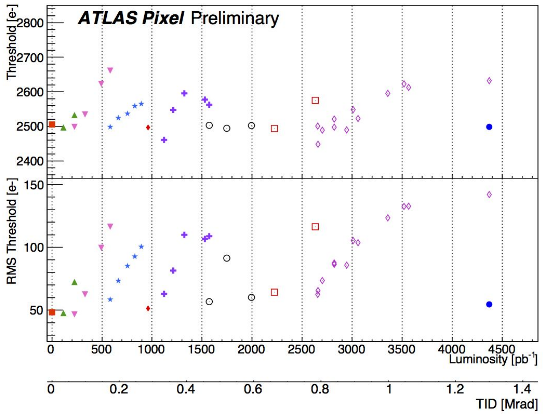
[PIX-2017-007]



both: layer-1 read-out upgrade effects on clusters and desync

Run 2: FE-I4 Radiation Induced Effects

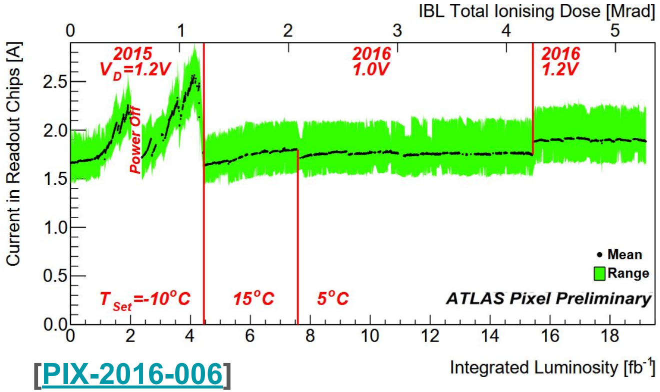
[PIX-2016-005]



- Radiation not only bulk damage, also surface damage
  - shift of working point, TID bump at a the first few Mrad → changes in IBL operation and frequent retuning
  - Total ionising dose (TID) effect causes increased leakage in NMOS
- Pre-irradiation of 130 nm ITk Strip ASICs

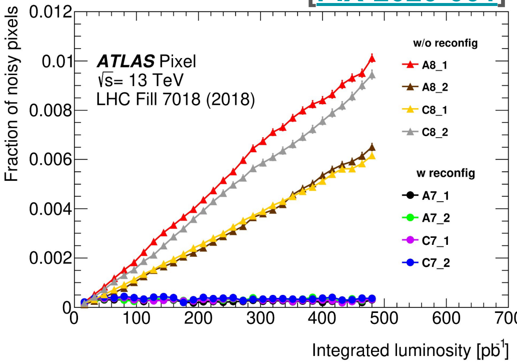
Publication on SEU in FE-I4: [G. Balbi *et al* 2020 *JINST* **15 P06023]**

- Single event effects cause bit flips in latches or transient glitches which can modify memory
- Mitigation implemented in the read-out to reconfigure FE configurations without introducing any dead-time (exploiting ATLAS ECR dead-time)
- ITkPix has trickling configuration where "idle" time on the TX lines is used to reconfigure FE memory



[PIX-2016-006]

[PIX-2020-001]



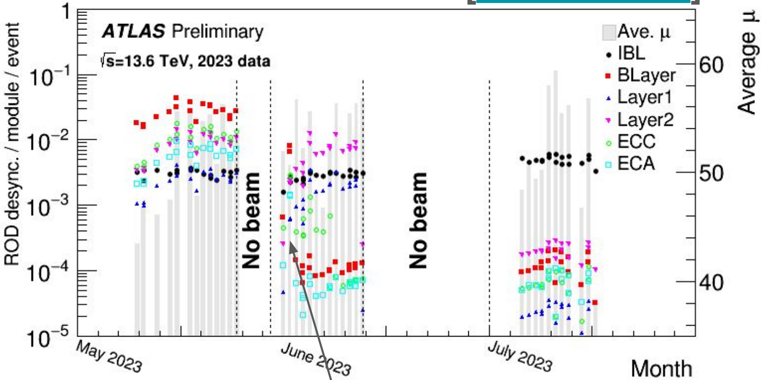
Run 3: Improving Desynchronisation

The ATLAS Pixel detector (including IBL) is a fully synchronous detector. Large events take longer to process.

Problem: FE-I3 pixel modules can only process 16 triggers → triggering them more often cause desynchronisation

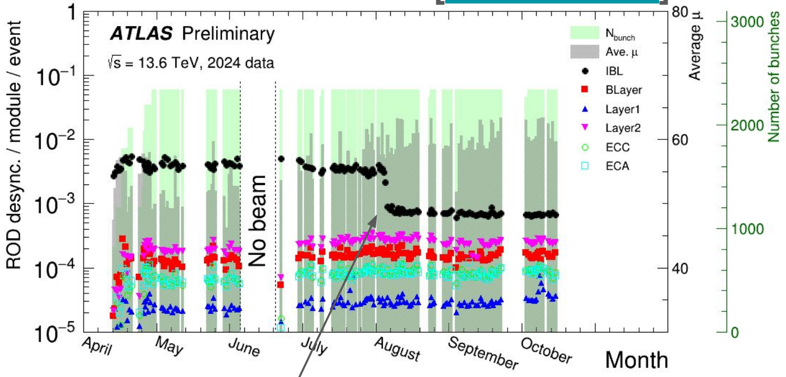
Solution: skip triggers if 16 are pending → "*smart-L1-forwarding*" (requires special **data-taking firmware**)

[PIX-2023-004]



Smart-L1-FW in BLayer

[PIX-2024-004]



Fix in IBL event building where hits were split

run 476875
31. May 2024

Item	Busy Frac. (Time)	Busy Frac. (Lumi)
IBL	0.17 %	0.17 %
BCM	0.00 %	0.00 %
Pixel	0.19 %	0.17 %

↓

run 499259
3. June 2025

Item	Busy Frac. (Time)	Busy Frac. (Lumi)
IBL	0.05 %	0.05 %
BCM	0.00 %	0.00 %
Pixel	0.10 %	0.09 %

New FW allows masking of busy as it offers the required protection → dead time reduction "*for free*"