Design and Characterization of a Radiation-Hardened CMOS Image Sensor Prototype

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Outline

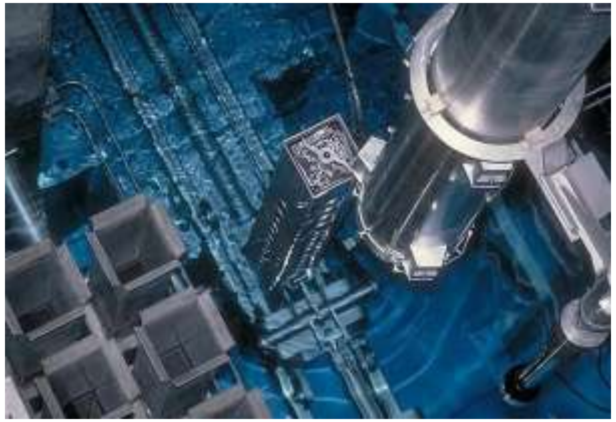
- **Introduction**
- **Radiation Effects**
- **Radiation-Hardened-By-Design (RHBD)**
- **Prototype Specifications and Designs**
- **Measurement Results**
- **Summary & Outlook**

Introduction

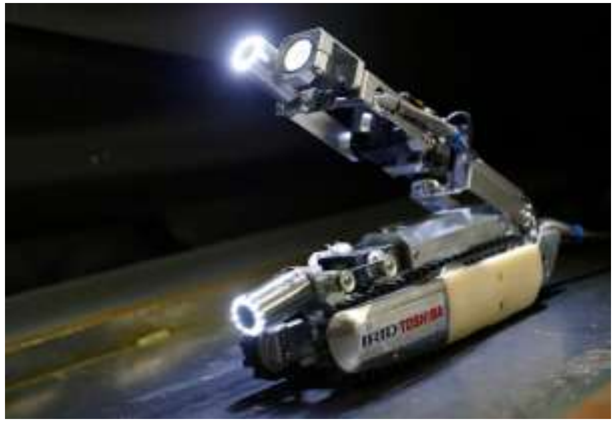
Applications

Radiation-tolerant cameras are demanding for imaging and monitoring Systems.

Nuclear Reactor



Remote Control



Space Exploration

HEP Experiments

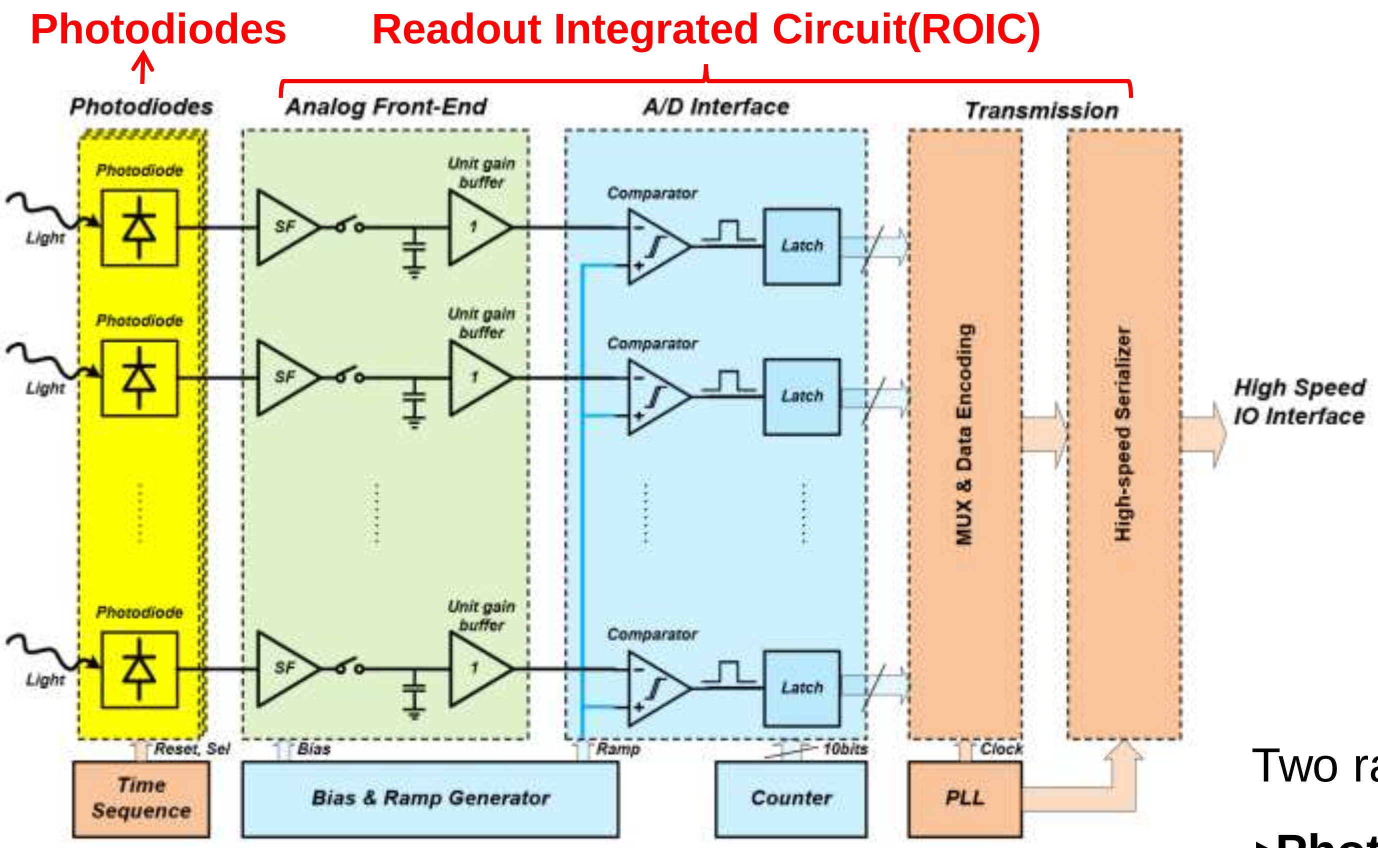
Current States

Three common radiation hardening approaches are as below.

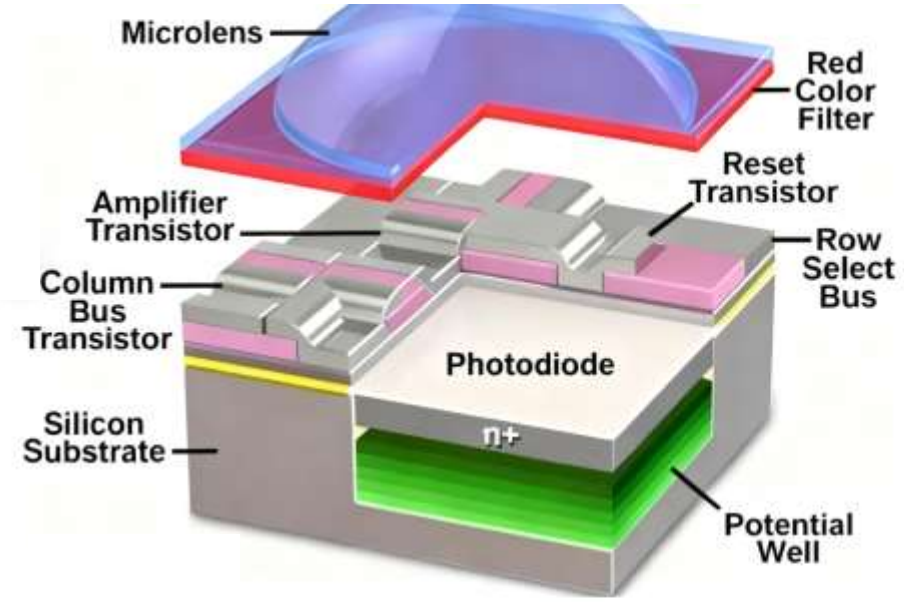
Conditions **&** ***Parameters***	***Approach-A*** 😔	***Approach-B*** 😊	***Approach-C*** 😊
Shielding with Lead ❓	YES	NO	YES
Radiation Tolerant Sensor ❓	NO	YES	YES
Weight	Very Heavy (~20kg) 😔	Light (<5kg) 😊	Not Heavy (5-10kg)
Radiation Tolerance	Low 😔	High 😊	Even Higher 😊
Lifetime	Short 😔	Long 😊	Long 😊

Introduction

CMOS Image Sensor



Block diagram of the CMOS Image Sensor



Two radiation-vulnerable critical blocks:

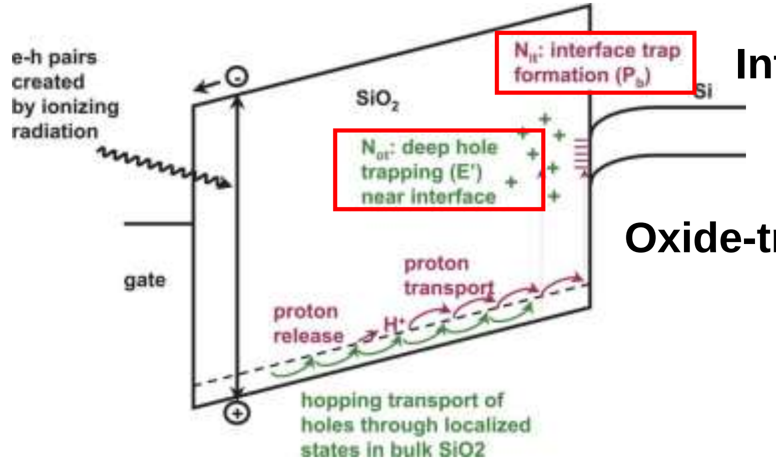
‣**Photodiode**: Incident light converted into charge signals

‣**ROIC**: transistors for amplification, digitization ···

Radiation Effects on the Image Sensor

Total Ionizing Dose (TID) Effect on Photodiodes and Transistors

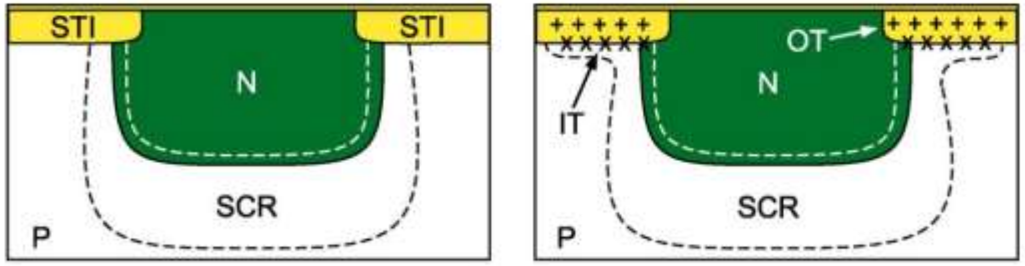
Ref: James R. Schwank, et al. Radiation Effects in MOS Oxides.



Interface states

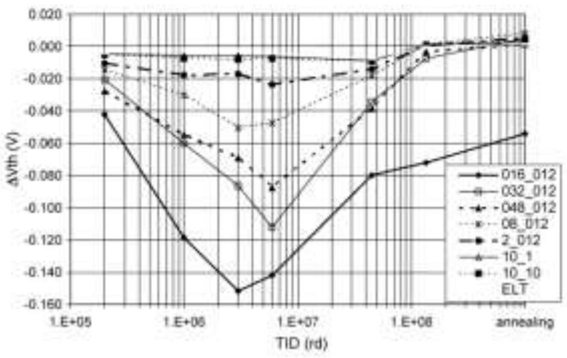
Oxide-trapped charge

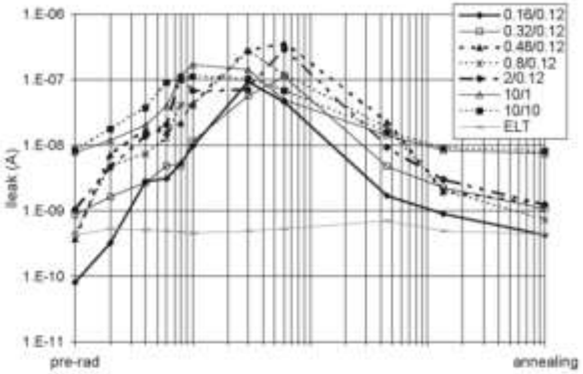
Ref: V. Goiffon, et al. Generic Radiation Hardened Photodiode Layouts for Deep Submicron CMOS Image Sensor Processes.



(a) Pre-irradiation (b) High TID

Ref: Federico Faccio and Giovanni Cervelli. Radiation-Induced Edge Effects in Deep Submicron CMOS Transistors.





For photodiodes:

Dark current increase, Depletion region extension

For transistors:

Threshold voltage shift, Leakage current increase

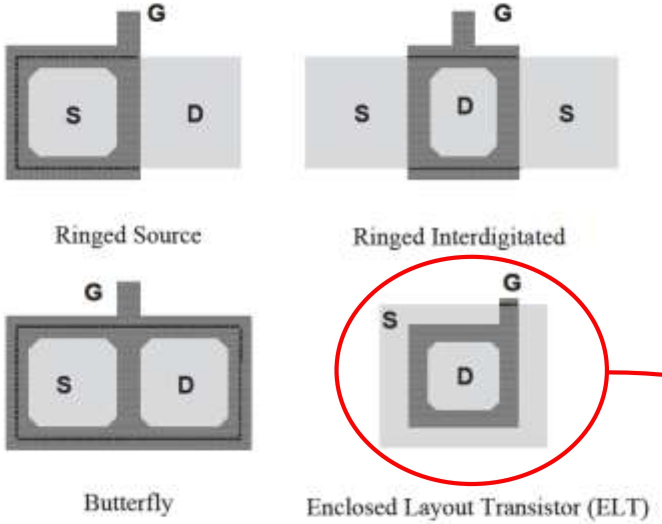
Summary

- STI is a big trouble for both **photodiodes** and **transistors**
- **What about gate oxide?**

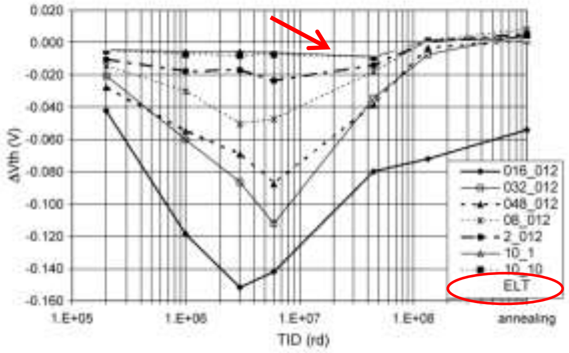
Radiation-Hardened-By-Design (RHBD)

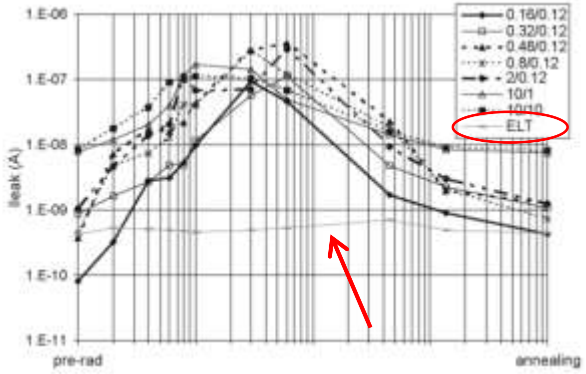
Total Ionizing Dose (TID) Effect

Ref: Radiation Effects on Embedded Systems.



Ref: Federico Faccio and Giovanni Cervelli. Radiation-Induced Edge Effects in Deep Submicron CMOS Transistors.





Layout techniques to enhance the radiation tolerance of MOS transistors

- mitigate the TID effect on STI
- but can not totally eliminate the TID effect on gate oxide
- ELT is very tolerant to ionizing radiation （~ 100Mrad）
- Gate oxide is much more tolerant to ionizing radiation

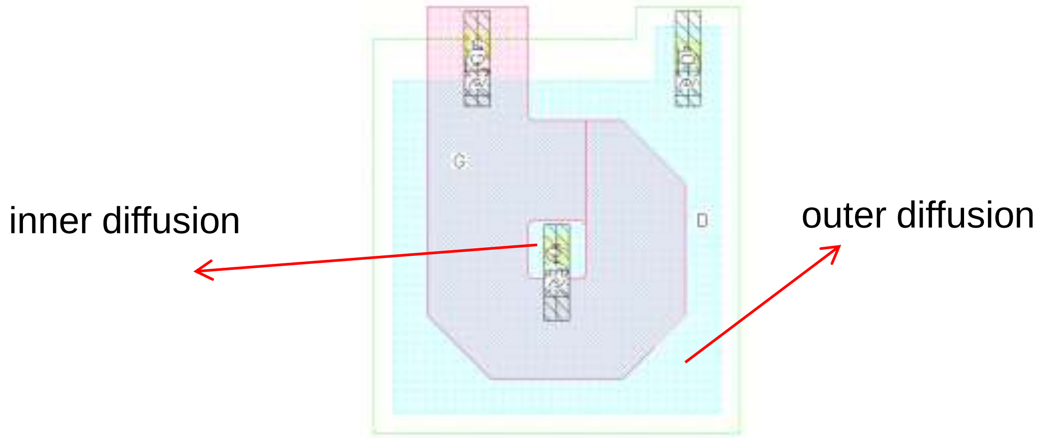
Radiation-Hardening Strategy

Comparison of STI oxide and gate oxide

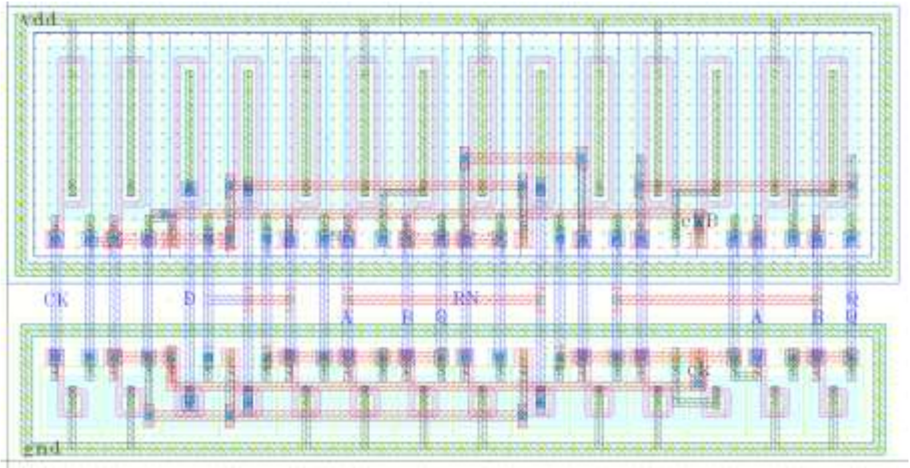
180nm process	STI	Gate Oxide
depth / nm	~ 400	~ 4

Prototype Designs

Read Out Integrated Circuit (ROIC)



Implemented Enclosed Layout Transistor



D Flip-Flop Layout with ELT

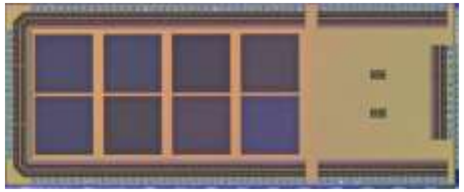
*For radiation-hardened **photodiodes**, please follow the presentation of J. Deng on Tuesday morning.*

- All analog circuits (and critical digital circuits) designed with enclosed layout transistors.
- P+ and N+ guardrings implemented to decrease latch-up possibility.
- Outer diffusion of adjacent NMOS transistors connected to the same node or isolated by P+ rings to cut the leakage path between transistors.

Prototype Specifications

Timeline of the Image Sensor

MPW1: To study the RHBD strategy.



Features:

· 64×64 Pixel Array

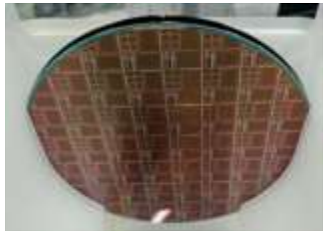
· RH / STD Photodiodes

· RH / STD ADC

Today's topic!

Sensor Prototype I

To characterize TID performance



Features:

· 1280×720 Pixel Array

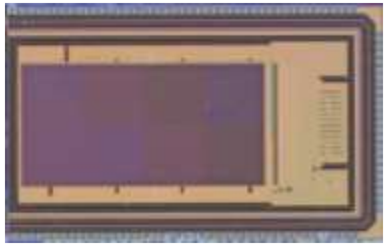
· 1 Gbps data rate

· 100Mrad-level radiation tolerance

Camera Prototype I

2022 2023 2024 2025 2026 2027

Camera Prototype II



Features:

· 256×128 Pixel Array

· Column-parallel ADC

· LVDS interface

MPW2:To validate the read out chain.

Sensor Prototype II

—— higher performance

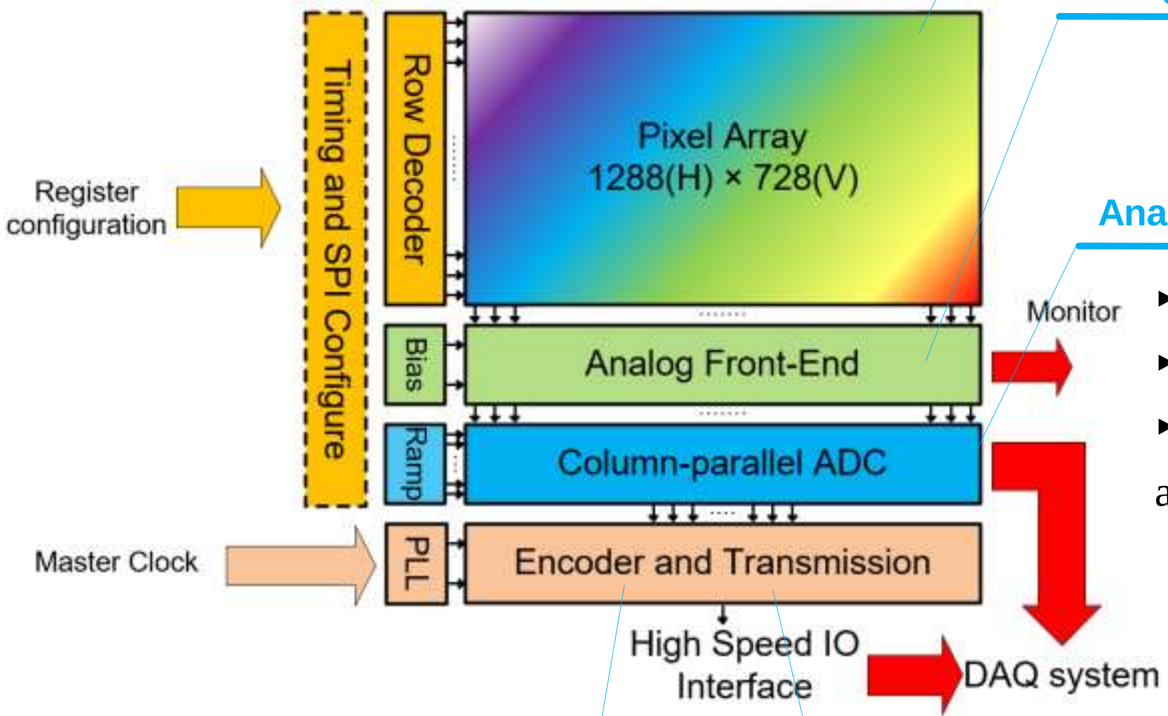
· Photodiode optimization (geometry ···)

· ROIC performance improvement (power, noise ···)

· Triple modular redundancy (Single Event Effect)

Prototype Specifications

Overall Architecture



Active Pixel

- 10 µm pixel size, 1288 × 728 pixel array
- Sensing **Photodiode** + 3 transistors

Analog Front End Electronics

- Double sampling —— low noise
- Amplifier buffer —— low noise

Analog/Digital Interface

- Digital codes (0/1) are more robust compared to analog signals
- **10bits digital quantization** —— humans can tell 200-400 gray levels
- Column parallel Wilkinson **ADCs** are popular due to the simplicity, area and power efficiency

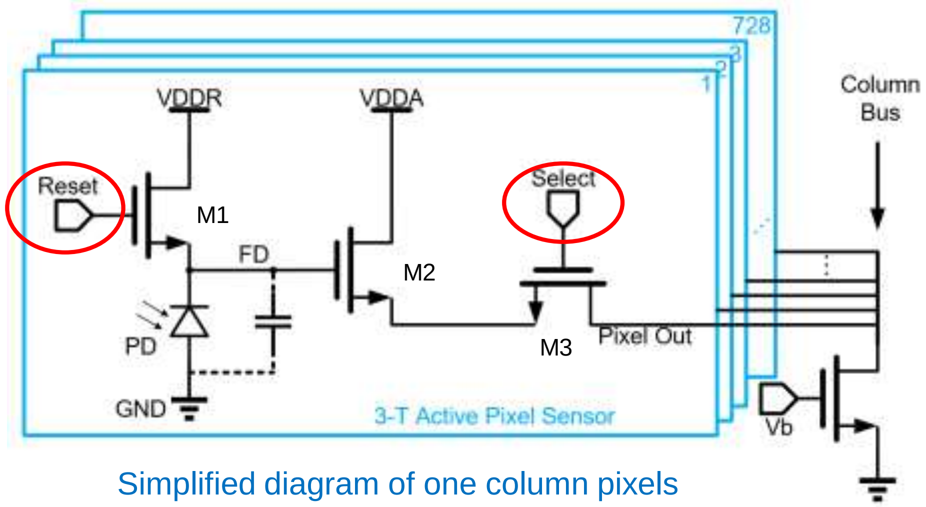
Data packing

- Formatted pixel data
- **Data transmission** with phase lock loop

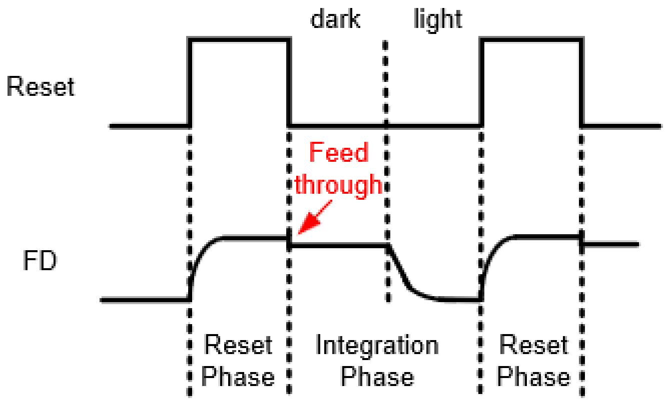
Serializer with LVDS Interface

Prototype Designs

In-pixel Electronics



Simplified diagram of one column pixels



Working principle of the pixel

- 3-T Active Pixel Sensor

  Photodiode + 3 transistors in 10×10 μm^2

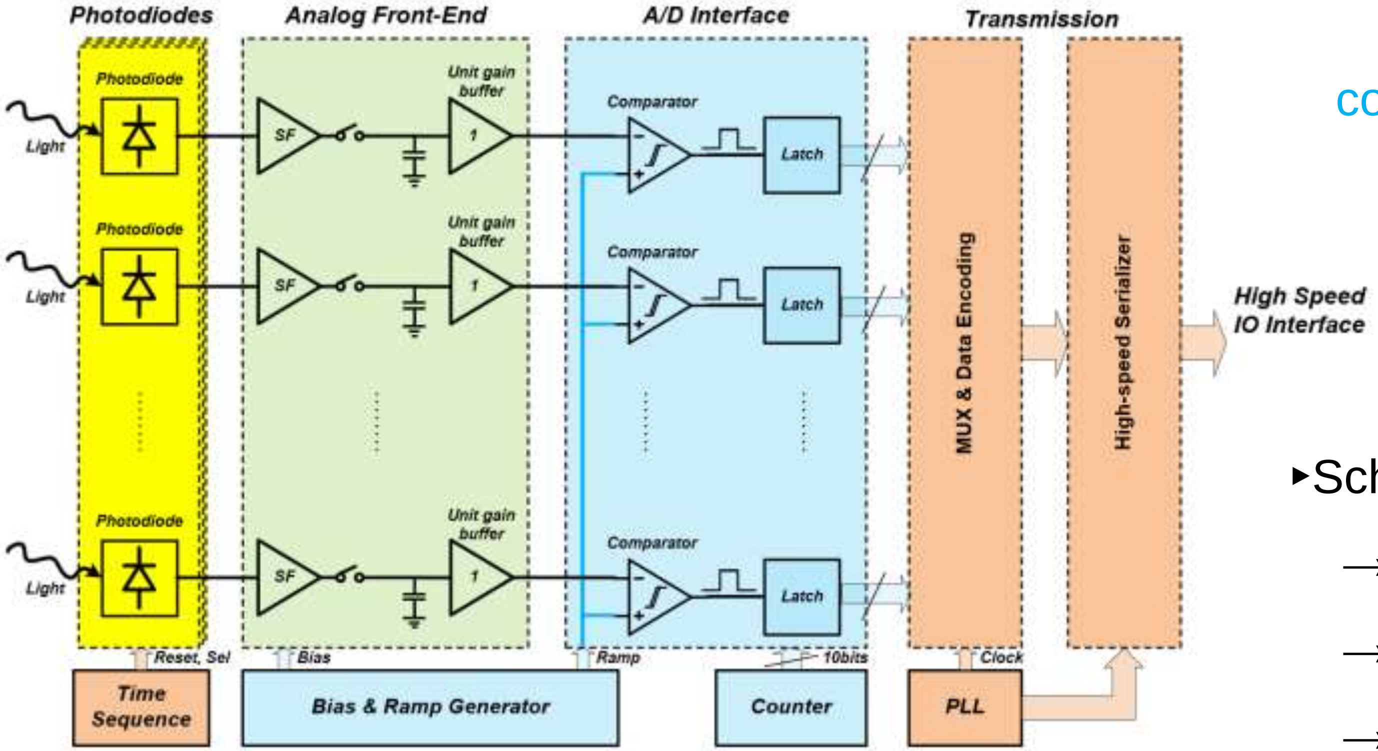
  M1 and M3 work as switches, M2 is used to drive the large load capacitance of the column bus

- In reset phase, the reset transistor is on to **charge** the photodiode to a high level (reset level).

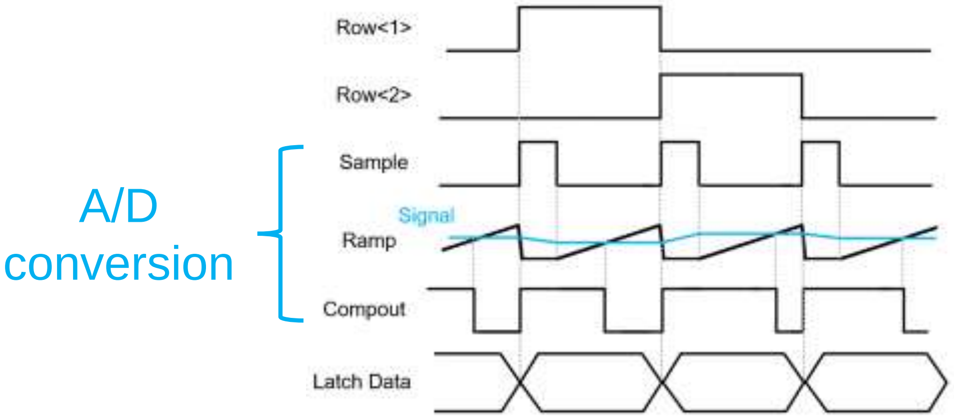
- In integration phase, the reset transistor is off and photodiode **discharges** due to leakage current or photon-generated electron-hole pairs.

Prototype Designs

Read Out Scheme



Block diagram of the readout chain

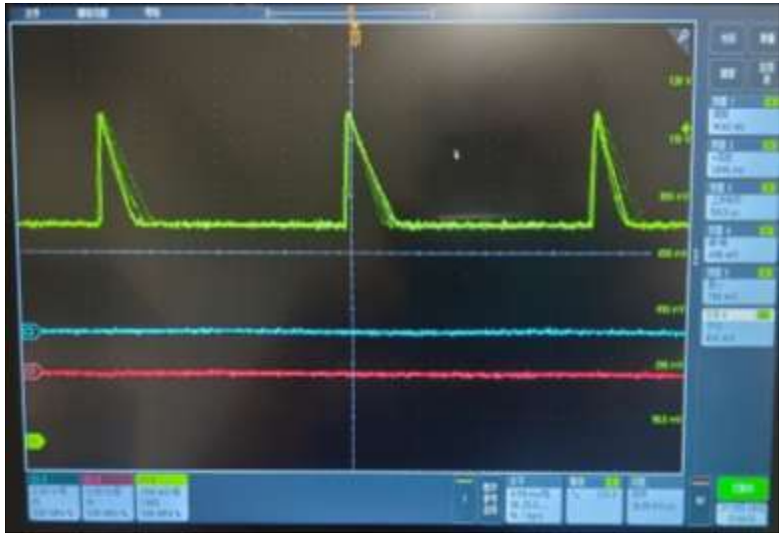


Time Sequence of readout scheme

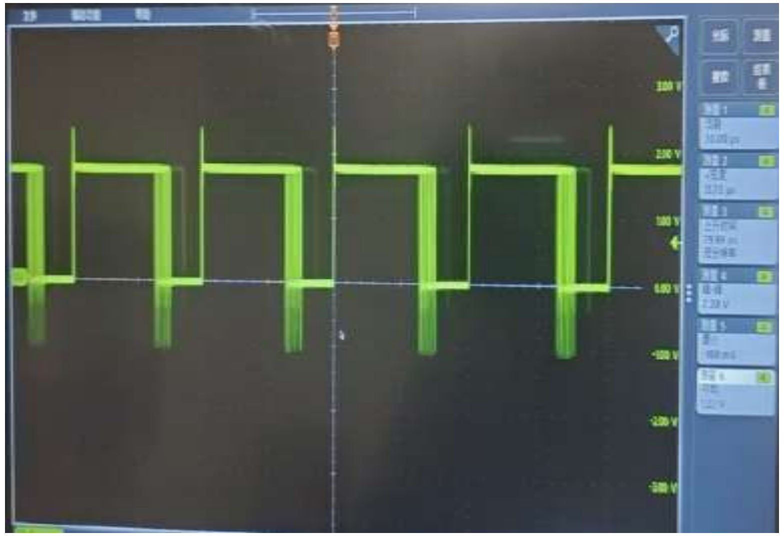
- Scheme:
  - → photodiodes for photon-electron conversion
  - → pixels readout row by row
  - → voltages sampled and digitized
  - → digitized outputs formatted and transmitted

Measurements Results

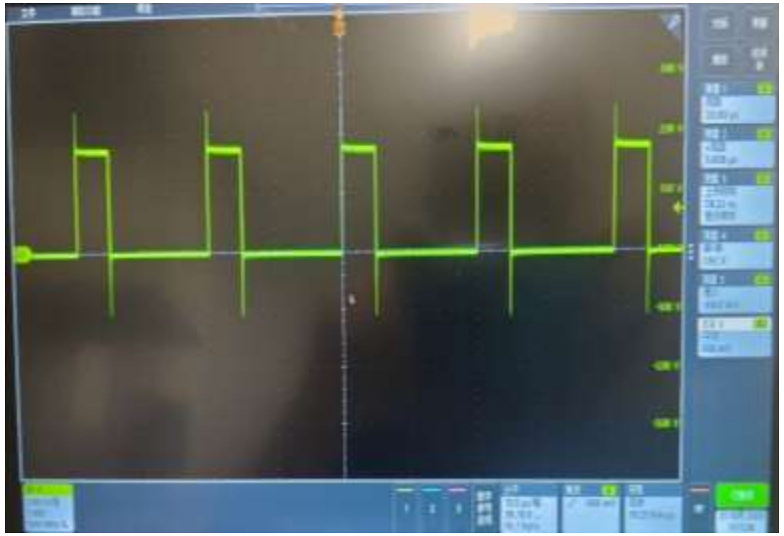
Functionalities



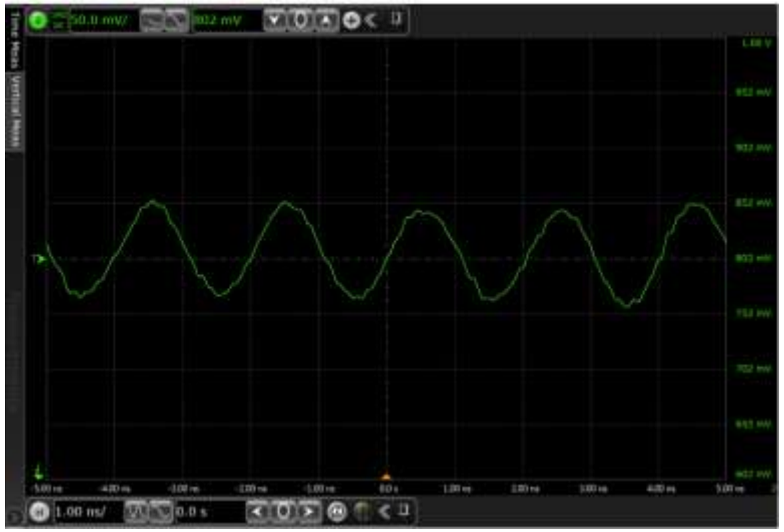
Pixel



Comparator Out



Sample

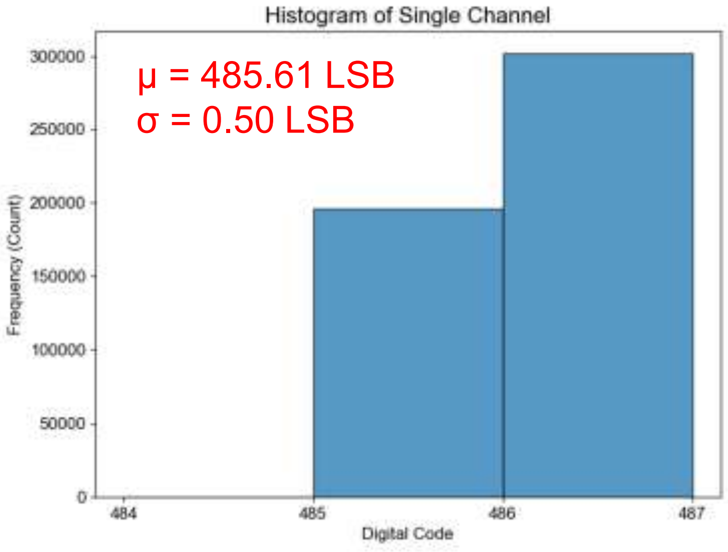


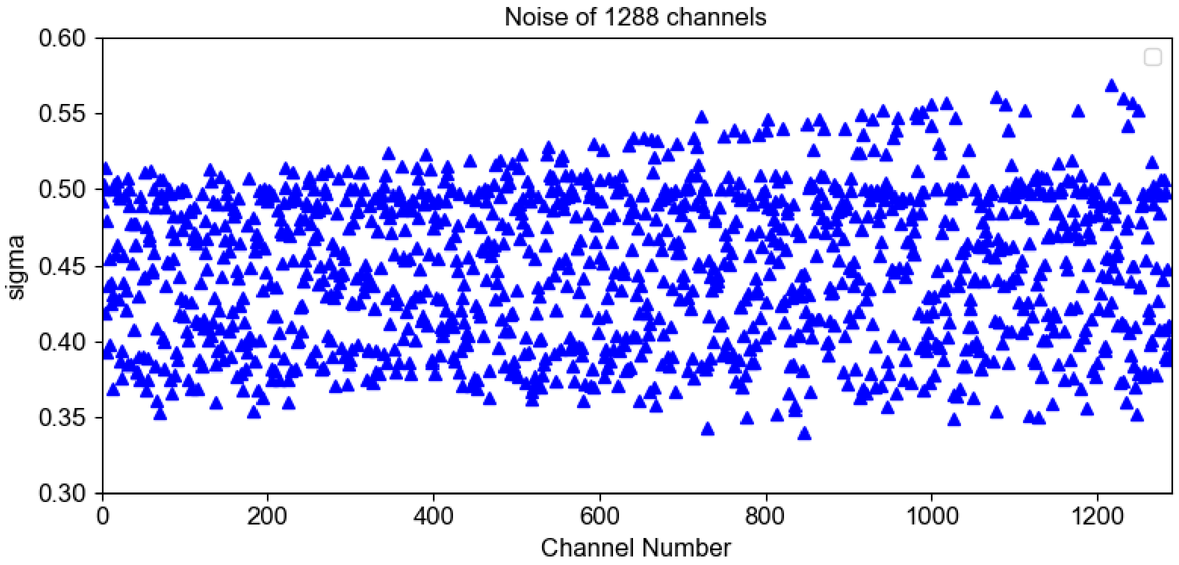
PLL
500 MHz

Measurements Results

A/D Conversion —— Noise

Methods: Study digital outputs distribution with a fixed input voltage





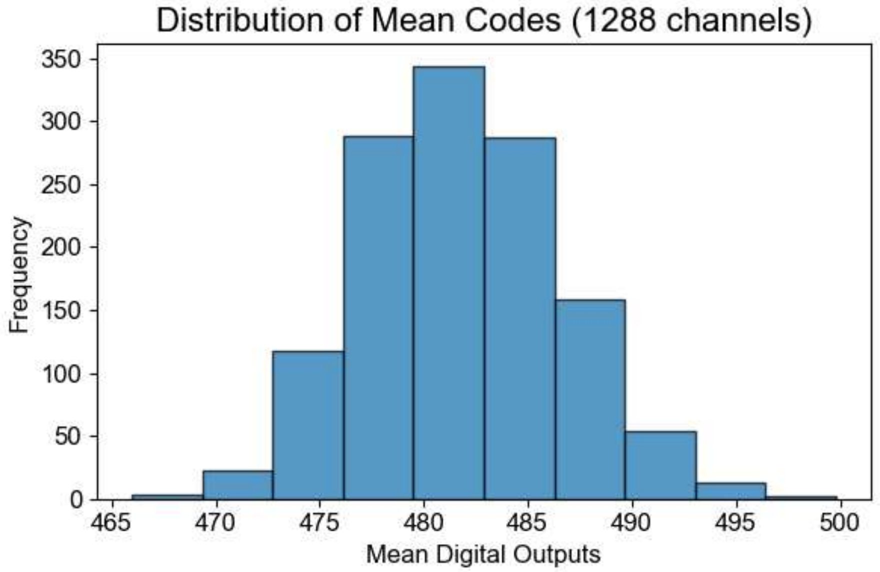
- **Only 3** digital codes obtained
- Noise of ADC calculated to be 0.50 LSB
- Uniform Noise behaviors of 1288-channel ADCs
- Acceptable conversion noise for the image sensor

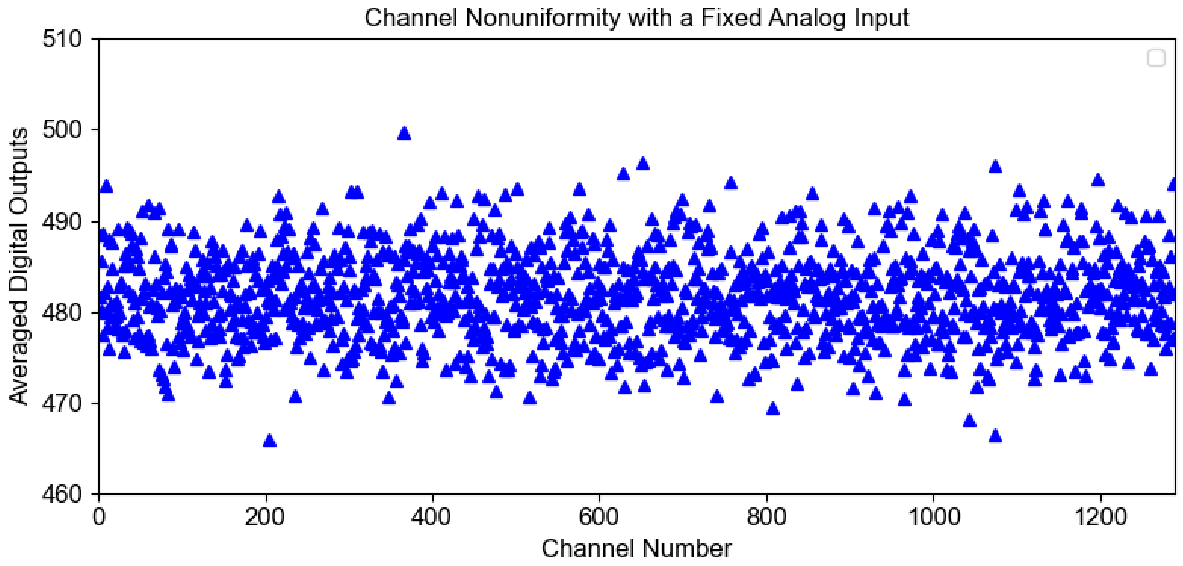
Measurements Results

A/D Conversion —— Column Offset Correction

Methods: 1. Measure (1288) mean digital values with a fixed input voltage

2. Calibrate DC offset of 1288 ADCs to get good uniformity





- ▸The results indicates the Monte Carlo nonuniformity of column-level ADCs.
- ▸From the distribution, the DC offset can be corrected with digital algorithm

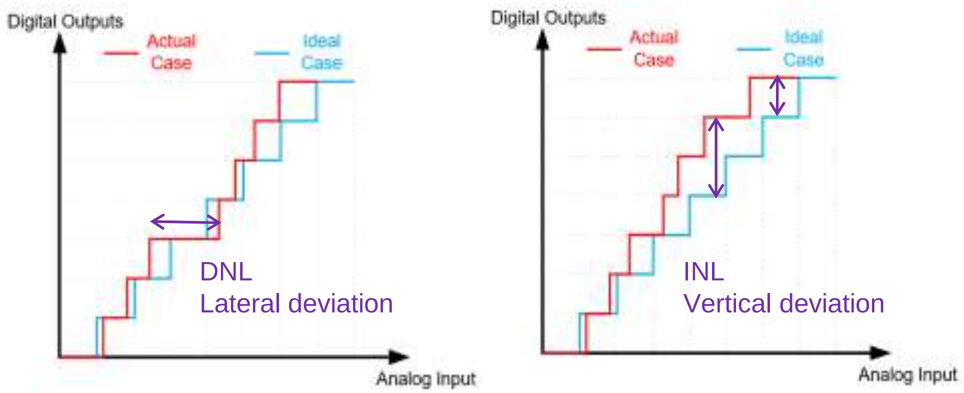
Measurements Results

A/D Conversion —— Histogram and Nonlinearity

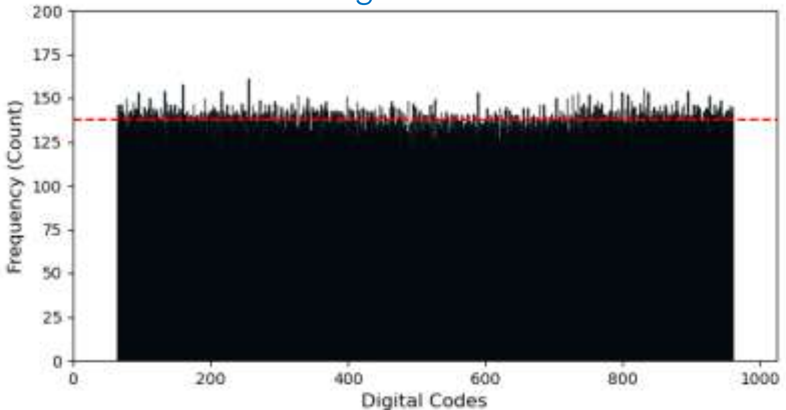
Methods: Measure digital outputs with a ramp wave for enough time

Calculate nonlinearity from digital codes histogram

Non-Linearity diagram



Histogram of codes



‣Differential Non-Linearity (DNL)

DNL indicates the analog difference relative to the ideal situation

‣Integral Non-Linearity (INL)

INL is the difference between the actual and the ideal digital output

‣Histogram measurement

Ideally, the histogram distribution should be completely flat.

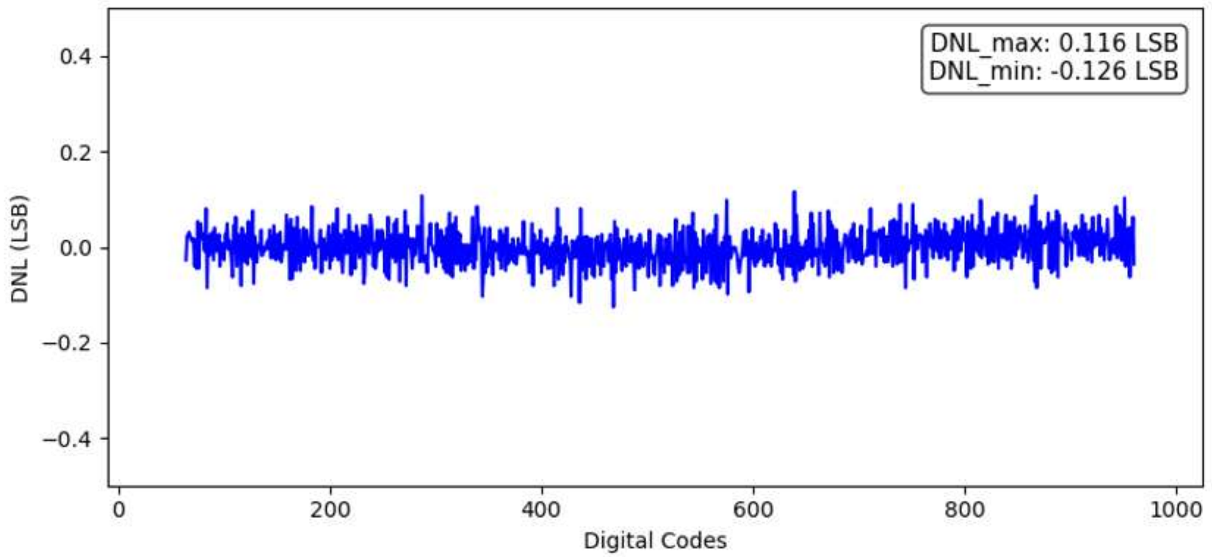
Actually, the histogram counts deviate from the average value.

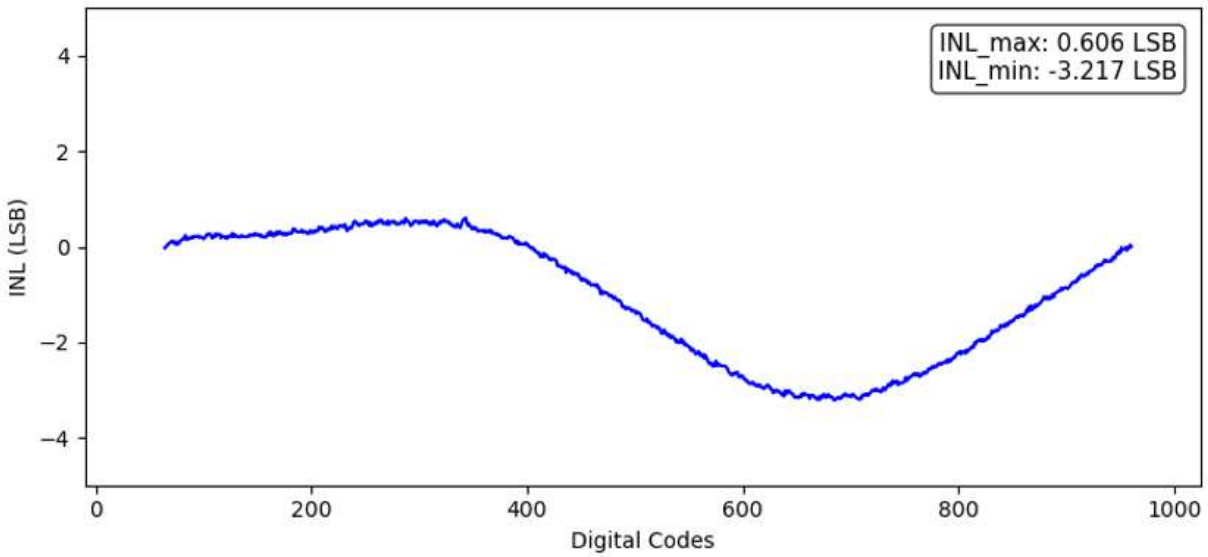
$$\mathrm{DNL}(n) = \frac{Counts\_actual(n) - Counts\_average}{Counts\_average}$$

$$\mathrm{INL}(n) = \sum_{i=0}^{n} DNL(i)$$

Measurements Results

A/D Conversion —— Nonlinearity

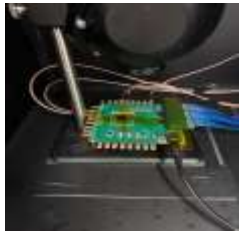




- The Differential Non-Linearity is relatively small and negligible
- The Integral Non-Linearity is a little high but it is acceptable for the imaging syetem

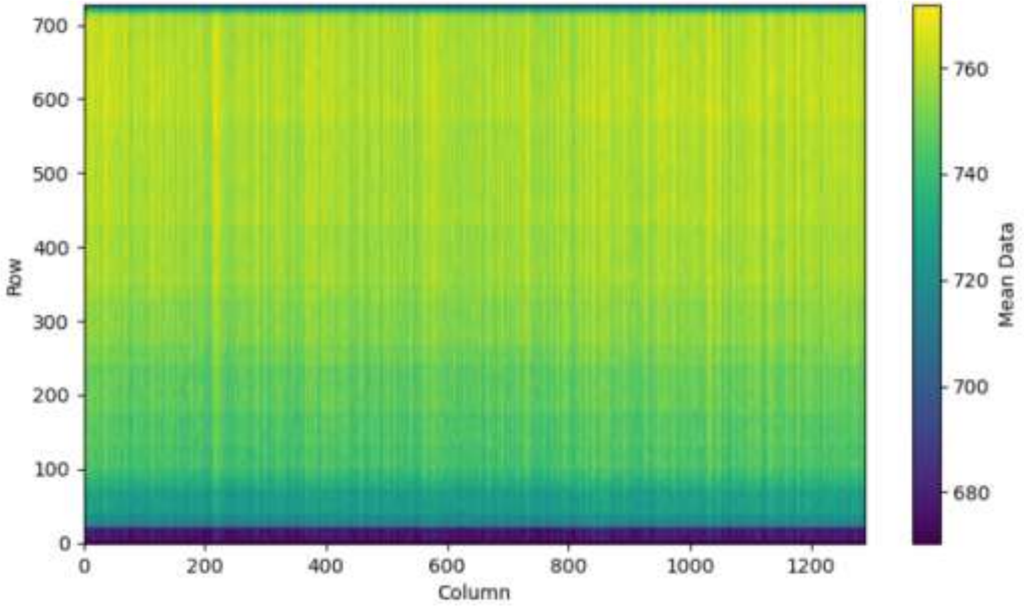
Measurements Results

Pixel Array —— Dark Current

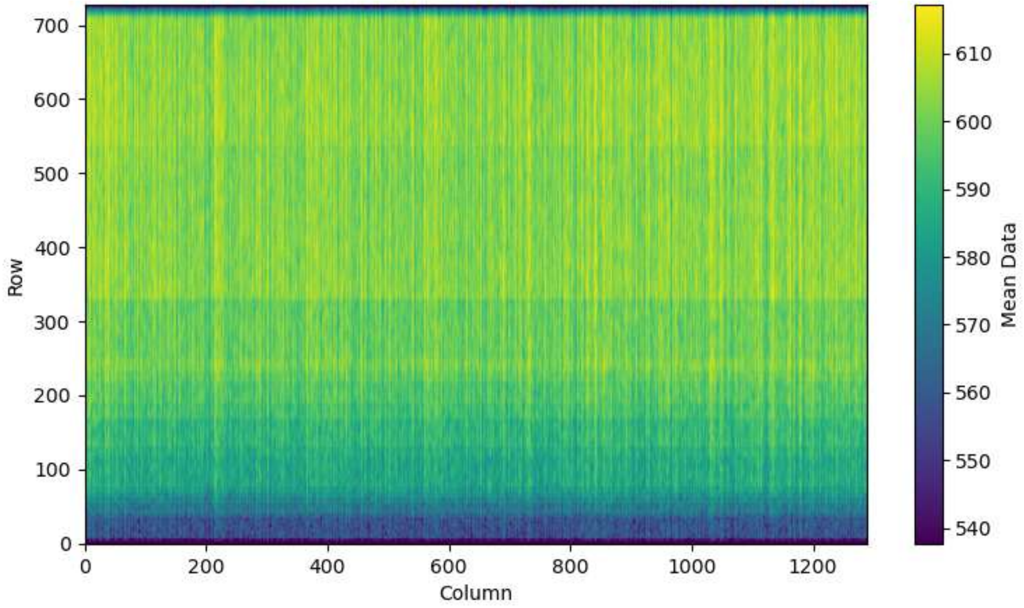


Under test!

Reset level of pixel matrix



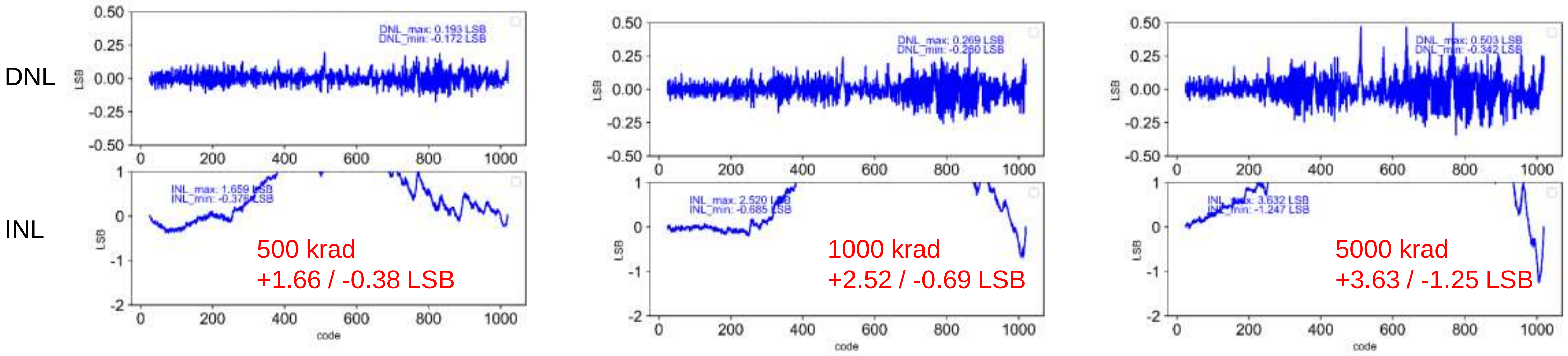
10ms dark current integration



- Strong non-uniformity in rows (0-20, 720-727) —— matrix edge, but not fully understood
- Vertical stripes dominated by the column readout chain (can be calibrated)

Measurements Results

A/D Conversion —— irradiation



- The results are from another ADC chip with similar design
- DNL rises from +0.20/-0.18 LSB → +0.50/-0.34 LSB
- INL changes from +1.66/-0.38 LSB → +3.63/-1.25 LSB

Summary & Outlook

Summary

- Pixel matrix information obtained with integrated read out chain
  - ---have to further understand the non-uniformity before imaging
- On-chip ADCs evaluated
  - --- DNL: +0.12/-0.13 LSB
  - --- INL: +0.61/-3.21 LSB (acceptable for the imaging system)
  - --- Noise: 0.45 LSB
  - --- TID: deterioration of DNL and INL

Outlook

- Sensor characterization to be continued
- Irradiation (up to 100 Mrad) and annealing tests to be performed

Thanks!

Contribution List

J. Deng, X. Geng, P. Li, D. Liu, H. Zhu✉ (Zhejiang University)

T. Li, F. Yan, J. Liu, P. Yang (Central China Normal University)

Y. Cheng, Y. Qin, C. Feng (University of Science and Technology of China)

M. Ji, K. Li, S. Li, Y. Liu, Z. Luo, H. Pang, C. Wang, J. Wu, S. Xiao, L. Zhang, X. Li

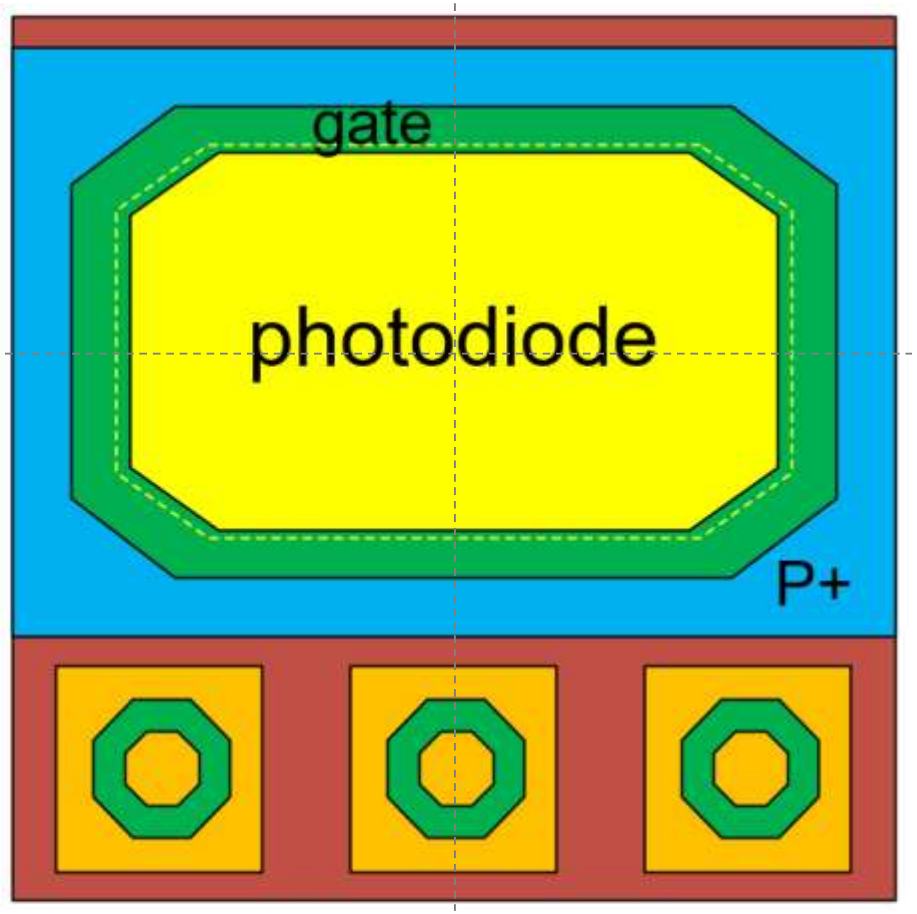
(China Institute of Atomic Energy)

Thanks for your attention !

Backup

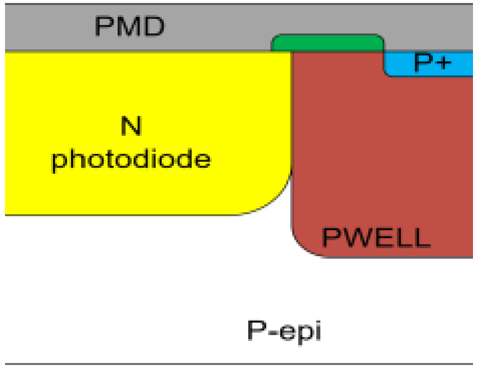
Backup

Photodiodes

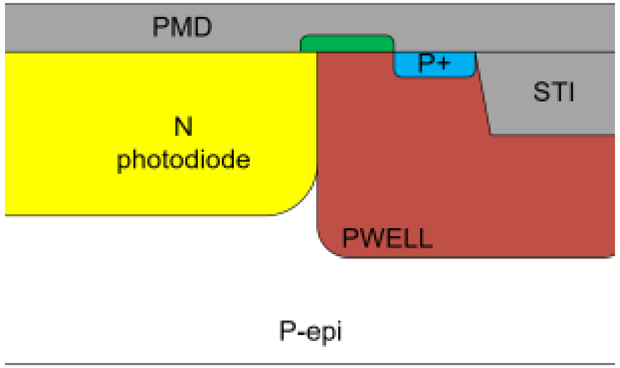


Simplified Pixel layout diagram
(Inspired by V. Goiffon(ISAE-SUPAERO Group))

Lateral cross section



Vertical cross section



- Gate Oxide replaces STI
- P+ to further prevent depletion region extension to STI
- In lateral case, pixels are isolated by P+ instead of STI
- In vertical case, pixels are isolated by P+ → STI → P+

For detailed information, please follow the presentation of J. Deng on Tuesday morning.

Backup

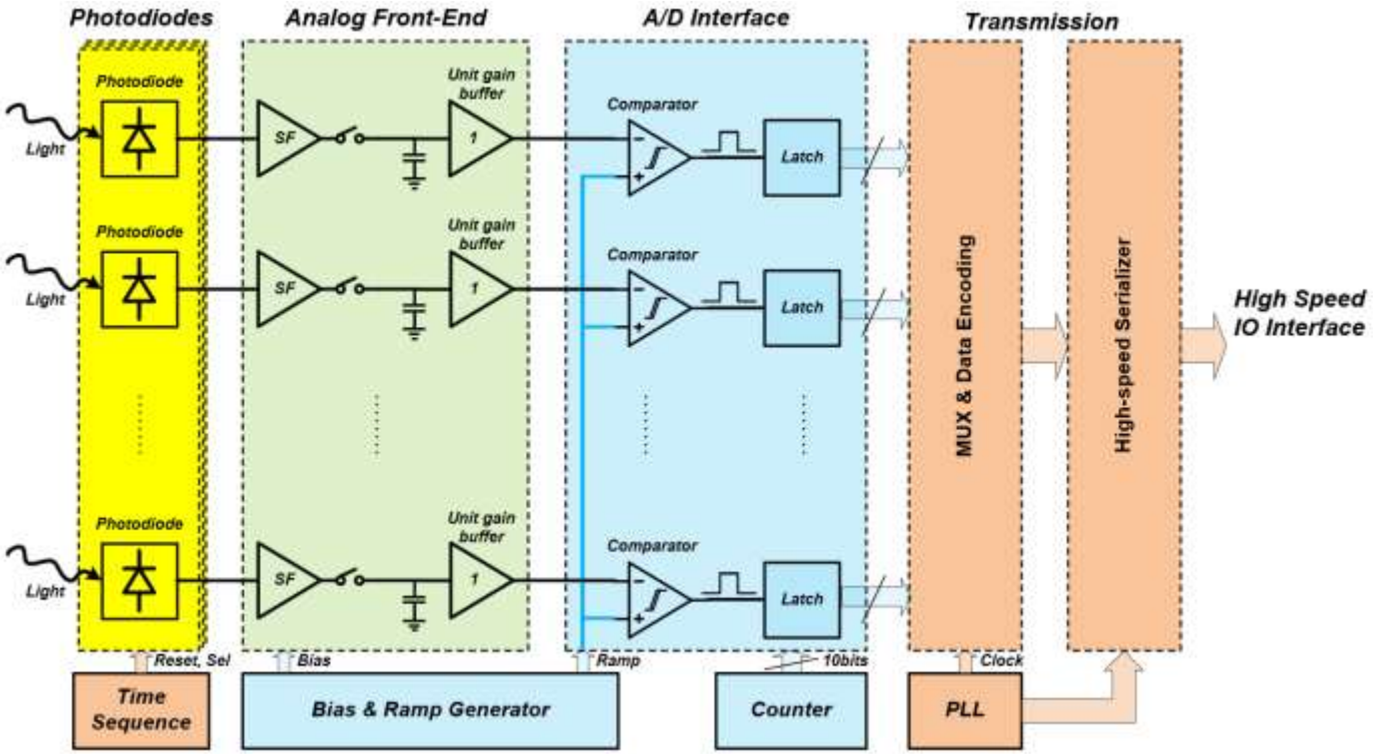
Aims and Requirements

Technology	180 nm CIS
Pixel Size	$10 \times 10\ \mu m^2$
Number of Pixels	1280×720
Chip Dimensions	$14.7 \times 11.6\ mm^2$
Read Out Mode	Row-wise
Exposure Time	Tunable
Frame Rate	> 60 FPS
ADC Resolution	≥ 10 bits
Data Rate	≥ 1 Gbps
Radiation Tolerance	100 Mrad(SiO_2) $10^{12}\ n_{eq}/cm^2$

Backup

CMOS Image Sensor

Photodiodes **Readout Integrated Circuit(ROIC)**



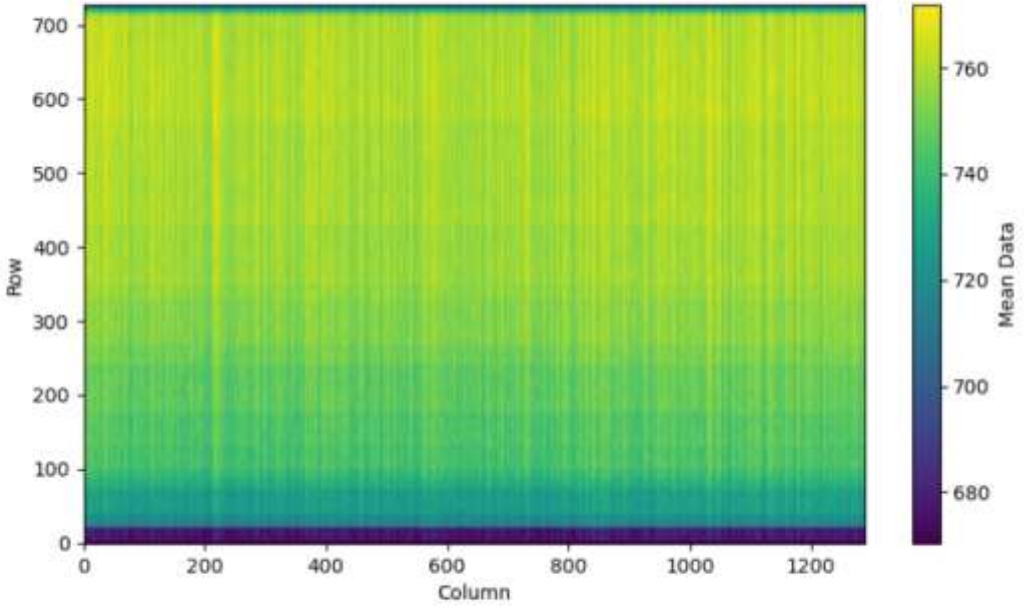
Block diagram of the CMOS Image Sensor

- Photodiodes (Light Detection)
  - Convert incident light into charge signals
  - Each pixel includes reset & select control
- Analog Front-End (Signal Conditioning)
  - Source follower drive the load
  - Unity gain buffer escape coupling from ADC
- A/D Interface (Single-Slope Conversion)
  - Comparator detects crossing with ramp signal
  - Latch and counter generate digital outputs
- Bias & Ramp Generator
  - Provides bias current and reference ramp for ADCs
- Transmission (High-Speed Output)
  - Data encoding and multiplexing for multiple channels
  - Serializer and PLL enable high-speed data interface

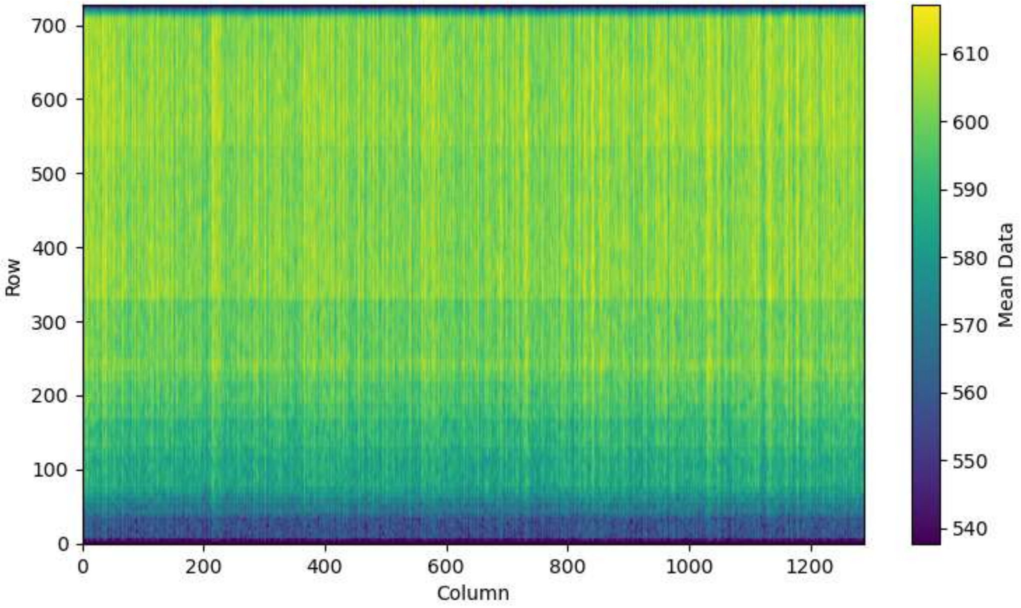
Backup

Pixel Array —— Photon Incidents

Reset level of pixel matrix



10ms photon incidents current integration



- Pictures obtained with a 520nm Light from Xenon lamp
- Overall behaviors are similar to the dark current case, but with higher current

Thanks !

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M. Ji, K. Li, S. Li, X. Li, Y. Liu, Z. Luo, H. Pang, C. Wang, J. Wu, S. Xiao, L. Zhang (China Institute of Atomic Energy)