

The CMS Phase-2 Tracker Upgrade: Meeting the Challenges of the HL-LHC

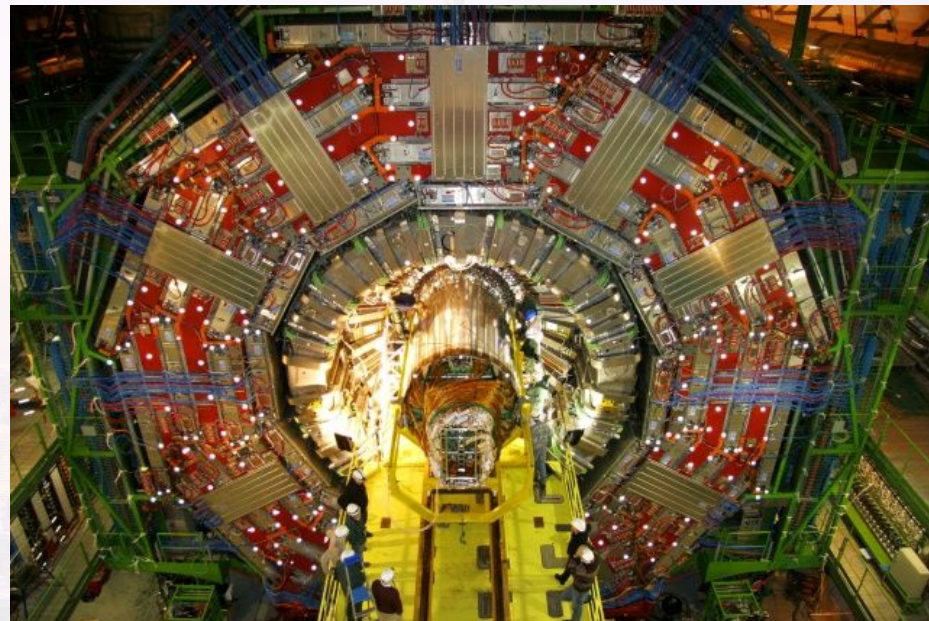
Amrutha Samalan¹ on behalf of the CMS Collaboration

1. Paul Scherrer Institute (PSI), Switzerland



The 14th international "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD 14)
Nov 16 – 21, 2025- Academia Sinica

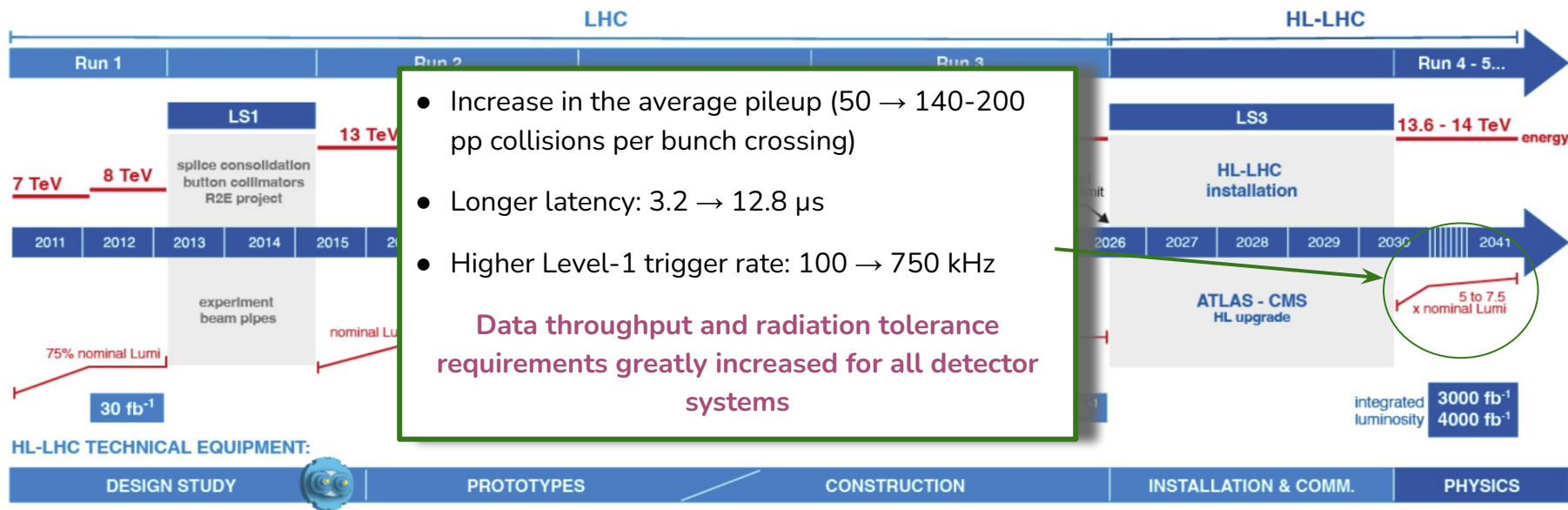
- Introduction to HL-LHC
- CMS Phase-2 Tracker Upgrade
- Outer Tracker Upgrade
 - Outer Tracker Layout and Modules
 - Module Production Status
 - Module Quality Control Tests
 - Latest Irradiation Test Results
 - Status of integration Tests
- Inner Tracker Upgrade
 - Inner Tracker Layout and Modules
 - Module Production Status
 - Module Quality Control Tests
 - Latest Irradiation Test Results
 - Status of integration Tests



Phase-1 tracker installation at CMS

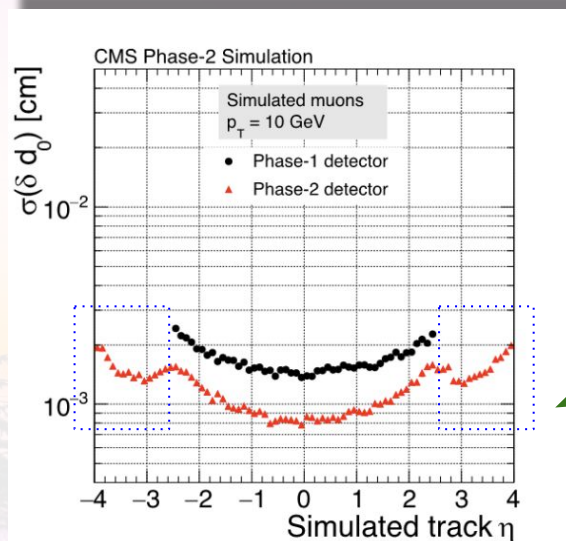


LHC / HL-LHC Plan



The current CMS Tracker will be replaced with an upgraded system

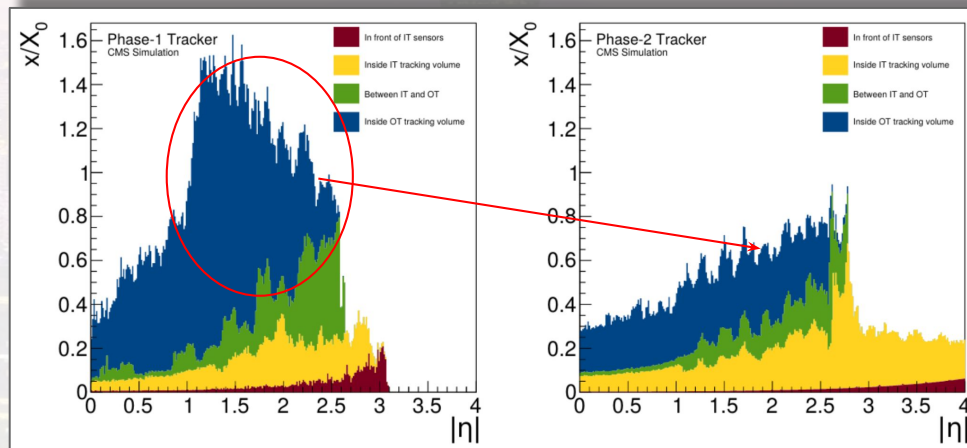
CMS Phase-2 Tracker Upgrade



Tracking performance in Phase-2 Tracker

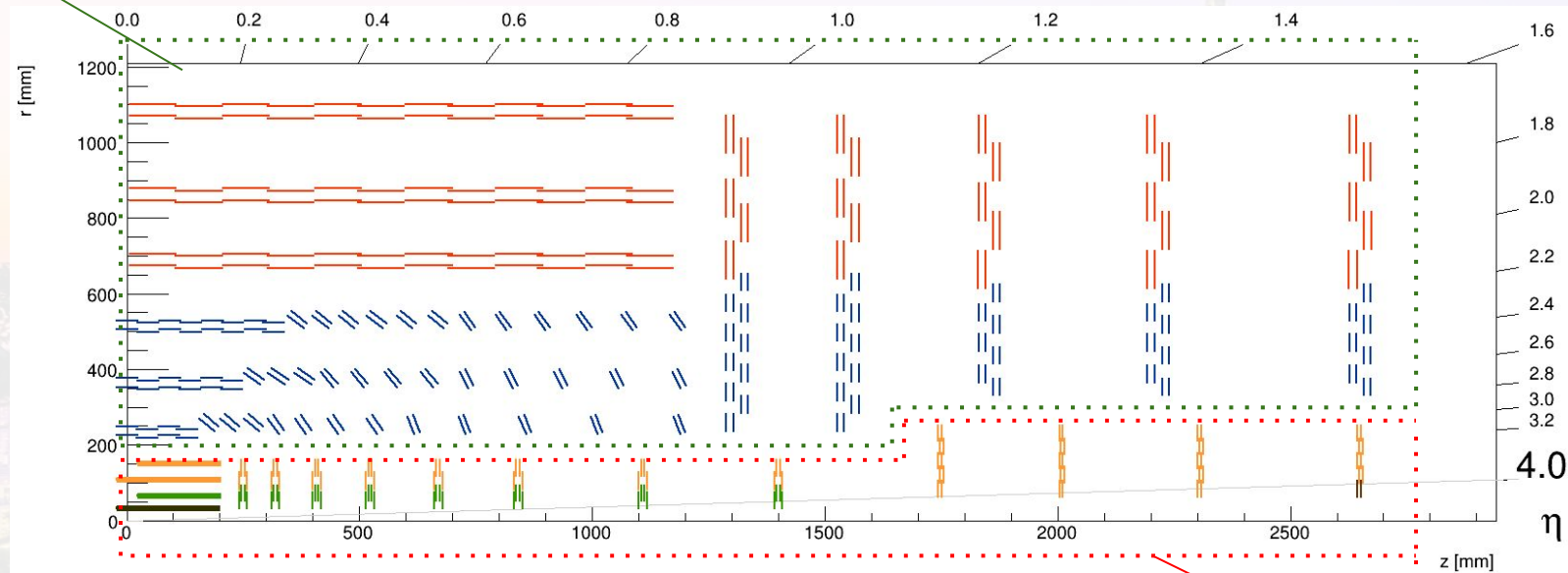
Significant reduction in material budget in the Outer Tracker region compared to the Phase-1 Tracker

- Capable to deal with hit, track and data rates expected for $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$
- **Increased radiation-tolerance up to 1 Grad** (fluence of $\sim 2 \times 10^{16} \text{ neq/cm}^2$ in the innermost regions-about an order of magnitude above Phase-1)
- **Increased granularity** ensures efficient reconstruction under extreme pile-up conditions
- Impact parameter resolution improves by about a factor of two compared to Phase-1.
- Tracking extended from $|\eta| \sim 2.5$ to $|\eta| \sim 4$



CMS Phase-2 Tracker Upgrade

Outer Tracker



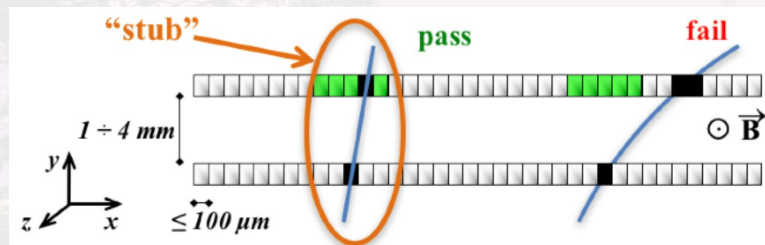
Inner Tracker

Outer Tracker Upgrade

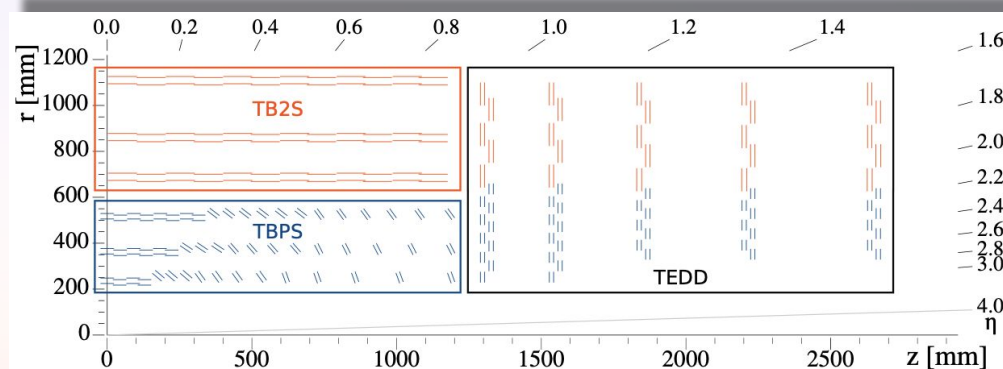
New!
OT will send tracking information to the CMS Level 1 trigger to control the data rates

- Two module types (pT modules):
Pixel-Strip (PS) and Strip-Strip (2S)
- Each module correlates hits from two closely spaced sensors to form “stubs”: tracks with $p_T > 2$ GeV

pT Module Concept

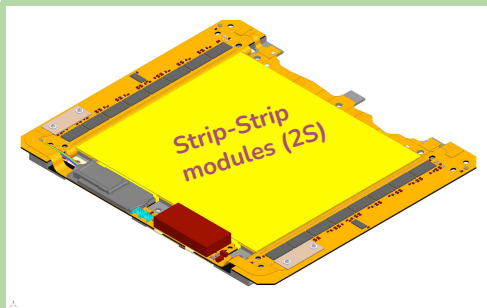


All pT-modules (TBPS, TB2S, TEDD) provide input to the Level-1 trigger at 40 MHz

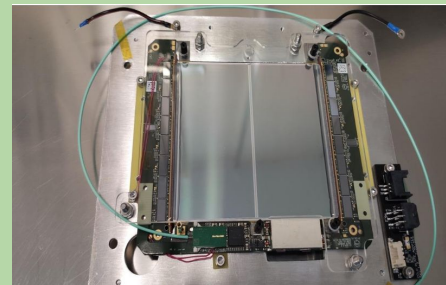


- Tracker Barrel with 2S modules (TB2S)
- Tracker Barrel with PS modules (TBPS)
- Tracker Endcap Double - Discs (TEDD)

Module type and variant	TBPS	TB2S	TEDD	Total per variant	Total per type
2S 1.8 mm	0	4464	2792	7256	7680
4.0 mm	0	0	424	424	
PS 1.6 mm	826	0	0	826	5616
2.6 mm	1462	0	0	1462	
4.0 mm	584	0	2744	3328	
Total	2872	4464	5960	13296	



- **2 different spacings:** 1.8 & 4 mm
- **2 micro strip sensors** with 5 cm x 90 μ m strips
- **Sensor dimension:** 10cm x 10 cm: two columns of 1016 strips

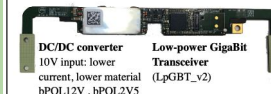


2S Module hybrids

2S Front End Hybrid (x2)

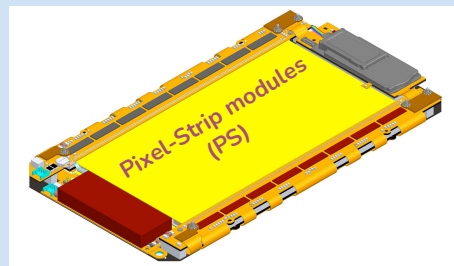


2S Service hybrid

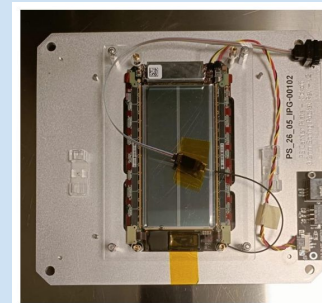


DC/DC converter
10V input: lower
current, lower material
bPOL12V, bPOL2V5

Low-power GigaBit
Transceiver
(LpGBT_v2)



- **3 different spacing:** 1.6mm & 2.6mm & 4mm
- **Strip sensor** (2.5cm x 100 μ m strips) + **Macro Pixel sensor** (1.5 mm x 100 μ m pixels)
- Sensor dimension 5cm x 10 cm (two column of 960 strips + 32x960 pixels)



PS Module hybrids

PS Readout Hybrid



2 variants: 10 / 5G, LpGBT_v2

PS Front End Hybrid (x2)



PS Power Hybrid



DC/DC: bPOL12V, bPOL2V5

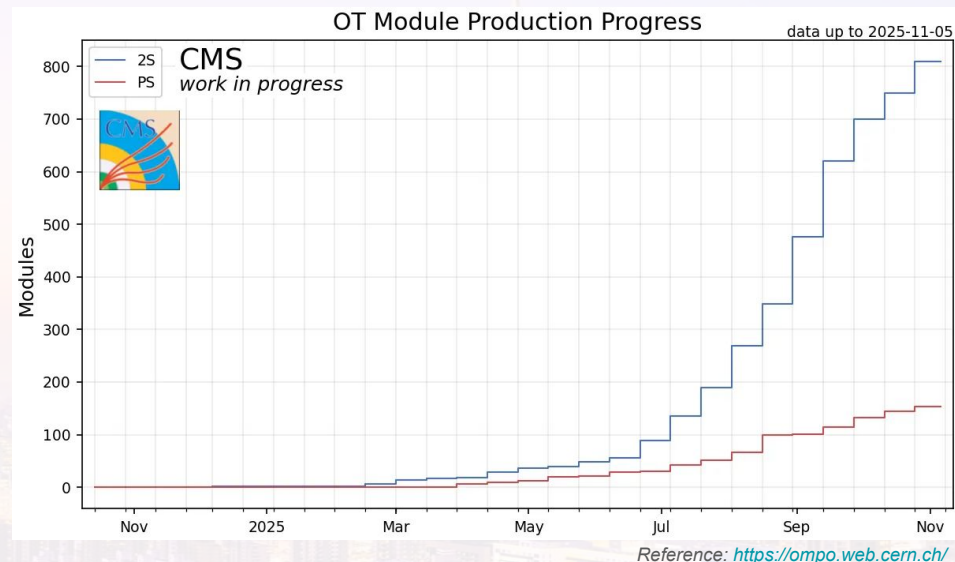
Spacing variants: 1.6mm, 2.6mm, 4.0mm

Module Production Overview

- **PS modules:** Production at 5 centers across Europe and the US
Bari and Perugia (Italy); DESY (Germany); Brown and Purdue (USA)
- **2S modules:** Production at 7 centers across Europe, US, India, and Pakistan
(RWTH Aachen, KIT (Germany); UCLouvain/VUB (Belgium); Brown, Purdue (USA); NISER (India); NCP (Pakistan)

Production Strategy

- Transition from sequential (pipeline) assembly → to parallelized module assembly
- Production rates increasing as lines mature
- **2S production scaled up in June;** PS throughput currently limited by Front-End Hybrids (FEHs) availability



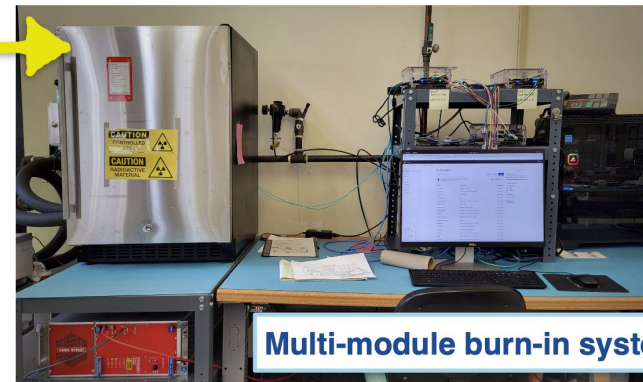
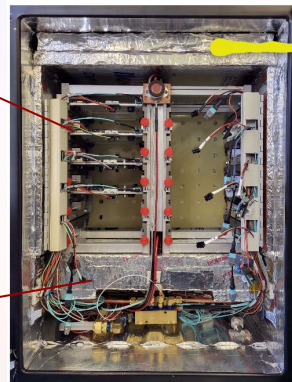
Coordinated monitoring of module production, QC results, and component flow between all assembly centres

- Sensor I-V tests before and after assembly
- Sensor alignment and configuration checks
- Wire bond pull tests and visual inspection
- Noise and functionality tests

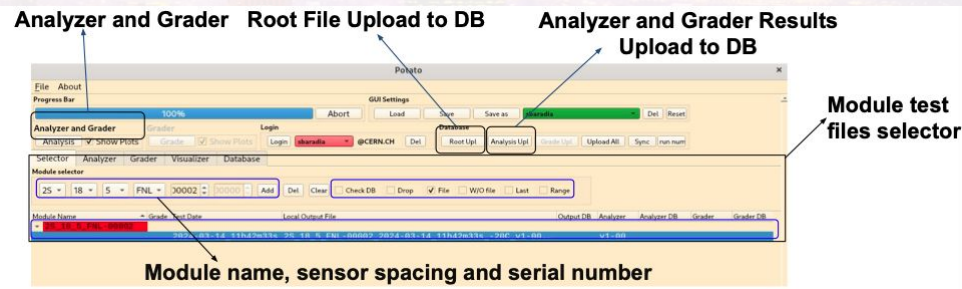
Burn-in Test Setup

- 48 h thermal cycling between +20 °C and -35 °C
- Electrical tests repeated at 5 points during the cycle

Results handling: automated frameworks for analysis, grading, and database uploads are fully implemented.



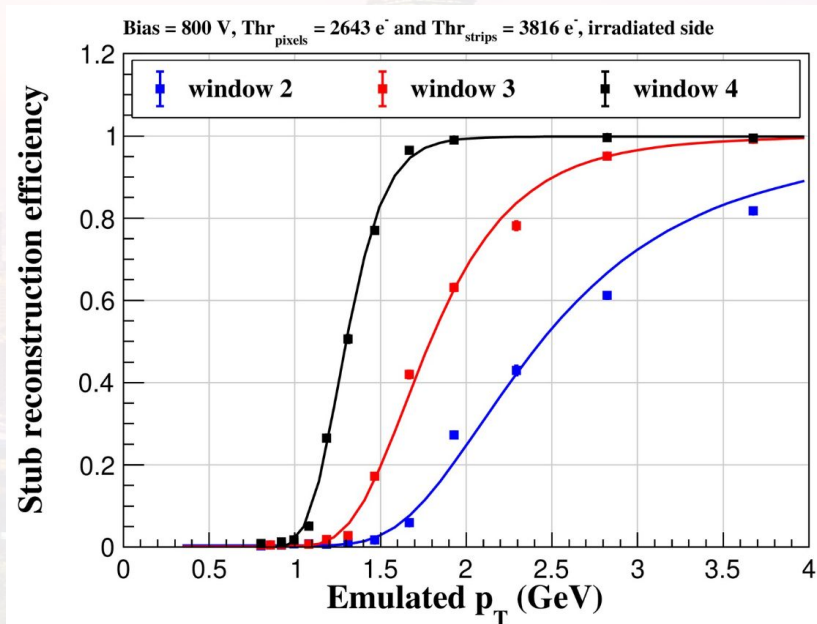
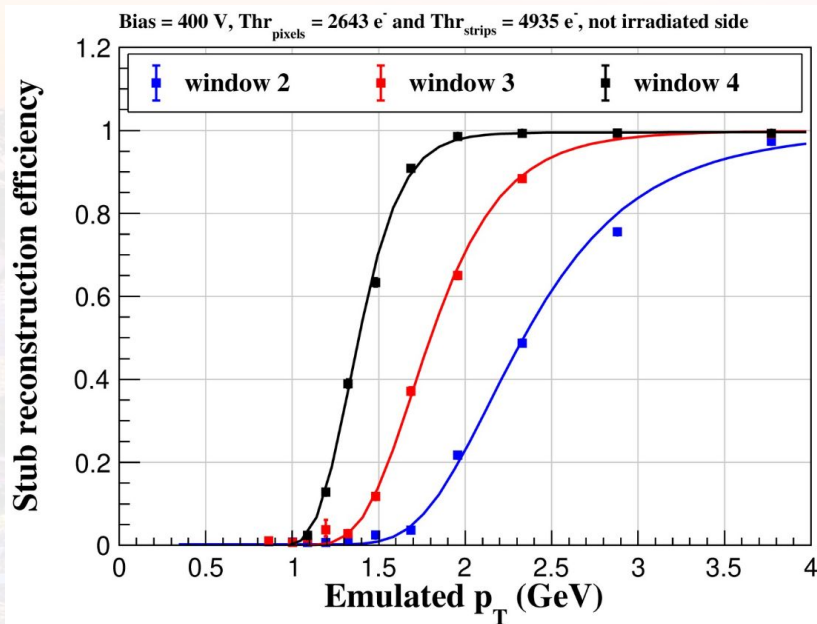
Multi-module burn-in system



POTATO(Phase-2 Outer Tracker Analyzer of Test Outputs)

2024 Fermilab Test Beam

- PS module with 1.6 mm sensor-hybrid spacing was evaluated.
- Tested before and after irradiation to a fluence slightly above HL-LHC end-of-life levels.
- No significant performance degradation observed after irradiation.
- Indicates stable operation margin for HL-LHC conditions.



Outer Tracker Integration - System Tests

Integration Centers: Modules assembled into test ladders / planks / rings /
DEEs for validation → Results stable

2S Ladders (TB2S, prototype):

Mechanical & thermal integrity validated on test ladders;
Electrical performance consistent with single-module results
across temperatures.

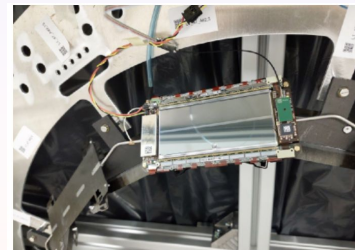
PS Ring and Plank (TBPS):

Noise tested at room and cold;
Ground connection scheme under evaluation.

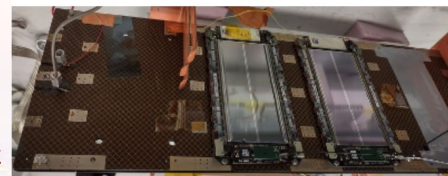
TEDD Sector Prototype:

Module mounting, service routing, and tooling successfully
demonstrated;
No significant noise increase after module installation.

TBPS Ring



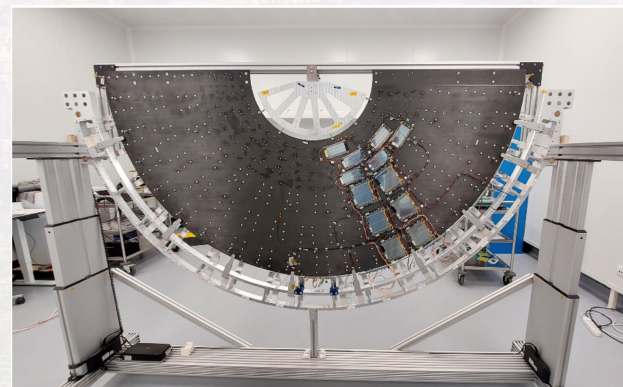
TBPS Plank



TB2S Ladder



TEDD DEE



Inner Tracker Upgrade

Tracker Barrel PiXel (TBPX)

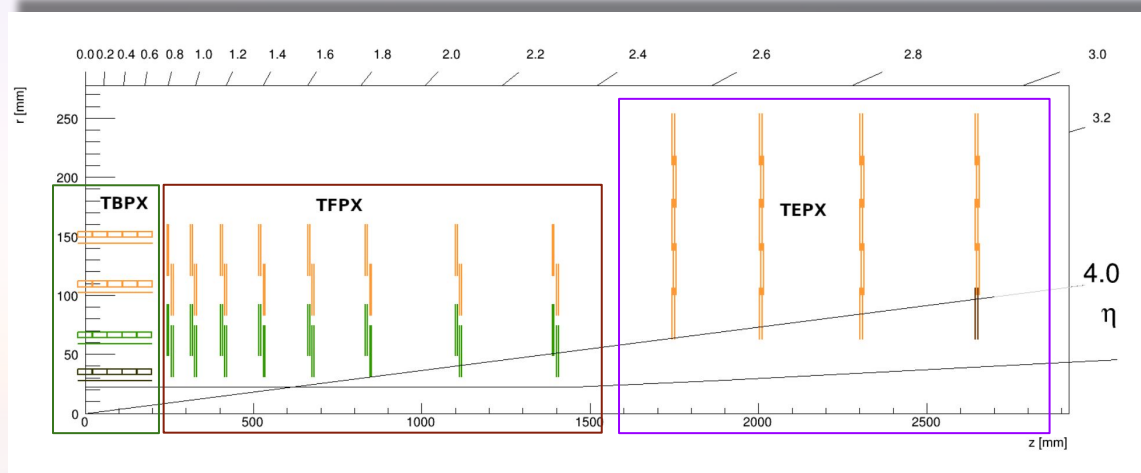
- 4 layers
- 756 modules
- Innermost layer $\rightarrow$ 3D modules (108 modules)

Tracker Forward PiXel (TFPX)

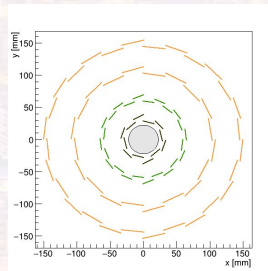
- 8 small double-disks on each side
- 1728 modules

Tracker Endcap PiXel (TEPX)

- 4 large double-disks on each side
- 1408 modules
- Will be used for tracking and luminosity measurements
- Ring 1 of Disk 4 $\rightarrow$ Fully used for luminosity measurements only

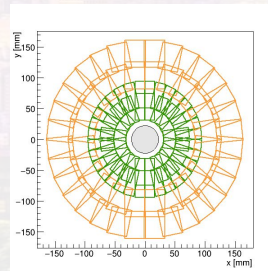


3D; Dual; Quad



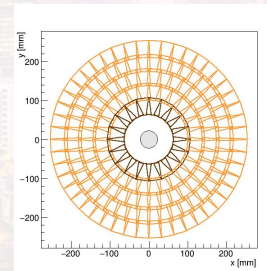
TBPX: 4 layers
4/5 modules per ladder

Dual; Quad

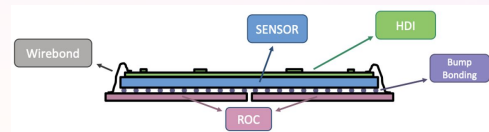


TFPX: 8 disks/end
4 rings/disk

D4R1; Quad



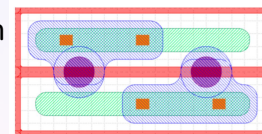
TEPX: 4 disks/end
5 rings/disk



Planar sensors: $25 \times 100 \mu\text{m}^2$ pixels and $150 \mu\text{m}$ thick

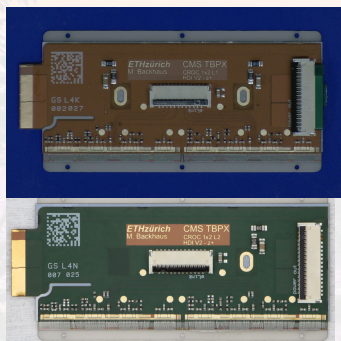
3D sensors: $25 \times 100 \mu\text{m}^2$ pixels, $150 \mu\text{m}$ thick, n^+ readout columns ($5\text{--}8 \mu\text{m}$ diameter, $115\text{--}130 \mu\text{m}$ length), enhanced radiation tolerance and lower depletion voltage

$100 \times 25 \mu\text{m}^2$

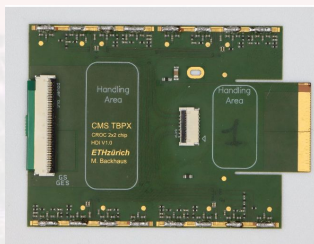


CROC readout chip (CMOS 65 nm, RD53): $50 \times 50 \mu\text{m}^2$ pixels, 3.2 GHz/cm^2 hit rate, radiation-hard up to 1 Grad, Shunt-LDO for serial powering

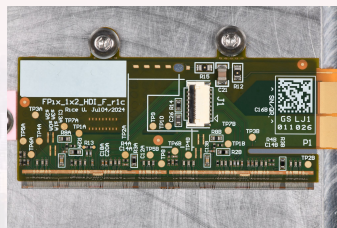
TBPX 1x2



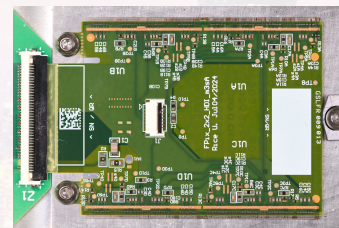
TBPX 2x2



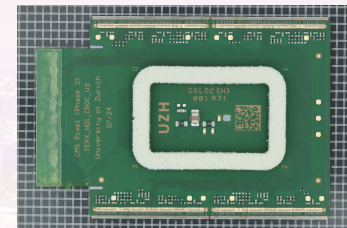
TFPX 1x2



TFPX 2x2



TEPX 2x2



TBPX Modules

- 3D Dual (2 ROCs and 2 sensors)
- Planar Dual (2 ROCs and 1 sensor)
- Planar Quad (4 ROCs and 1 sensor)

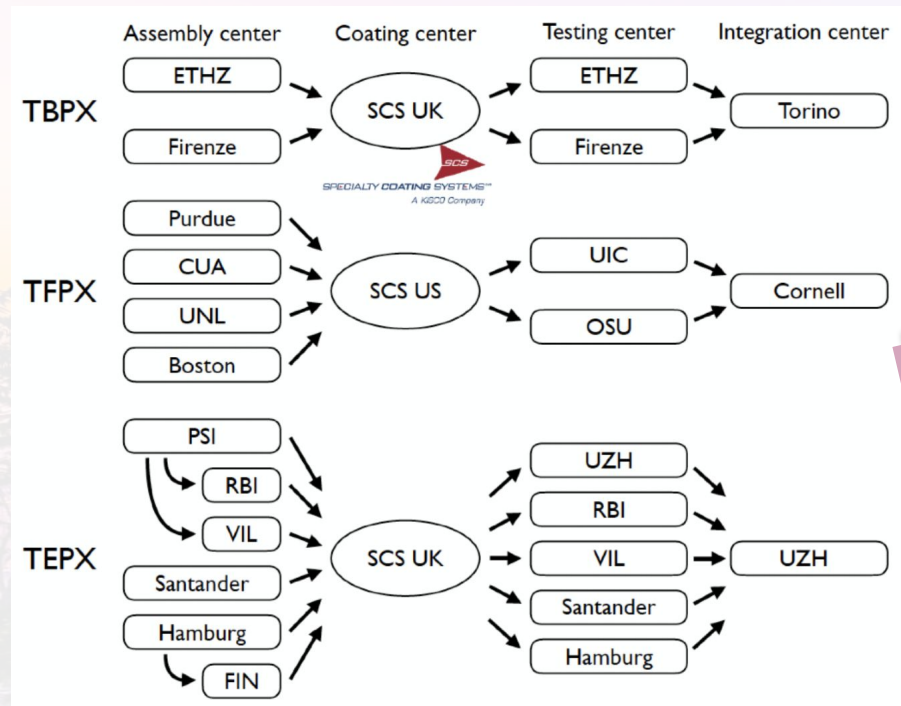
TFPX Modules

- Planar Dual
- Planar Quad

TEPX Modules

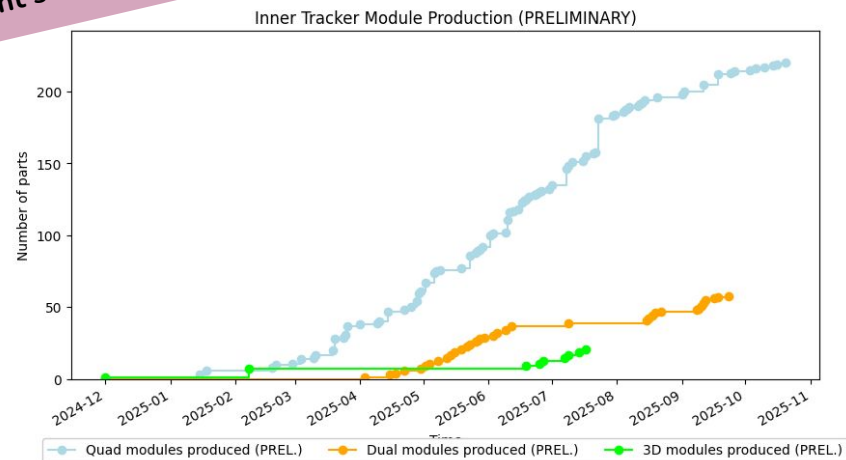
- Planar Quad

Inner Tracker Module Production Status



- Module assembly and testing distributed > 10 institutes
- In total 3892 modules required for installation in CMS. More than 6000 modules are planned
- Currently in pre-production -> production will be launched soon

Current status of production

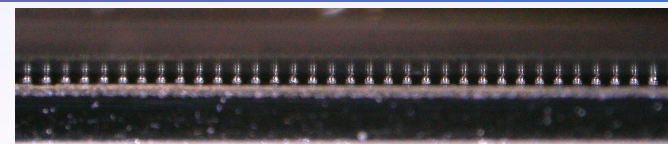


Poster by Chin-Chia Kuo

Details of IT module production and QC workflow:
[CMS Phase-2 Inner Tracker for the HL-LHC Upgrade](#)

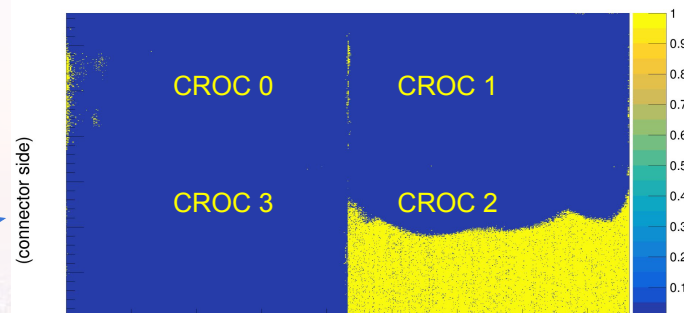
Electrical tests and Visual inspection during assembly

- **SLDO tests** (input, digital and analogue voltages of ROC)
- **Sensor I/V curves**
- **Threshold tuning and Pixel scans** (dead & inactive pixels)
- **Bump connectivity** -> Crosstalk measurements
- **Thermal cycling (BURN-IN Test)**: At least 10 thermal cycles within a temperature range of -35°C to $+40^{\circ}\text{C}$.



Microscope image of bump bonds

confirmed broken bumps for module P1007

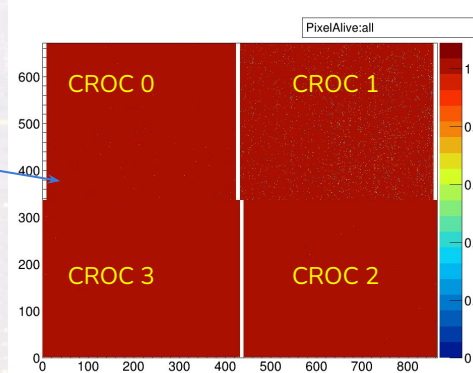


(connector side)

Major issues observed and under investigation:

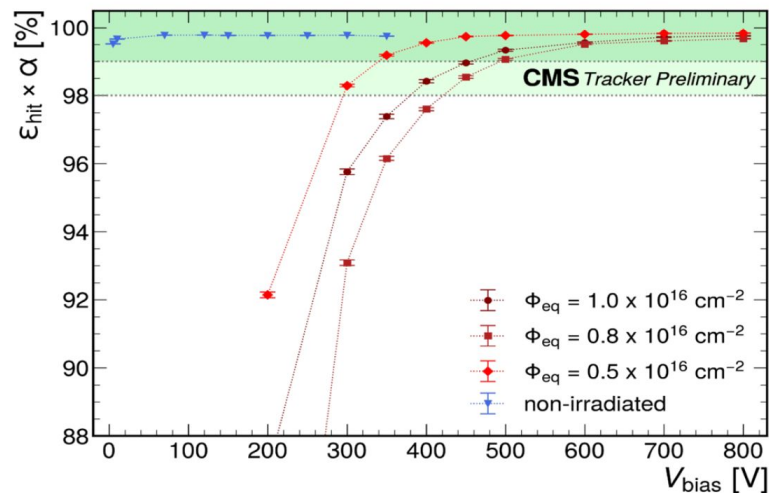
- Broken bump-bonds (non optimal bonding jigs)
- Core column issues

Coated modules are currently undergoing full performance QC to evaluate their quality



QC frameworks for automated testing, grading, and database integration are established and under further development

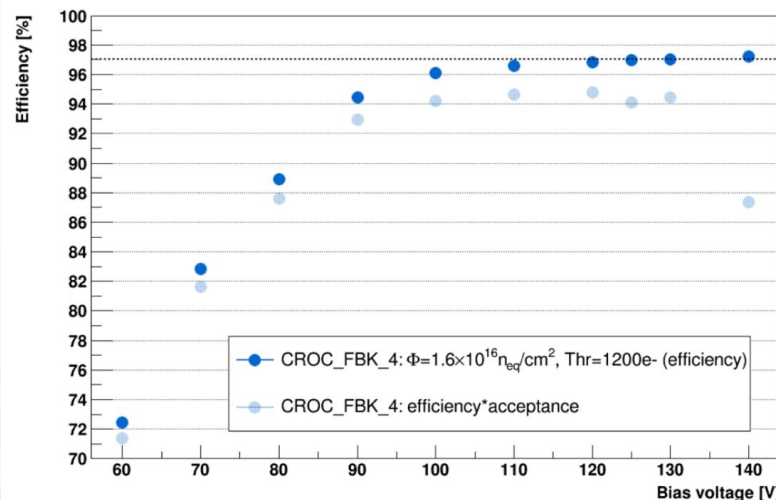
$$\text{Acceptance: } \alpha = 1 - \frac{N_{\text{masked pixels}}}{N_{\text{total pixels}}}$$



Planar Sensors

- Fluence: from $0.5 \times 10^{16} \text{ neq/cm}^2$ to $1 \times 10^{16} \text{ neq/cm}^2$
- Efficiency > 99% @ 600 V (within requirements)

$$\text{Efficiency: } \epsilon_{\text{hit}} = \frac{N_{\text{observed tracks}}}{N_{\text{total tracks}}}$$



3D Sensors

[arXiv:2510.13304](https://arxiv.org/abs/2510.13304)

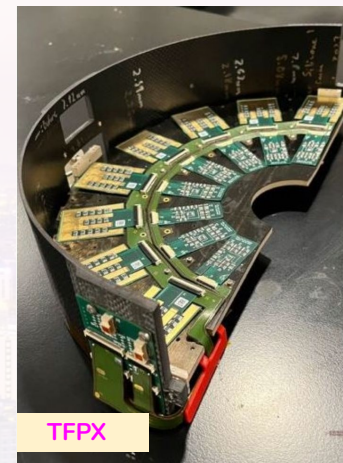
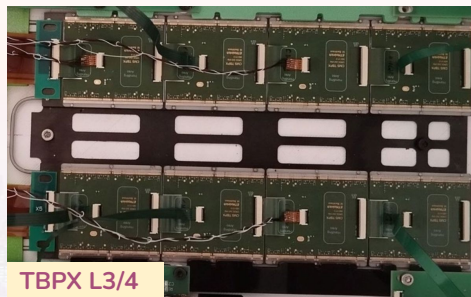
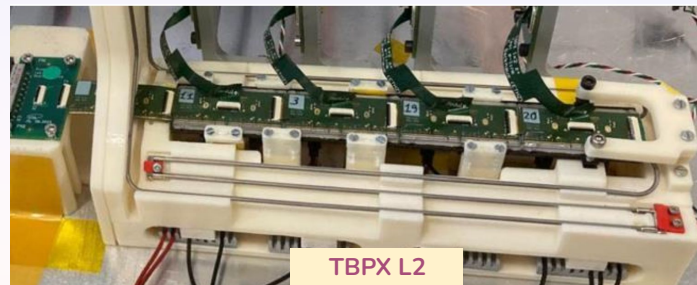
- Fluence: $1.6 \times 10^{16} \text{ neq/cm}^2$ (replacement of layer-1 foreseen after 6 years of operation)
- Efficiency > 96% @ 110 V for normal incidence (within requirements*)

* 3Ds have geometrical inefficiency for normal incidence, because of the columns

Inner Tracker Integration - System Tests

Four different setups with final integration structures:

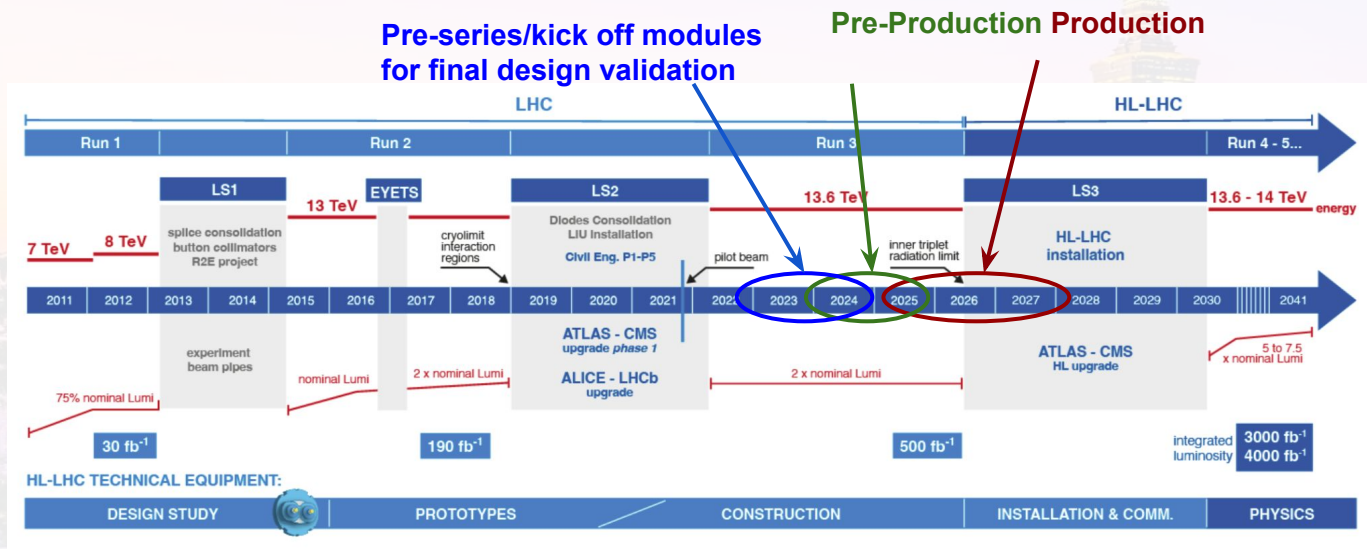
- ✓ **TBPX** L2 and L3/4
- ✓ **TFPX** disk
- ✓ **TEPX** disk



Major studies progressing:

- Thermal studies and simulations validation
- Mechanical studies
- LV distribution tests with serial power configuration
- HV distribution and grounding studies
- Full readout chain validation

- The CMS Tracker will be fully replaced for the HL-LHC, featuring:
Extended forward acceptance ($|\eta| < 4$), higher hit-rate capability, increased radiation tolerance, reduced material budget and track information available at Level-1 trigger

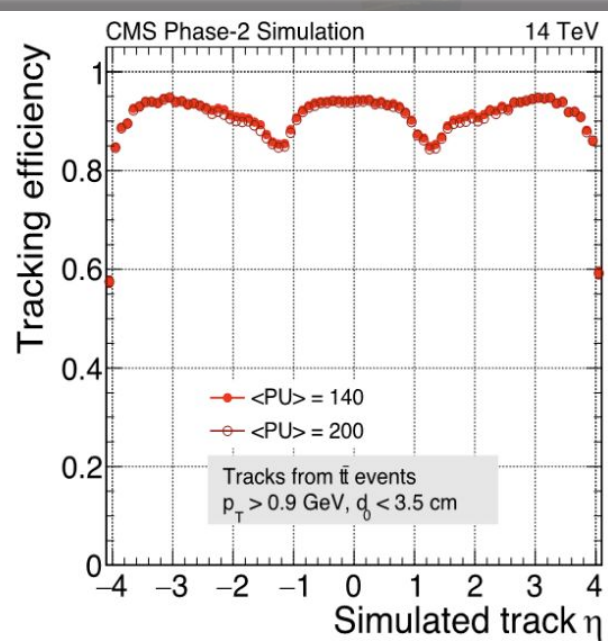
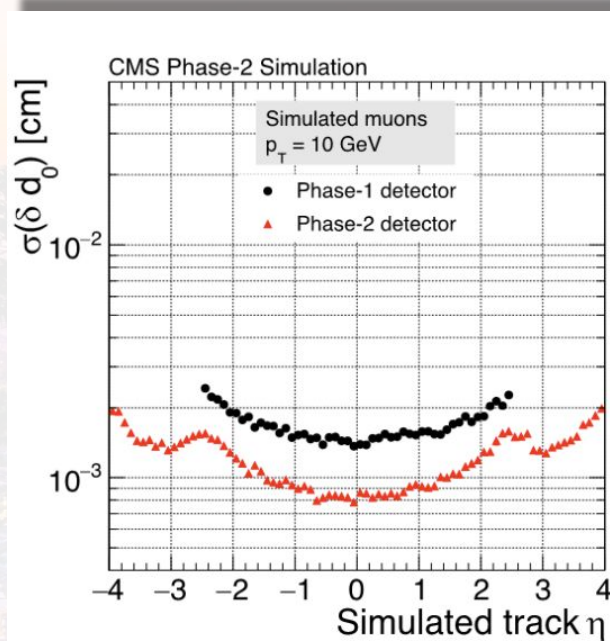


- Module production is underway for both Inner and Outer Tracker, with QA/QC workflows established and supporting scale-up production.
- Support systems (mechanical structures, powering, cooling) are in place and undergoing validation tests.
- System integration tests are ongoing**, and the first assembled structural units are being built and evaluated as production ramps up.

Thank You

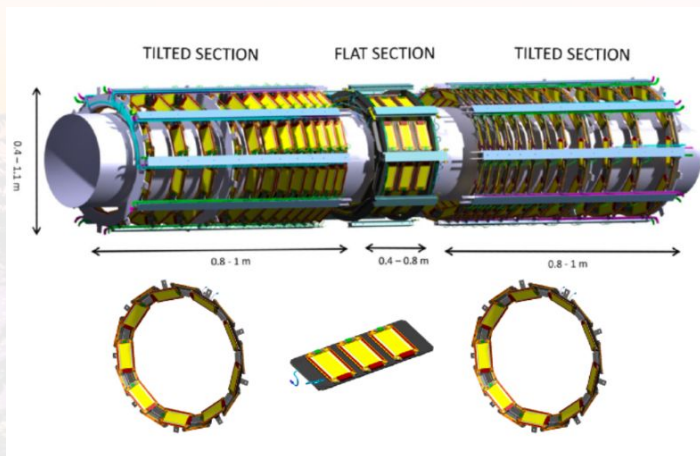
Tracking performance in Phase-2 Tracker

- Impact parameter resolution improves by about a factor of 2 compared to Phase-1.
- Tracking extended up to $|\eta| < 4$ with resolution $< 200 \mu\text{m}$.
- High Tracking efficiency ($> 85\%$) even at 200 pile-up



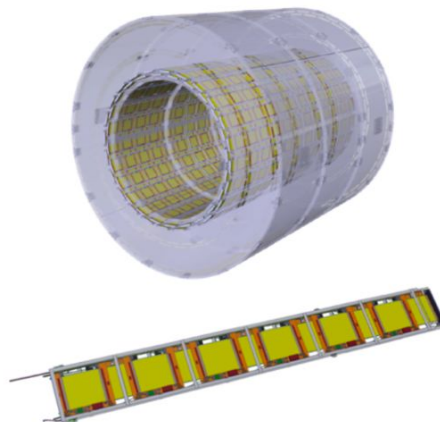
TBPS

- Planks & Rings



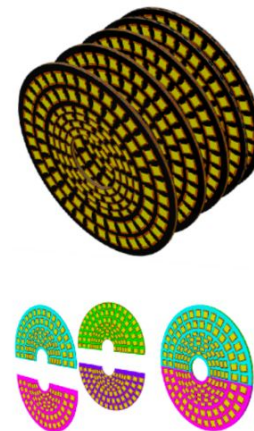
TB2S

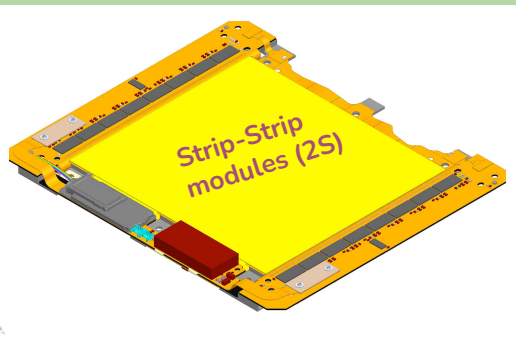
- Ladders -> Cylindrical layers



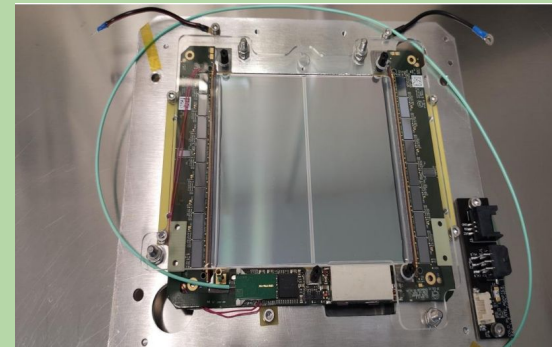
TEDD

- Double disks with dees (D shaped parts)



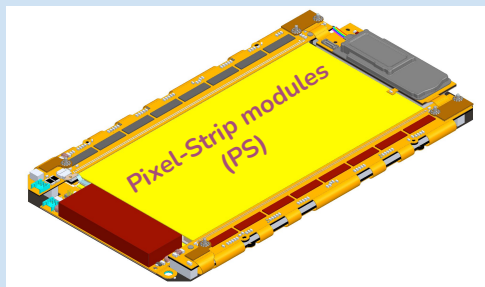


- **2 different spacings:** 1.8 & 4 mm
- **2 micro strip sensors** with 5 cm x 90 μ m strips
- **Sensor dimension:** 10cm x 10 cm: two columns of 1016 strips

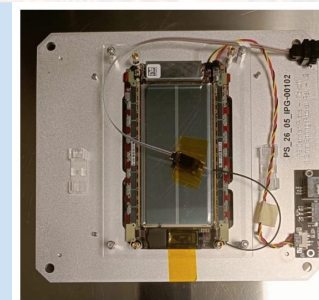


Front-end Electronics

- **CBC** – CMS Binary Chip (130 nm): Sensor readout and stub finding in 2S modules
- **SSA** – Short-Strip ASIC (65 nm): Readout of the short-strip sensor in PS modules
- **MPA** – Macro-Pixel ASIC (65 nm): Stub finding on the macro-pixel sensor in PS modules
- **CIC** – Concentrator Integrated Circuit (65 nm): Aggregates and serialises data from all modules for off-detector transmission



- **3 different spacing:** 1.6mm & 2.6mm & 4mm
- **Strip sensor** (2.5cm x 100 μ m strips) + **Macro Pixel sensor** (1.5 mm x 100 μ m pixels)
- **Sensor dimension** 5cm x 10 cm (two column of 960 strips + 32x960 pixels)



The Pixel-strip (PS) module

Strip sensors

strip: $\sim 2.4 \text{ cm} \times 100 \mu\text{m}$
module area: $\sim 10 \times 5 \text{ cm}^2$

Short Strip ASIC (SSA)
strip sensors readout chip

DC/DC converter
10V input: lower
current, lower
material

LpGBT

VTRx+
5 or 10 Gb/s optical readout

CIC (On the back)

Pixel sensor + Macro Pixel ASIC (MPA) = MaPSA
(on the back side)

$\sim 2 \times 45 \text{ cm}^2$ active area
2 $\times$ 960 strips: $\sim 2.4 \text{ cm} \times 100 \mu\text{m}$
32 $\times$ 960 macro-pixels: $\sim 1.5 \text{ mm} \times 100 \mu\text{m}$

The Strip-strip (2S) module

Concentrator Integrated Circuit (CIC)

Aggregates and serialises
the data from the readout chips

DC/DC converter
10V input: lower
current, lower
material

Low-power GigaBit Transceiver (LpGBT)
CERN development for
data transfer
at HL-LHC

VTRx+ electrical-optical converter
5Gb/s optical readout

Strip sensors

$\sim 2 \times 90 \text{ cm}^2$ active area
2 $\times$ 1016 strips: $\sim 5 \text{ cm} \times 90 \mu\text{m}$
2 $\times$ 1016 strips: $\sim 5 \text{ cm} \times 90 \mu\text{m}$

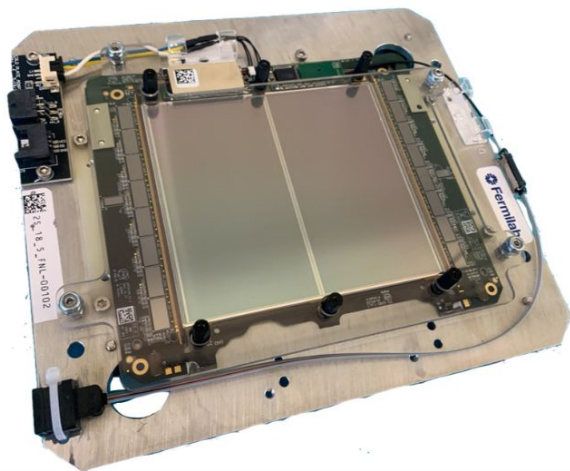
CMS Binary Chip (CBC)
Strip sensors readout

irradiation hardness: $5 \times 10^{14} \text{ nEq/cm}^2$

2S Module Assembly

- 7608 2S + spares needed
- 7 production centers in Europe, US, India and Pakistan

Rotate Left



Service hybrid

Ground balancer

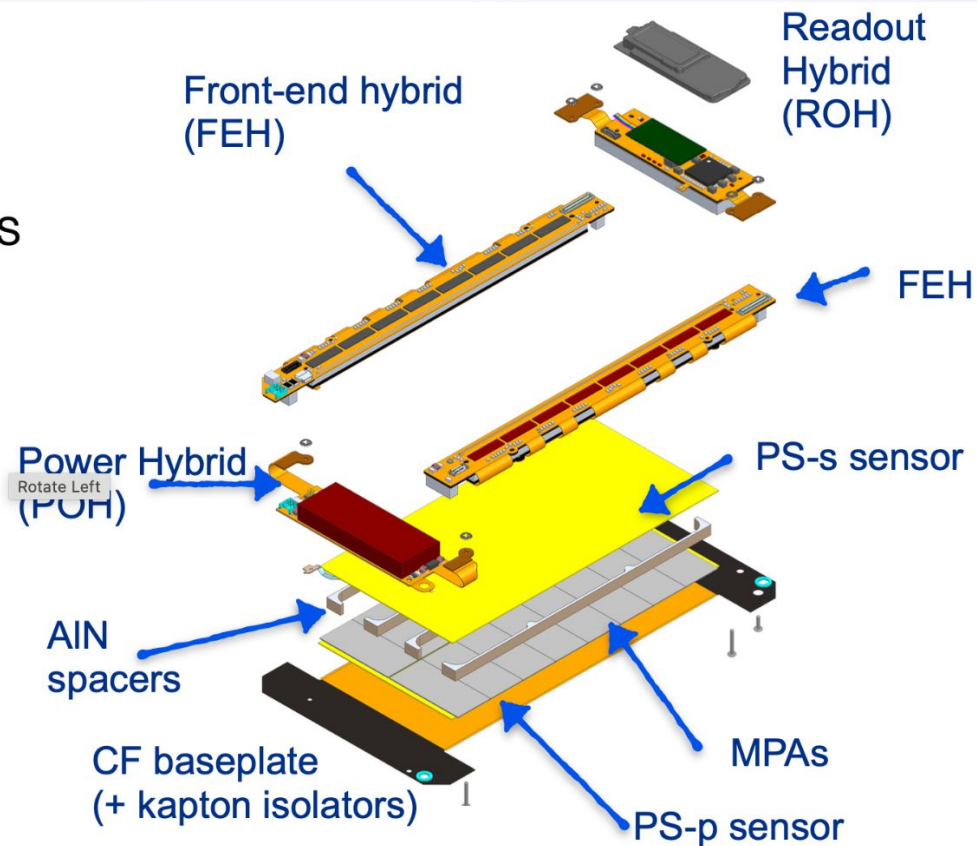
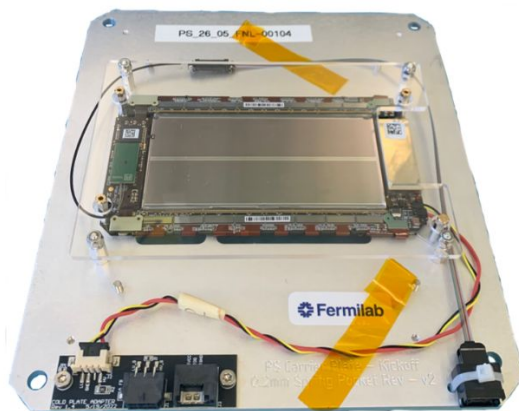
Readout hybrids

Sensors

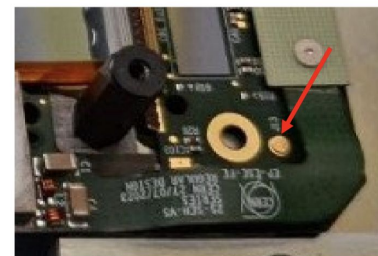
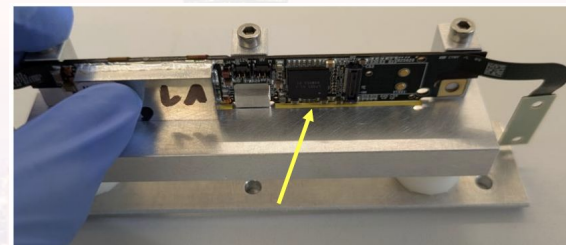
Al-CF main and
stump bridges
(+ kapton isolators)

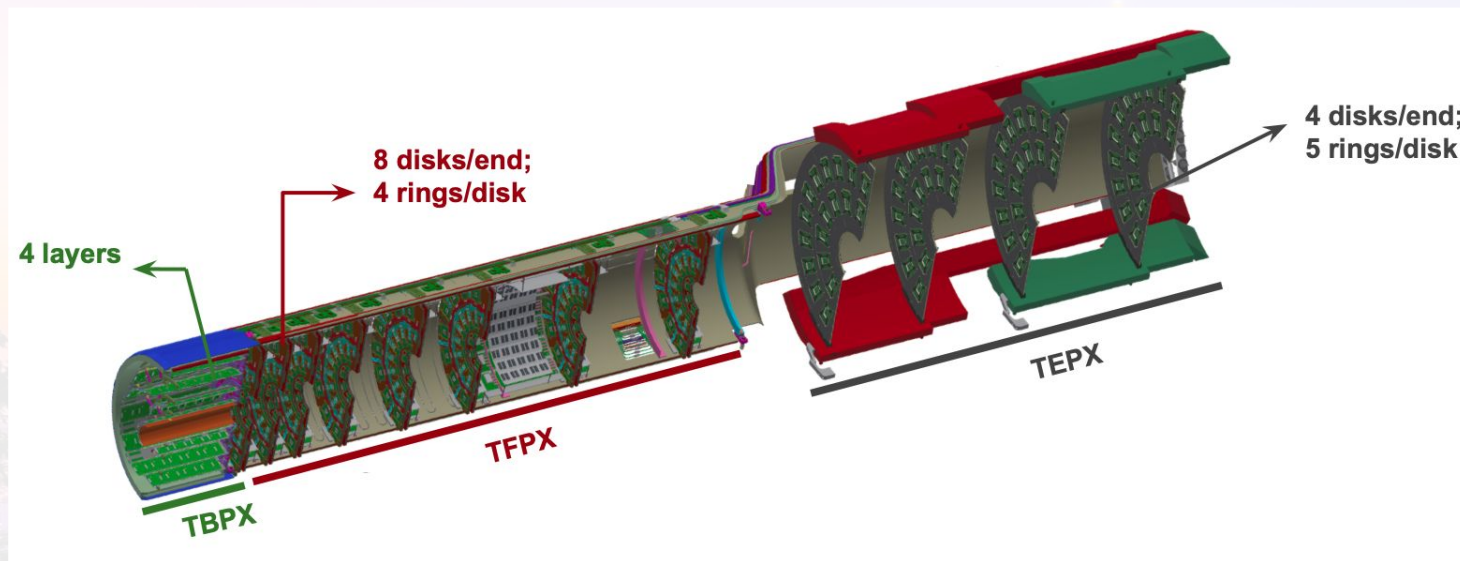
PS Module Assembly

- ▶ 5592 PS + spares needed
- ▶ 5 production centers in Europe and US



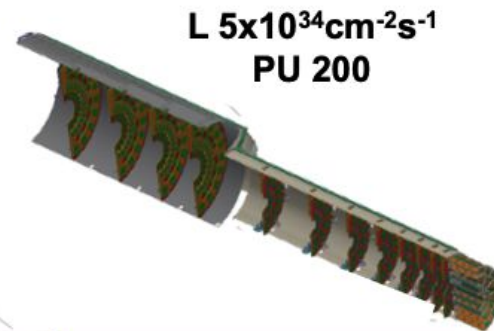
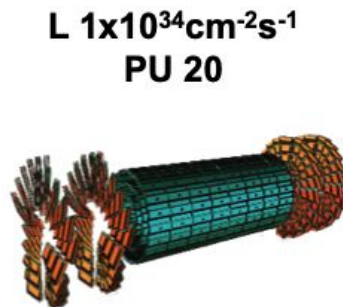
- **Wirebond Pad Cleanliness:** Residue contamination traced to spacer geometry → cleaning workflow improved and new spacer designs under evaluation.
- **1.8 mm 2S High-Voltage Sensitivity:** Small sensor–stiffener spacing caused discharge and dead channels after HV tests.
→ Kapton isolation solution adopted; hybrid gluing + HV tests temporarily paused until fix applied.
- **Grounding Pin Reliability (2S & PS):**
Inconsistent stiffener grounding and degradation after thermal cycling.
→ Standardizing on soldered grounding pins for future and existing modules.





- Light Carbon Fiber structures with embedded cooling pipes
- Flat disk geometry (replaces turbine design of Phase-1)
- Can be extracted for maintenance (during extended technical stops)
- Barrel splits in half @ $z \sim 0$
- Cooling based on evaporative CO₂ ($T = -35^\circ\text{C}$):
 - ✓ TBPX: 1.8 mm outer diameter stainless steel pipes
 - ✓ TFPX: 3.0mm outer diameter titanium pipes
 - ✓ TEPX: 2.3mm outer diameter titanium pipes

Inner Tracker Upgrades



	Phase 0	Phase 1	Phase 2
Mechanics	3 layers+ 4 disks	4 layers + 6 disks	4 layers + 24 disks
Inner radius	4 cm	3 cm	3 cm
Active Si area	1 m ²	1 m ²	5m ²
Channels	66M	124M	2000M
Pixel size	100x150 μm ²	100x150 μm ²	25x100/50x50 μm ²
Radiation tolerance	100 Mrad	300 Mrad	1000 Mrad

Inner Tracker Module Assembly

TBPX:

- ✓ Assembly with dedicated jigs

TFPX:

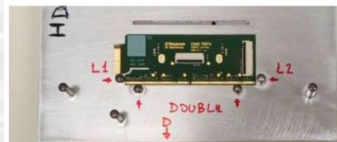
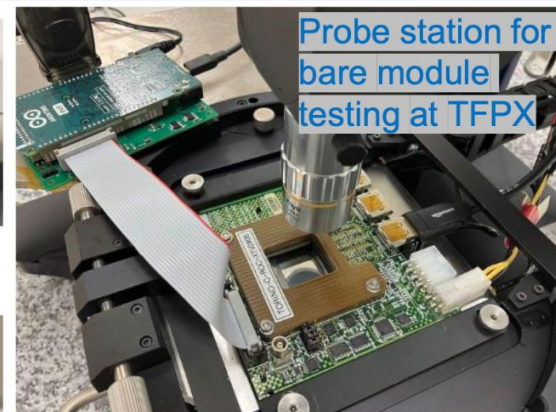
- ✓ Assembly with gantry

TEPX:

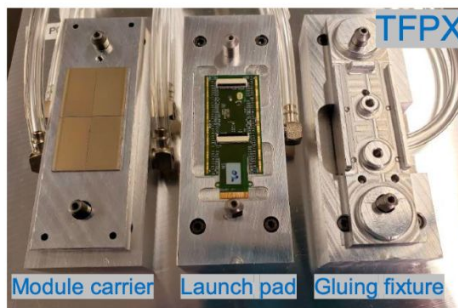
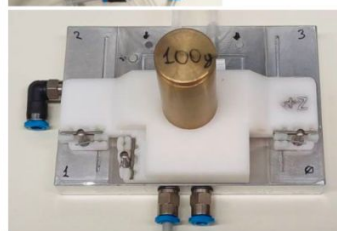
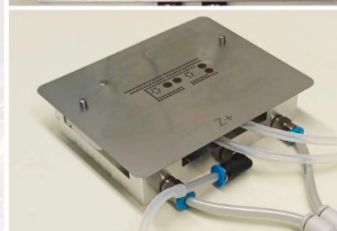
- ✓ Assembly with robotic arm



3Ds bare module HV testing tool



TBPX

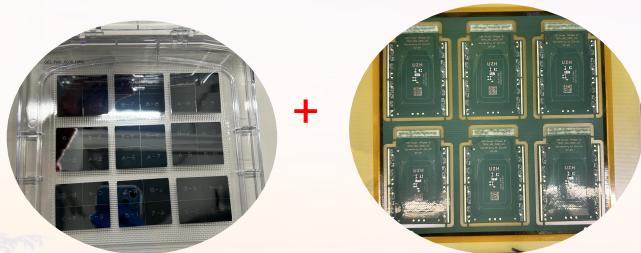


TEPX



TEPX Module Assembly

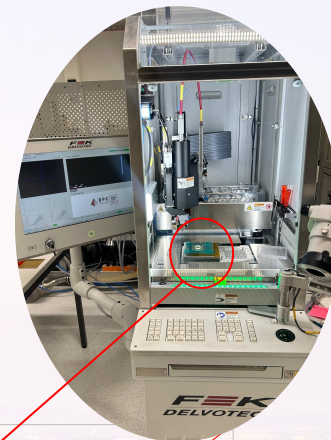
Bare modules (sensor bump bonded to the chips) and HDIs arrive at PSI



HDIs and Airex frames (for mechanical stability) are glued using the a robotic arm



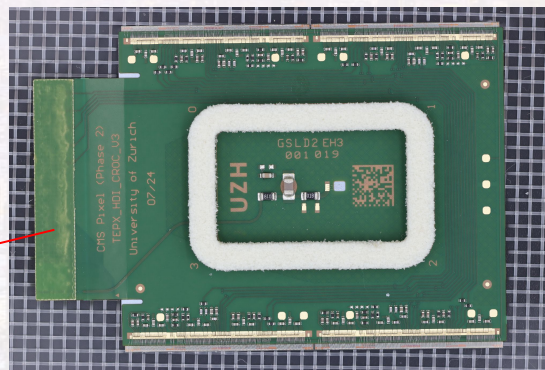
Modules are wire bonded



Module undergoes a visual inspection after assembly



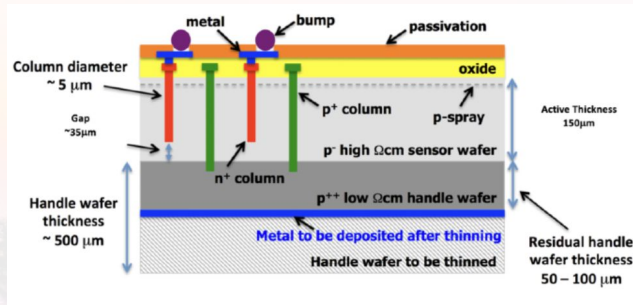
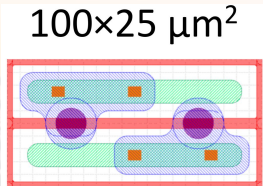
A fully assembled module



Inner Tracker Sensors and Readout Chip

Planar Sensors:

- $25 \times 100 \mu\text{m}^2$ per $150 \mu\text{m}$ active thickness
- Hit efficiency $>99\%$ after $2 \times 10^{16} \text{ neq/cm}^2$

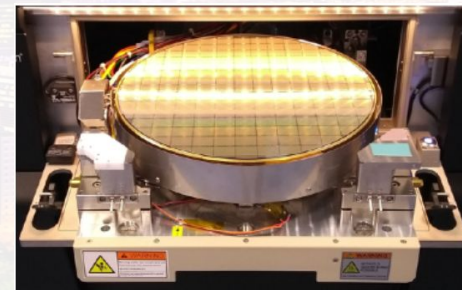
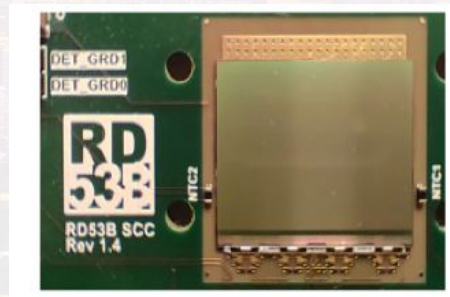


3D Sensors:

- Better performances for radiation (than planar)
- Lower depletion voltage
- Hit efficiency $> 98\%$ after $1.8 \times 10^{16} \text{ neq/cm}^2$

CMS Readout Chip (CROC):

- CROC 65 nm CMOS ASIC developed by joint ATLAS-CMS RD53 Collaboration (pixels: 432×336 ; size $21.6 \times 18.6 \text{ mm}^2$)
- $50 \times 50 \mu\text{m}^2$ cell size
- 3.2 GHz/cm^2 hit rate
- Radiation tolerance up to 1 Grad



Powering scheme:

- Low material budget for a 60 kW detector power
- Modules are grouped in 576 serial power chains → **Serial Powering**
- Up to **11 modules/chain serially powered**
 - Within each module, chips are powered in parallel → on chip shunt-LDO regulators for serial powering
 - HV supply in parallel

Readout scheme:

- Electrical ↔ optical data conversion handled on portcards (not on modules), ~700 total.
- Portcard: 3× lpGBT + VTRx+ and DC-DC converters.
- Up-links: up to 6× E-links @ 1.28 Gb/s (module → lpGBT).
- Down-link: 1× E-link @ 160 Mb/s (clock + trigger + config).
- Optical fibers: between portcards and the Data, Trigger, and Control (DTC) boards

