Testing and Characterization of Wafer-Scale MAPS Prototypes for the ALICE ITS3 Upgrade

Nicolas Tiltmann

on behalf of the ALICE Collaboration

CERN & University of Münster

The 14th international "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD-14)

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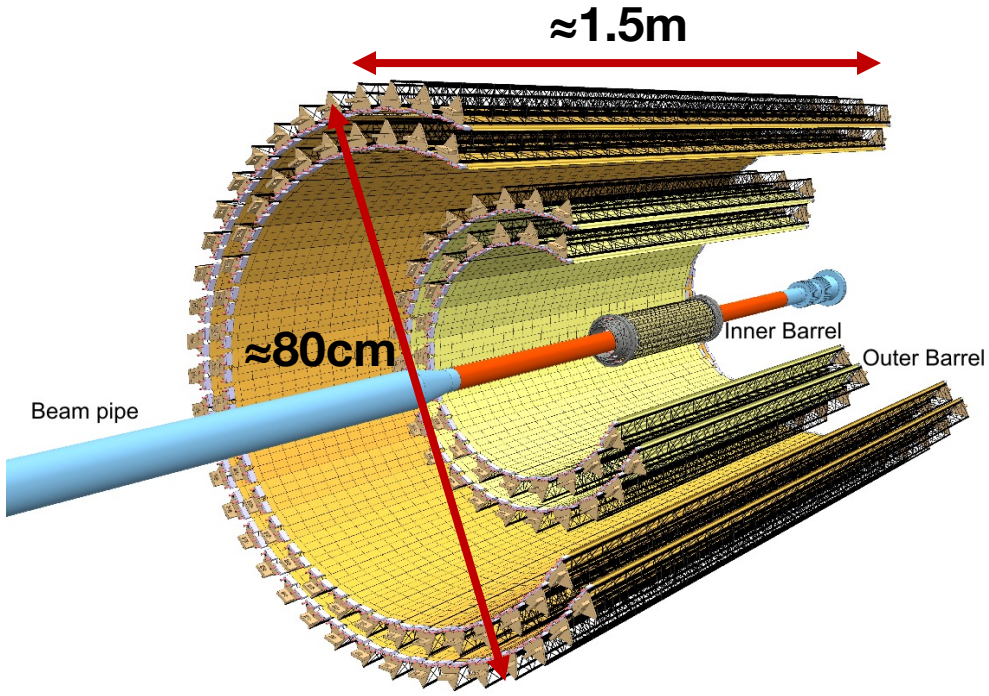
Bundesministerium für Bildung und Forschung

ALICE ITS

ALICE's current innermost tracker:

- Inner Tracking System (ITS) based on custom Monolithic Active Pixel Sensor **ALPIDE**
- Installed: LHC LS2 (2019-2021)
- Instruments ~10m² in 7 layers
- Strong interest in low-momentum particles in ALICE



doi:10.1088/0954-3899/41/8/087002

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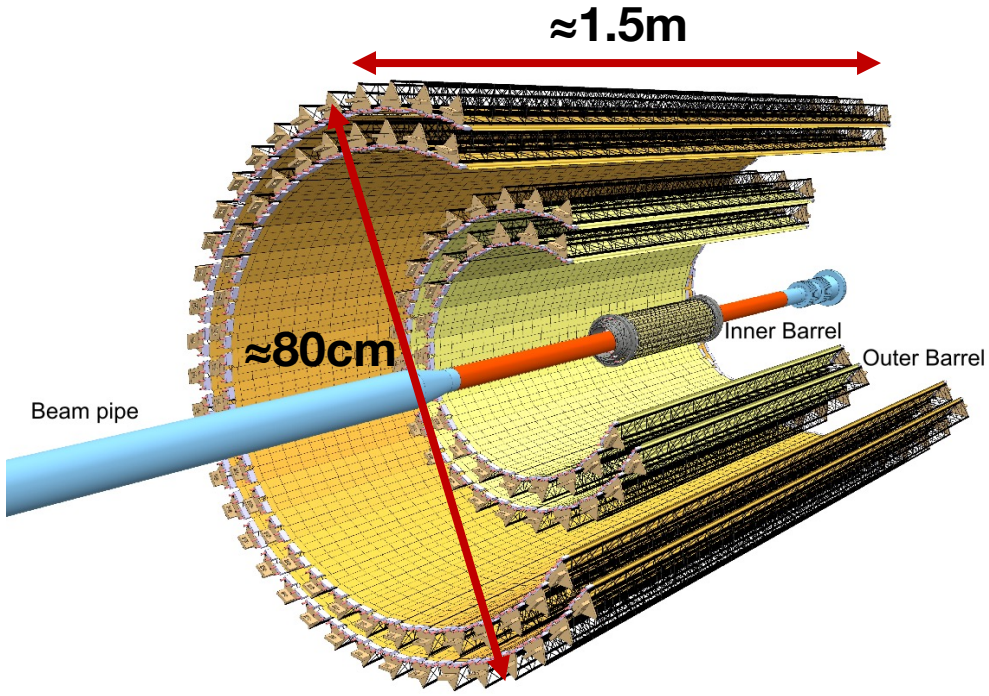

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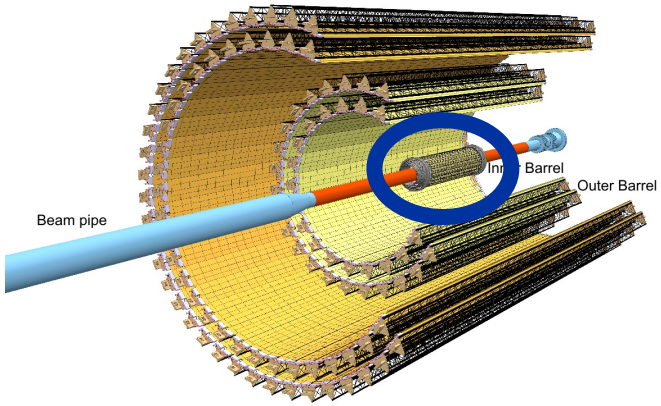
Can we build a detector even thinner and closer to interaction point?

Detector Concept



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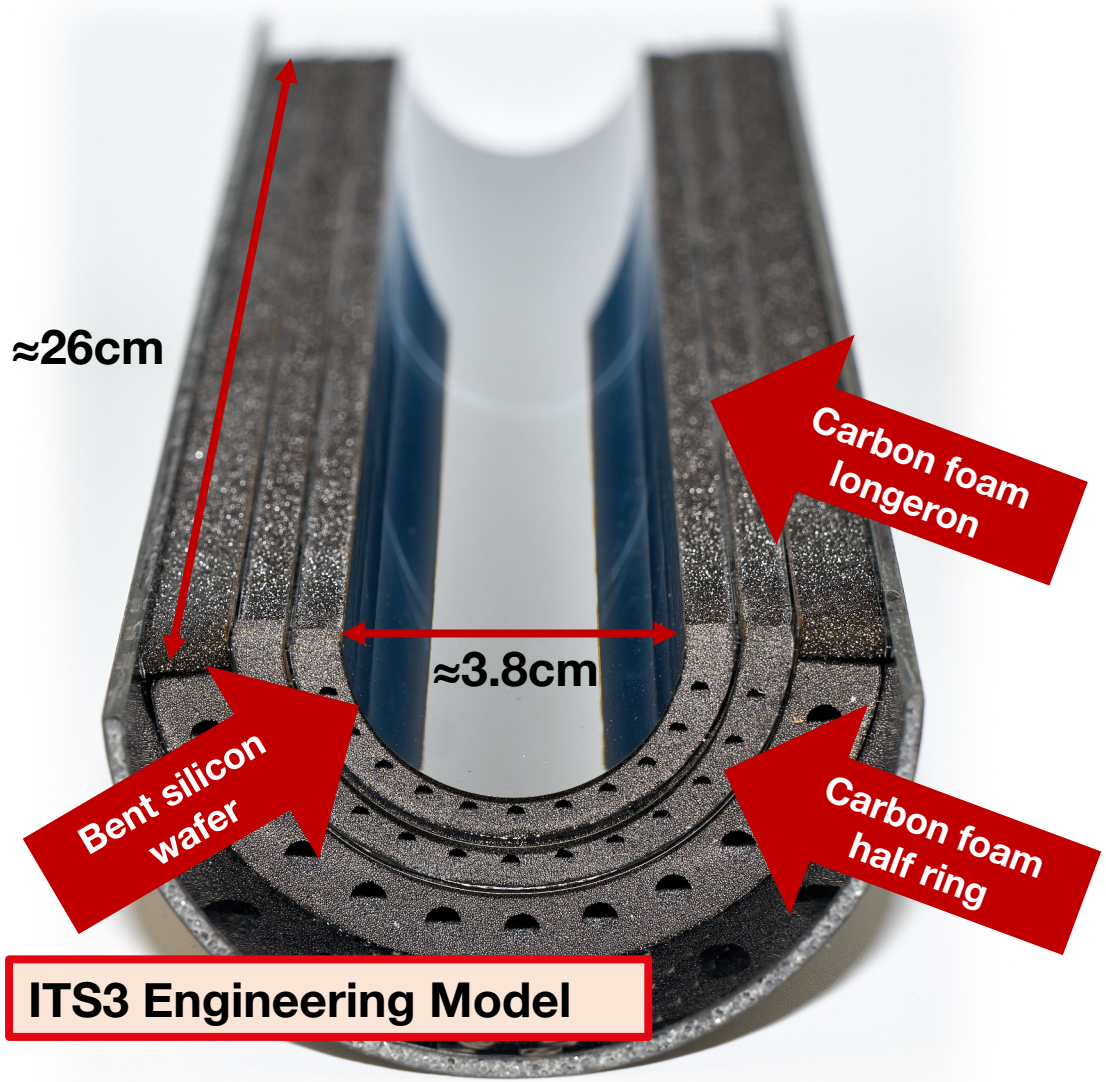
Upcoming Upgrade
LHC LS3 (2026-2030)



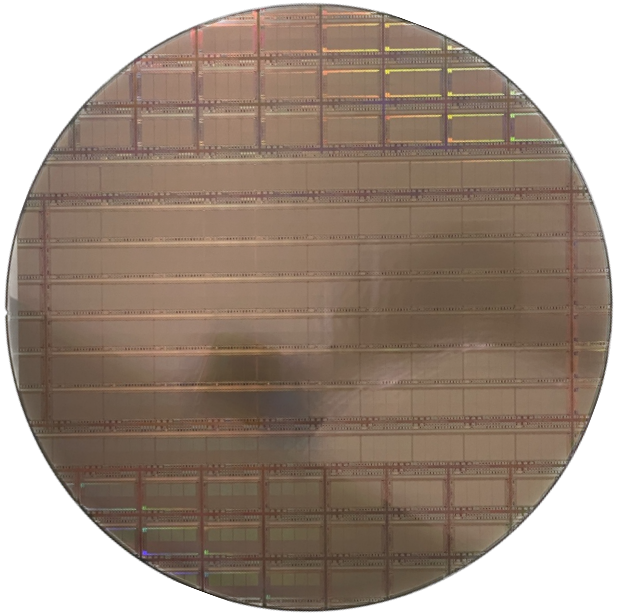
ITS3 Engineering Model

Key Facts

- ➔ Avg. **0.09% X/X_0** per layer (including supports)
- ➔ 50µm silicon thickness
- ➔ Layer 0 at 19mm from interaction point
- ➔ 20.8µm x 22.8µm pixel pitch
- ➔ TID: 400krad
- ➔ NIEL: $4 \cdot 10^{12}$ 1MeV $n_{eq}\,cm^{-2}$

Detector Concept

How to actually fabricate a wafer-sized chip?



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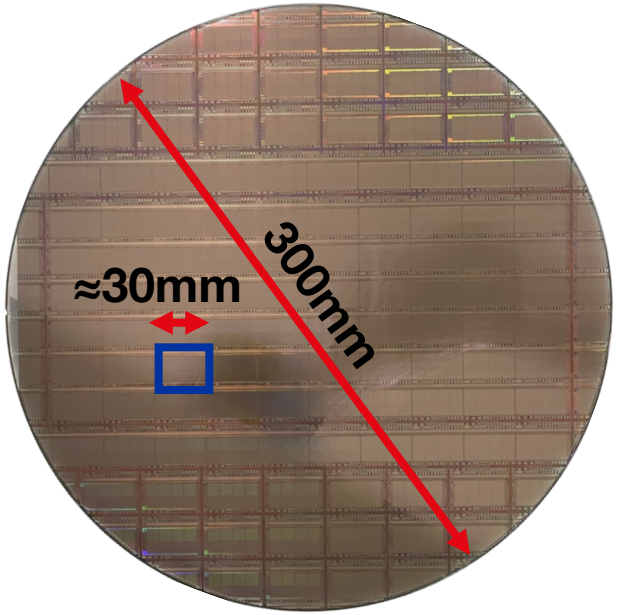
- **Stitching!**



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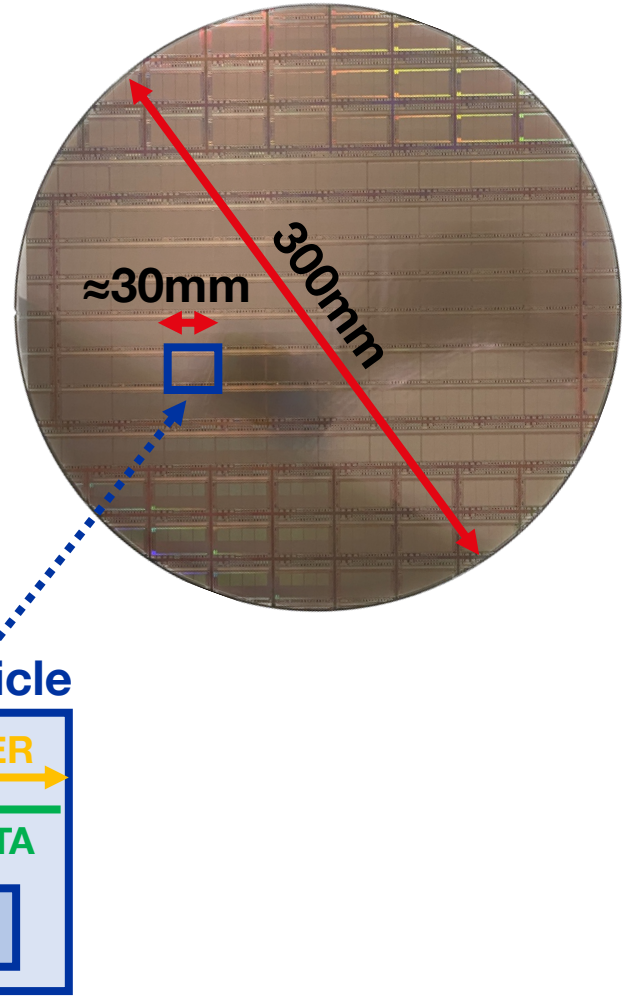

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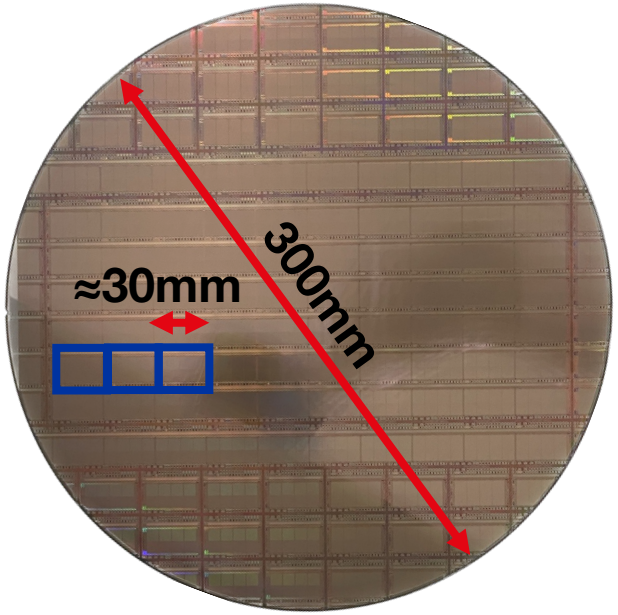

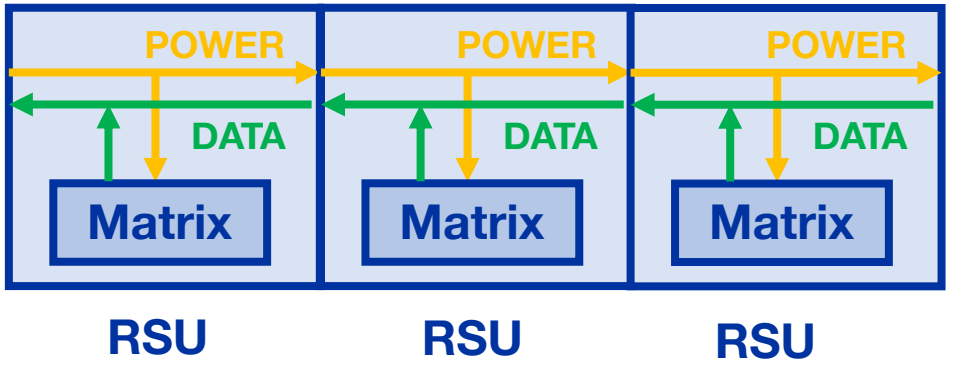

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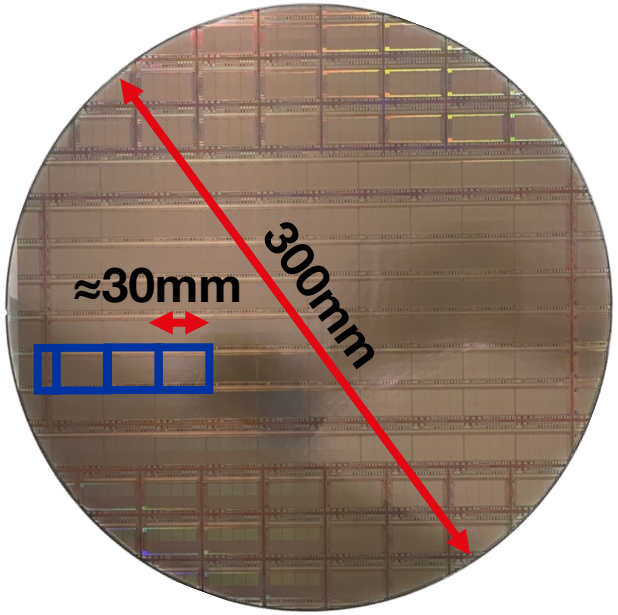
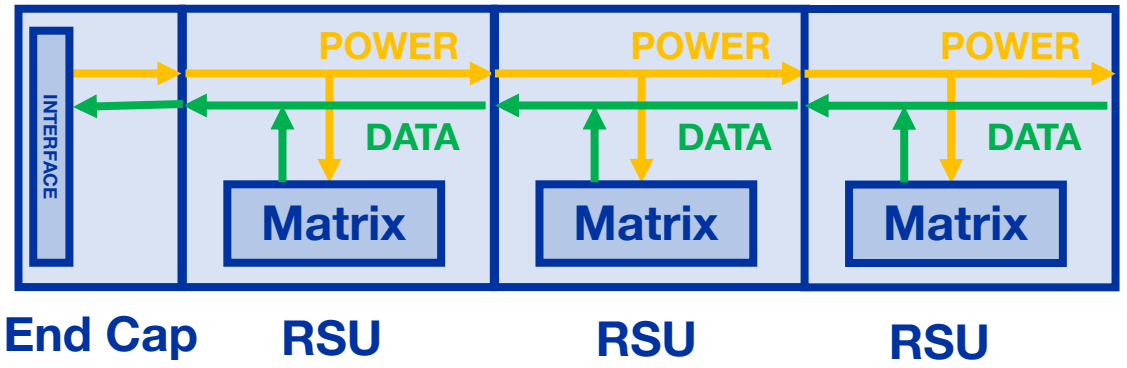
3. Separate reticle designs for end caps



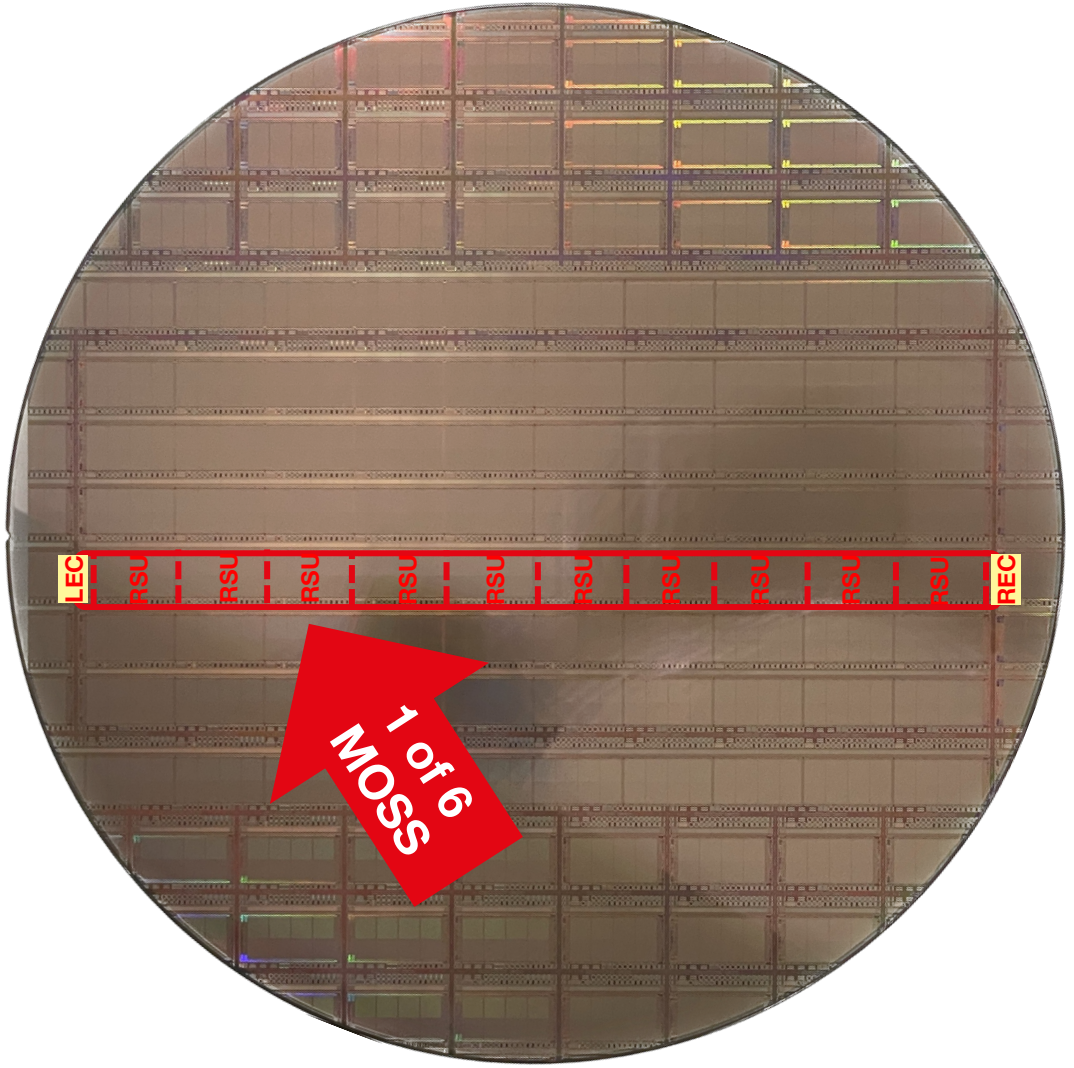


R&D towards ITS3

Process: **TPSCo. 65nm CIS**

Recent submission: 2 major test structures

- **MOSS**
  - 10x **RSU** + 2x **end cap** (left: LEC + right: REC)



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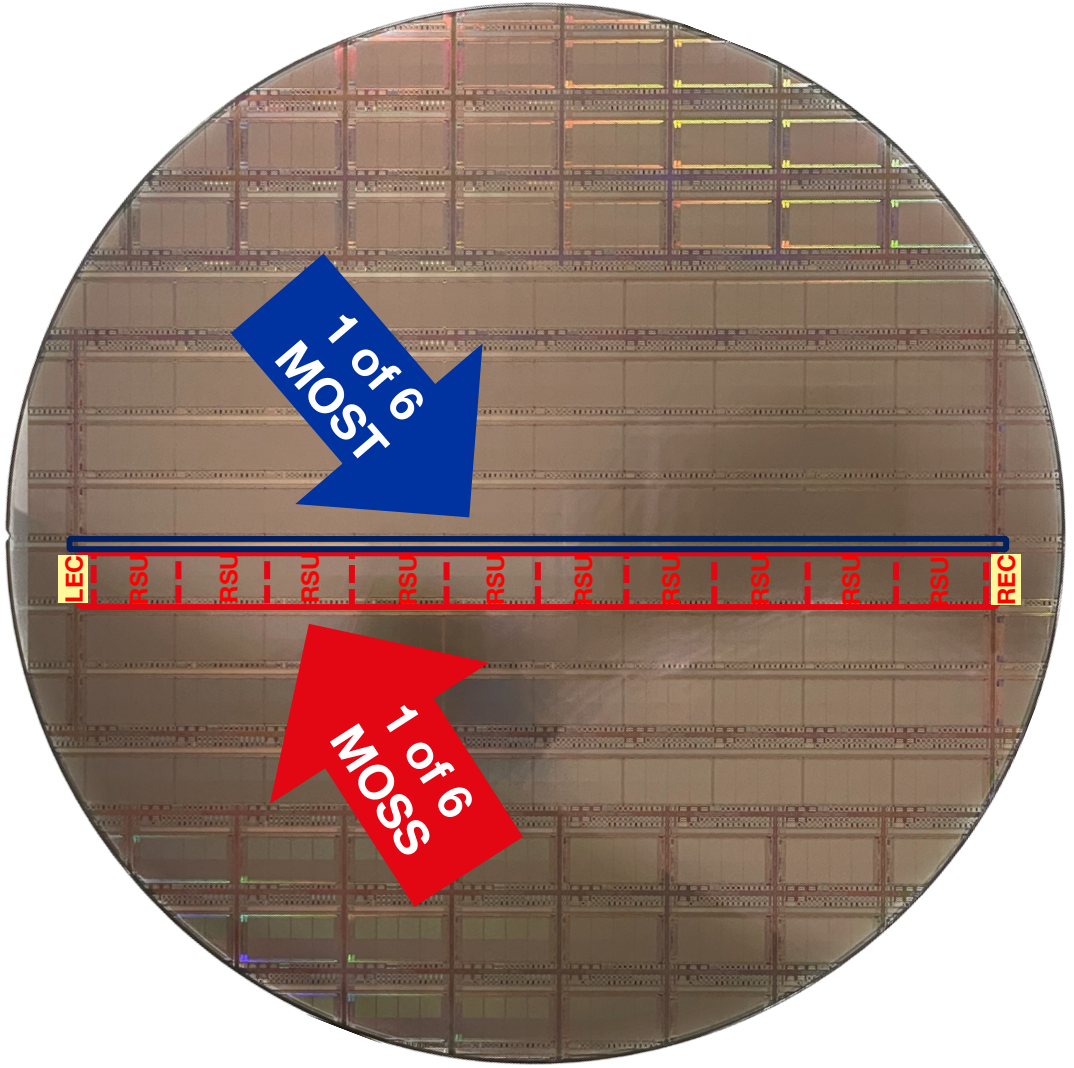

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- **MOST**
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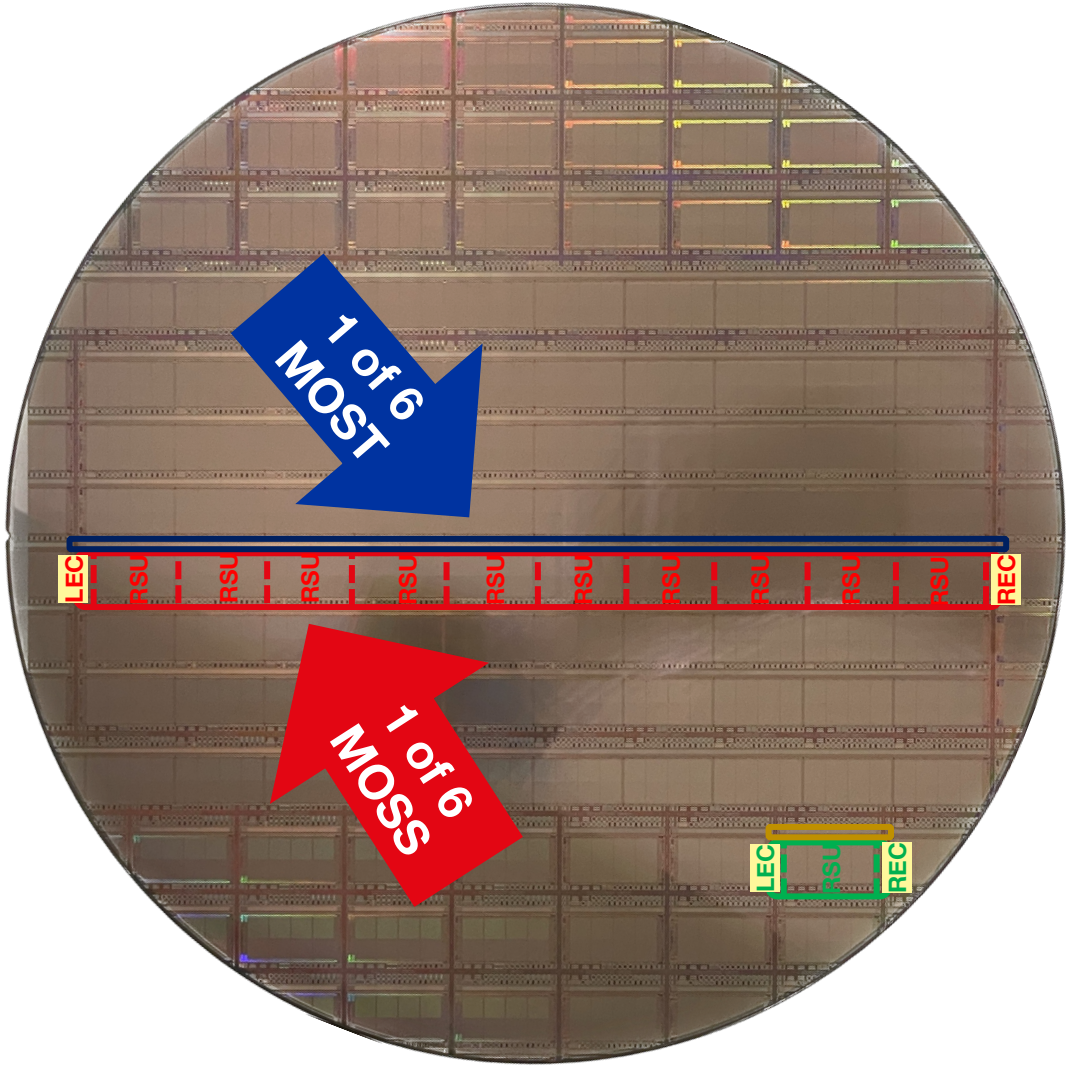
- Plenty **BabyMOSS** and **BabyMOST** with **single** RSU + 2x end cap



MOSS and MOST

	MOSS *Monolithic Stitched Sensor*	**MOST** *Monolithic stitched Sensor with Timing*
Length	259mm	
Width	14mm	2.5mm
Layout	10x repeated unit (RSU) + 1x left endcap + 1x right endcap	
Pixel Pitch	22.5µm & 18.0µm in upper/lower half	18.5µm
Integration Density	Lower	Higher
Powering	Separate power nets per half RSU	Global power nets with switches to detach groups of ≈300px
Diode Biasing	Negative voltage to substrate	Shift up front-end by positve voltage
Readout	In-pixel hit latch	Asynchronous with ToT

List not exhaustive…

Powering Yield

- Difficulty: Selection of sensors only possible on full wafer level
  - High yield crucial!
- MOSS: **120 chips** from 20 wafers

Powering Yield

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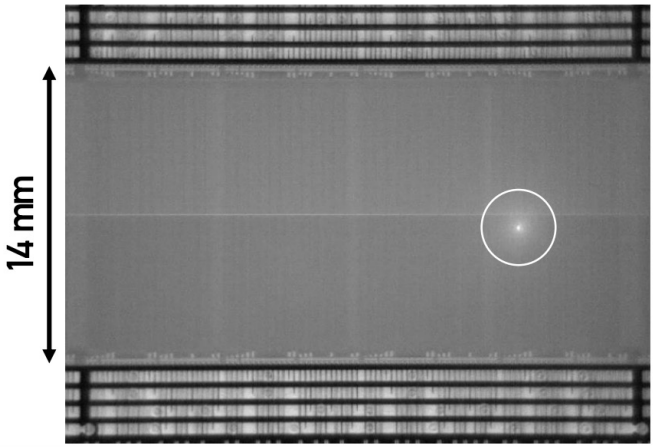
- MOSS: **120 chips** from 20 wafers
- Procedure:
  1. **Impedance** measurement
  2. **Power-ramp** under thermal camera
  3. **Impedance** measurement
- Impedance measurement to detect cross-net shorts (i.e. AVDD to DVSS, …)

Powering Yield

Observations:

- Thermal hotspots during ramp

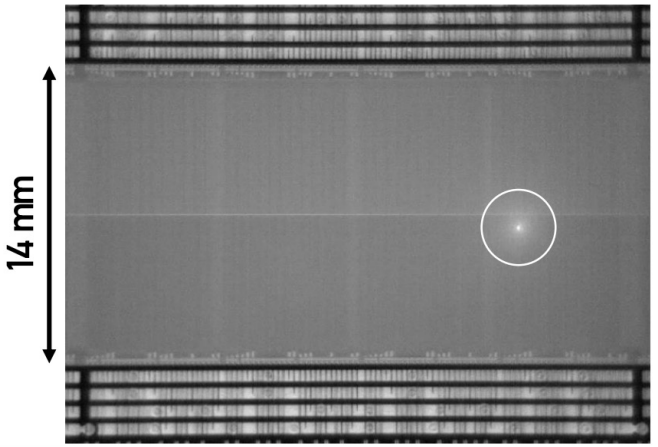


Thermal camera image of one RSU

Powering Yield

Observations:

- Thermal hotspots during ramp
- Sometimes strongly increased current during ramp
- If current transient → Impedance changes
- Thermal hotspots correlate spatially with power grid



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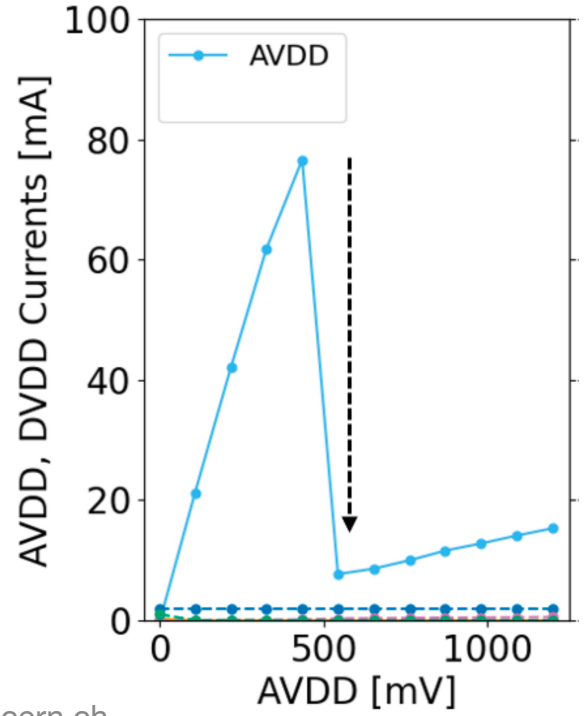

Example of a transient current

Powering Yield

- Hypotheses:
  - Shorts in power grid
  - Shorts can burn through

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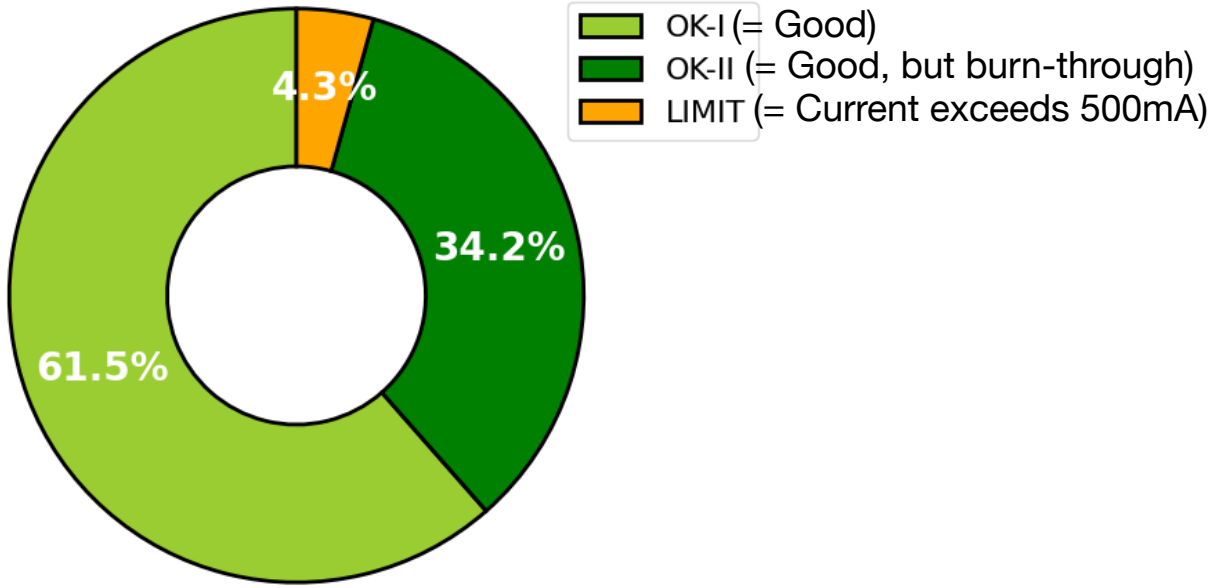
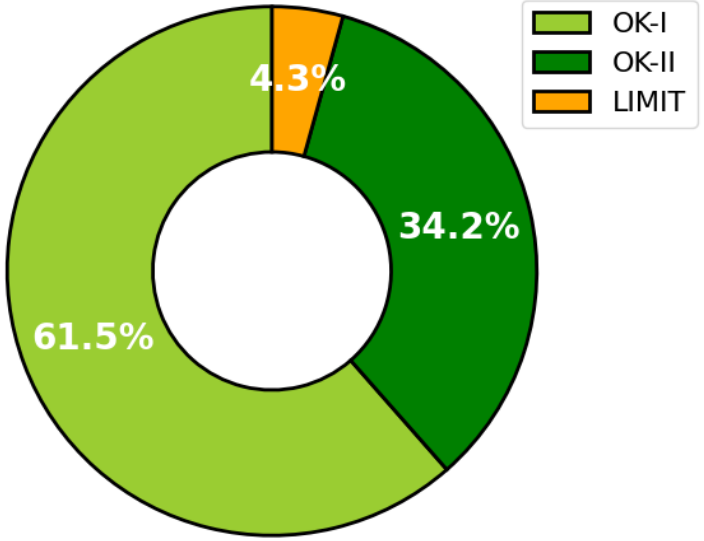
- **<5% with persistent shorts**
- OK-I and OK-II efficient in beam!



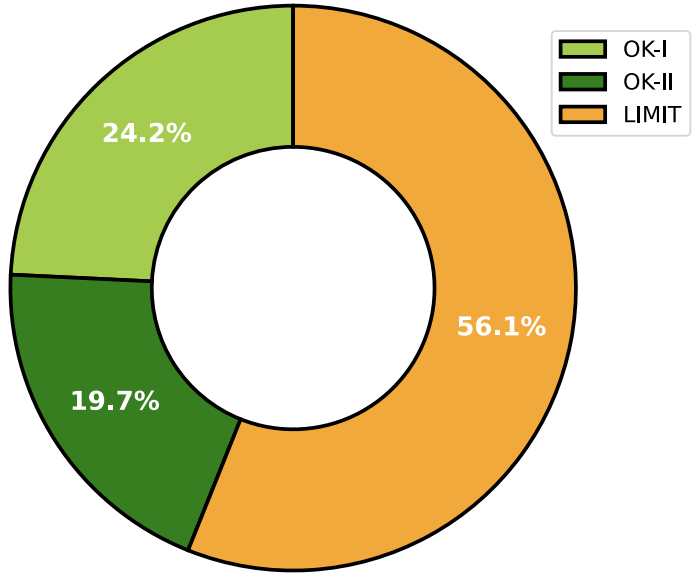
Powering Yield

- MOST: Chips can be powered **globally only**
- Number of **not working chips** is naturally much higher than number of **not working regions**
  - ➔ For final comparison: Need to normalize by number of possible failure spots



MOSS

Based on 1620 half RSU



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Based on 66 full chips

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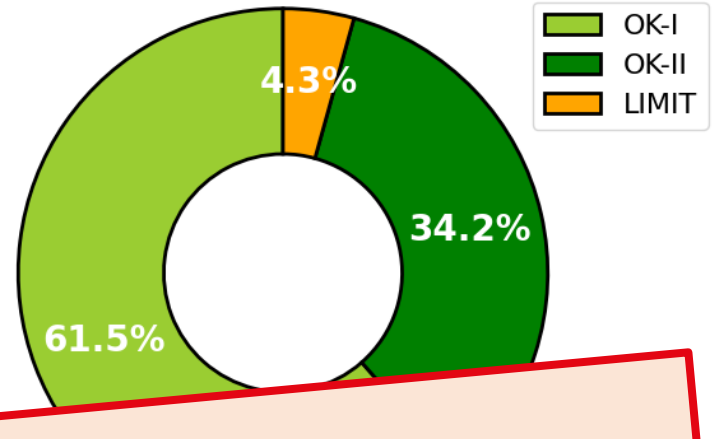
Close interaction with foundry
➔ Issue understood and will be mitigated



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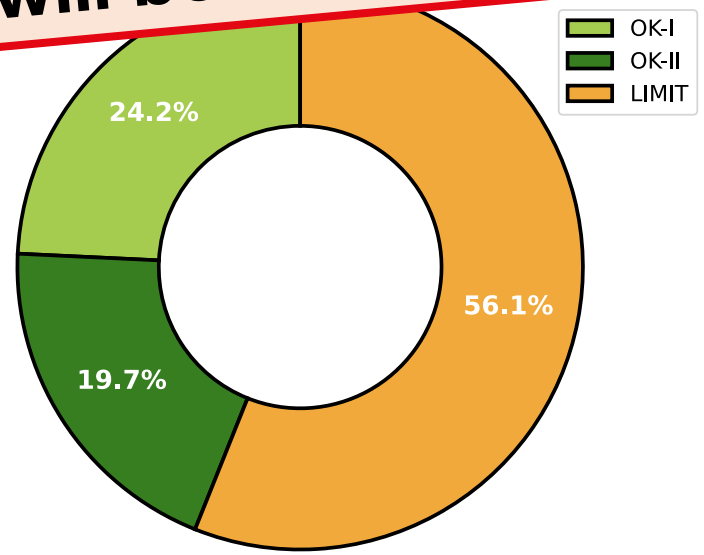

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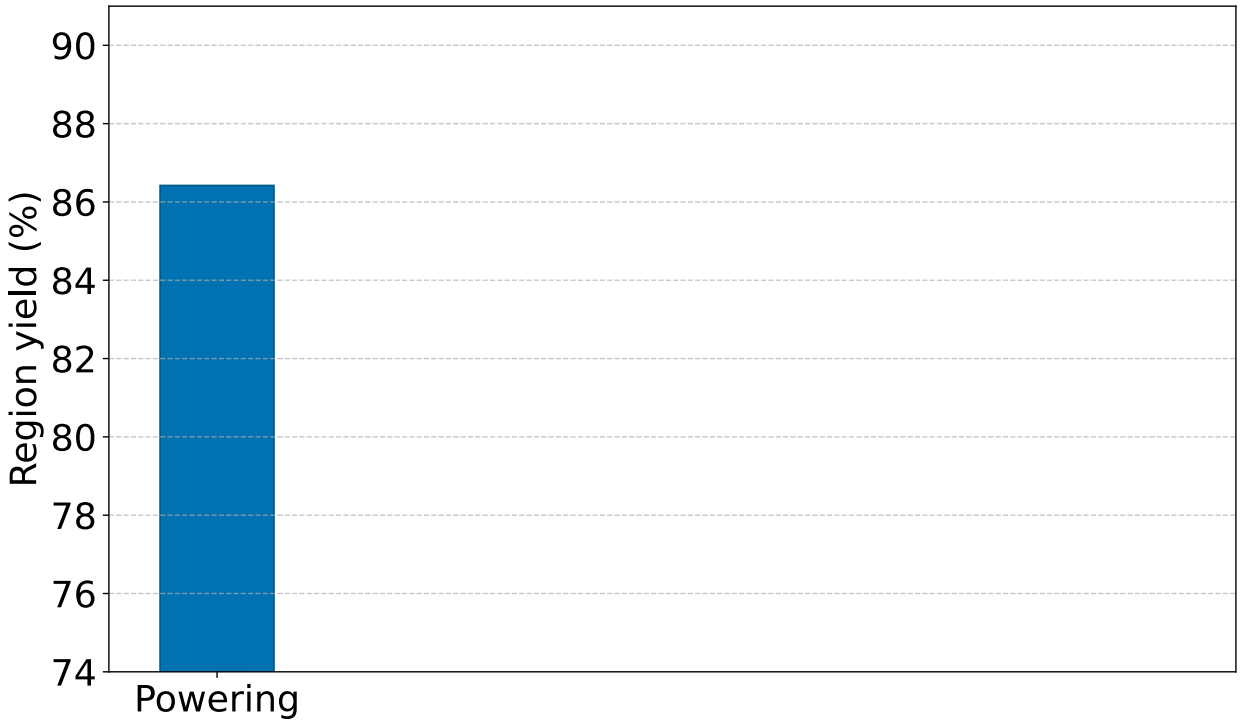
Functional Testing

- MOSS: **82 chips from 14 wafers**
- Region: $(256px)^2$ or $(320px)^2$
- Powering heavily affected by shorts in power grid



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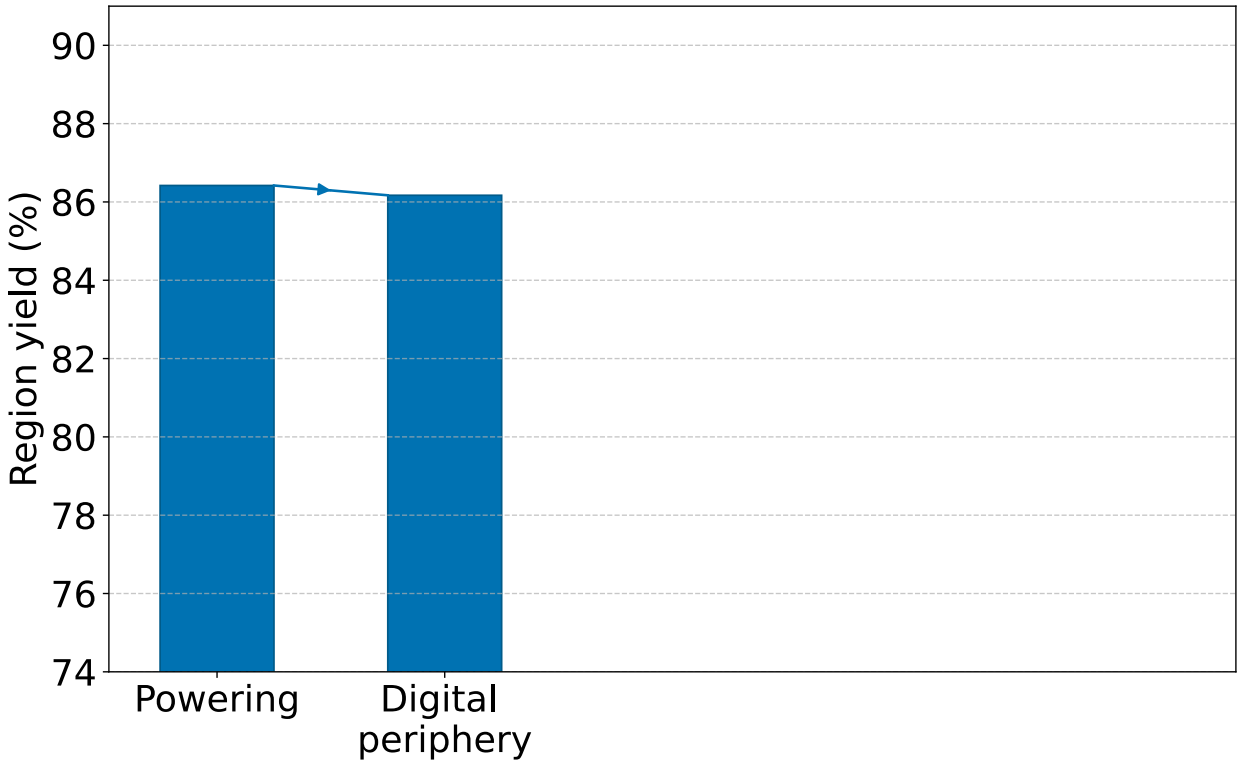

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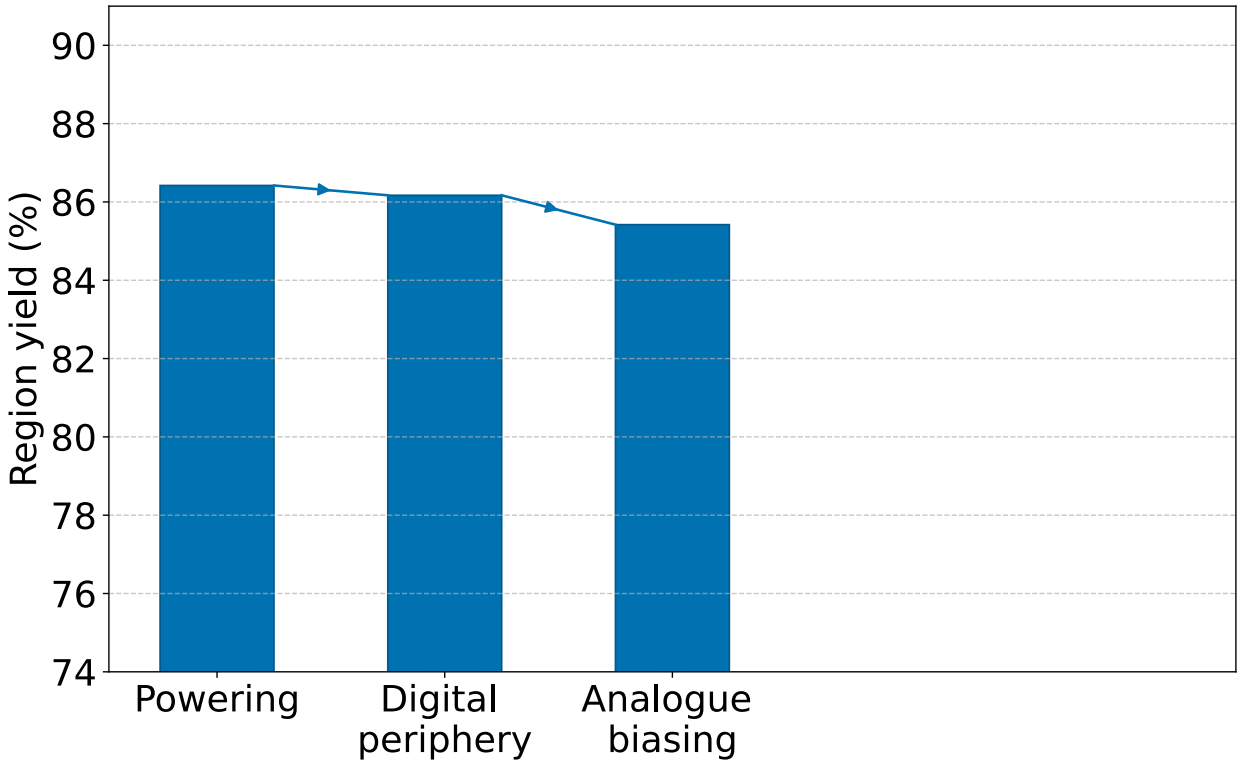

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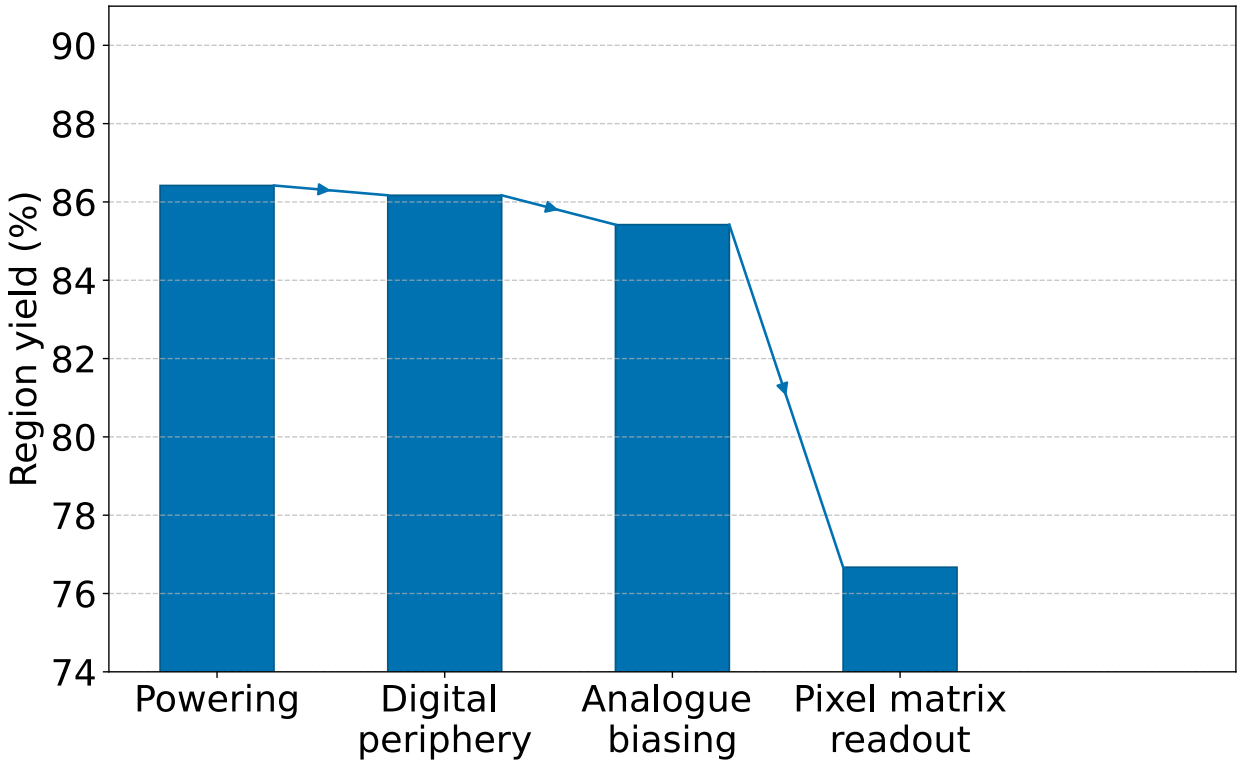

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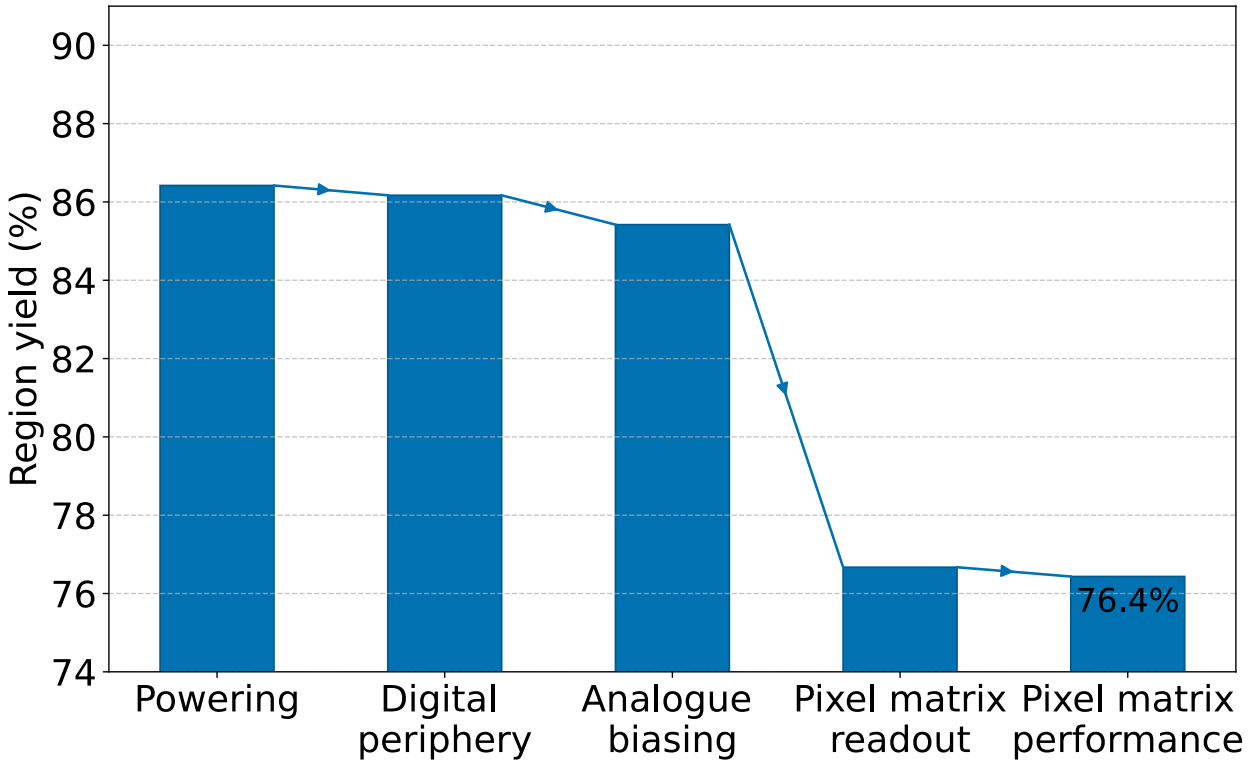

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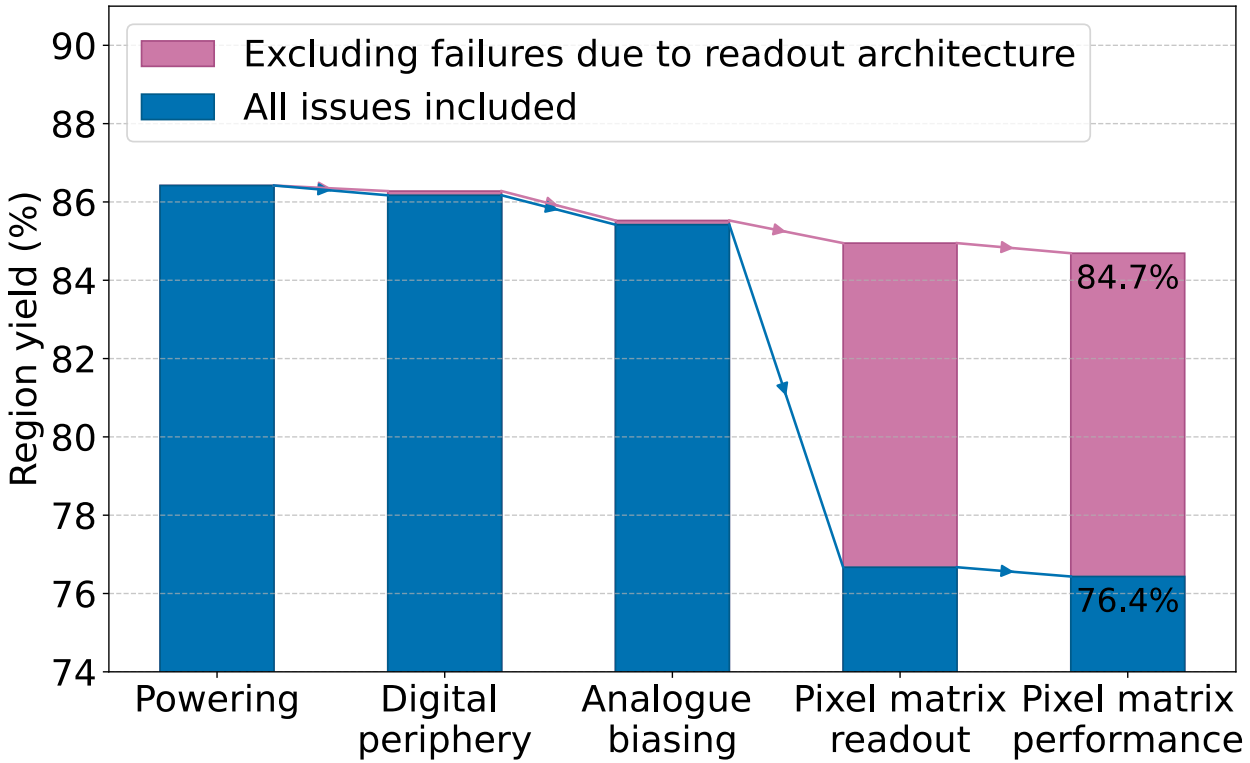

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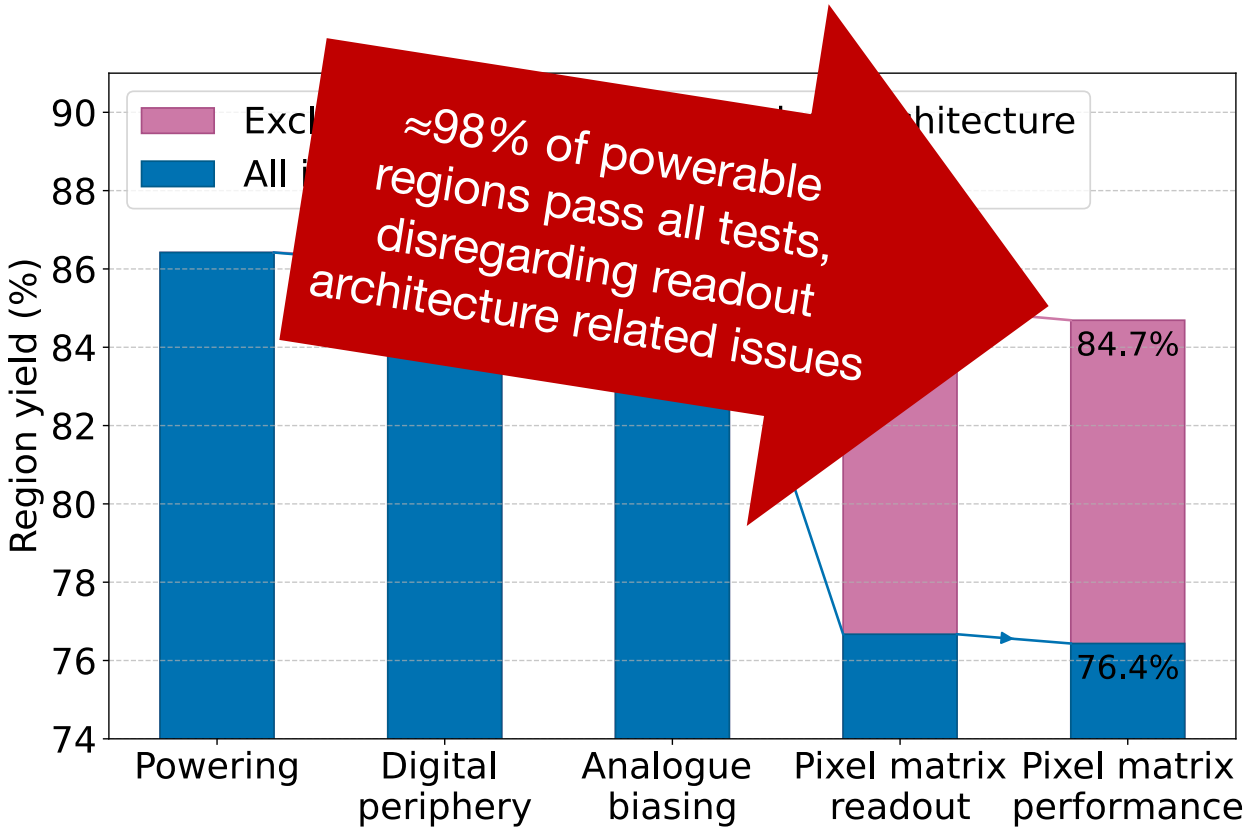
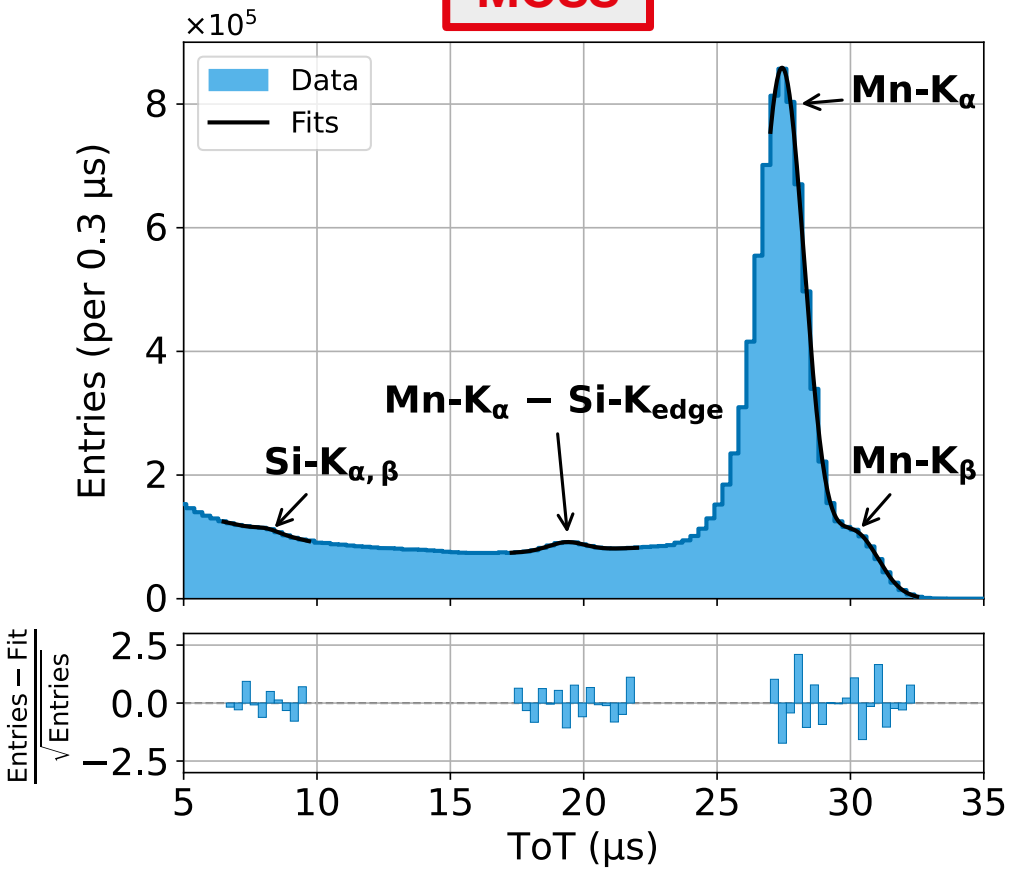


Fe55 Spectra

MOSS



Energy Resolution
$(7.3 \pm 0.2)\%$

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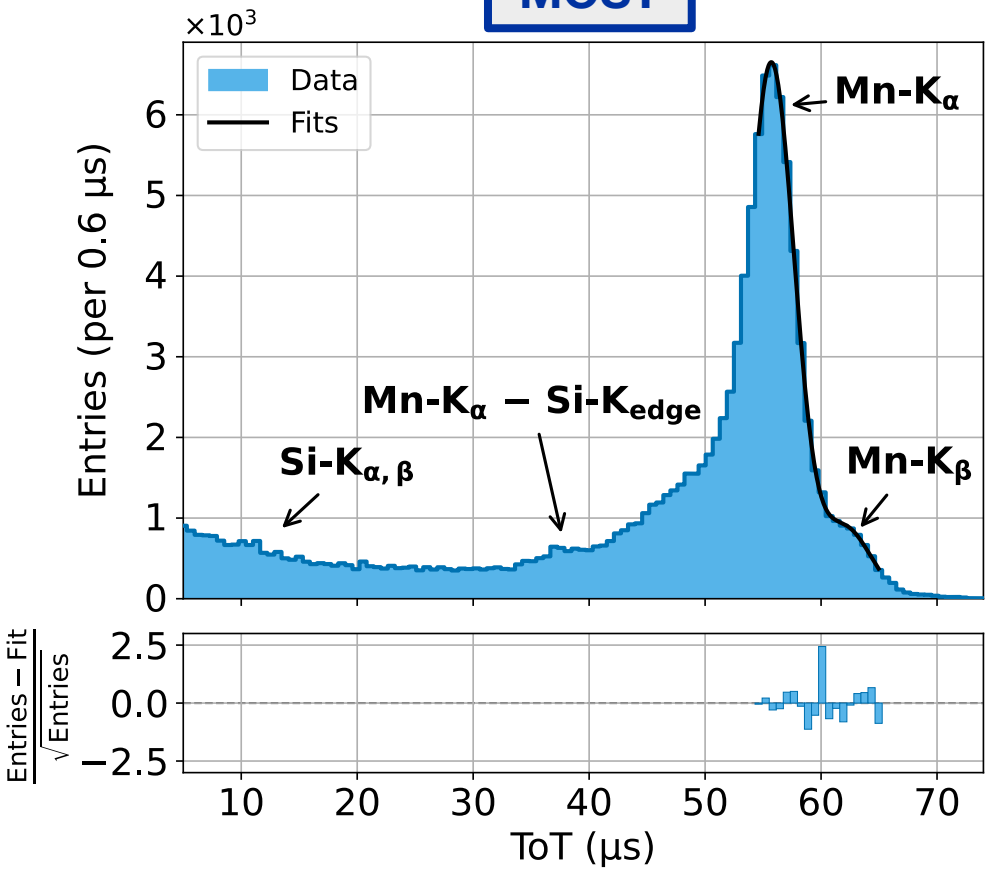

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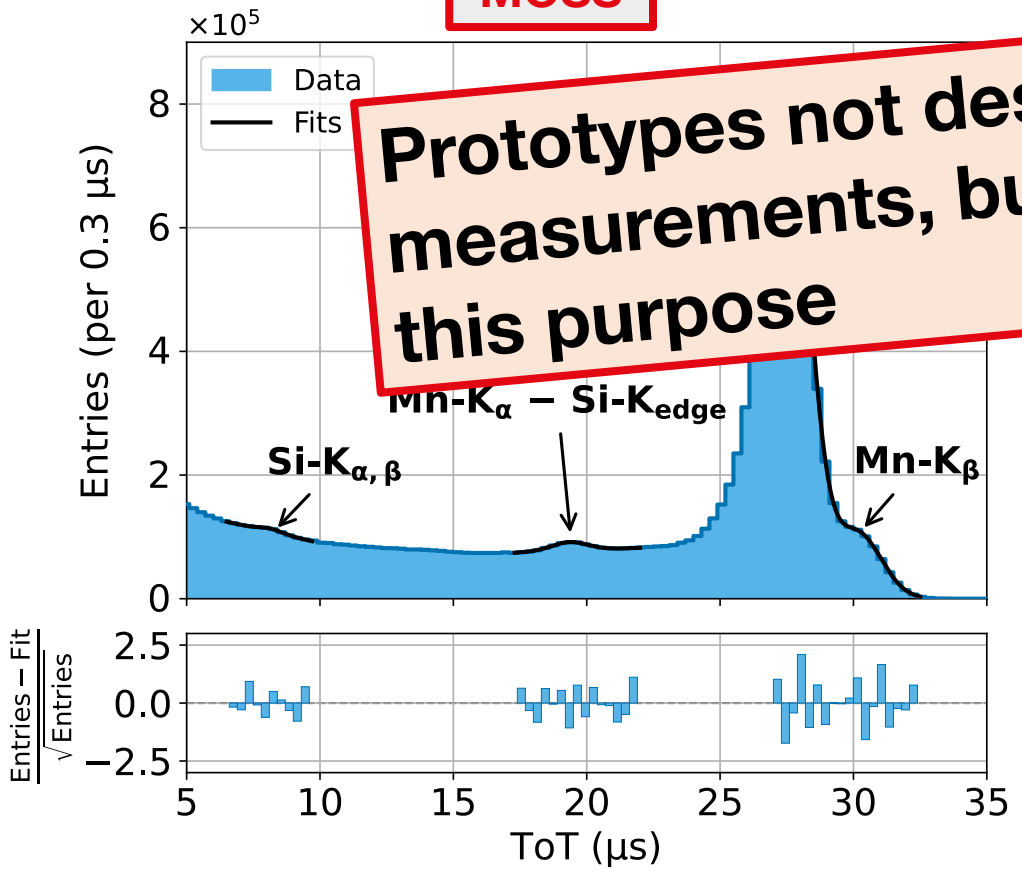
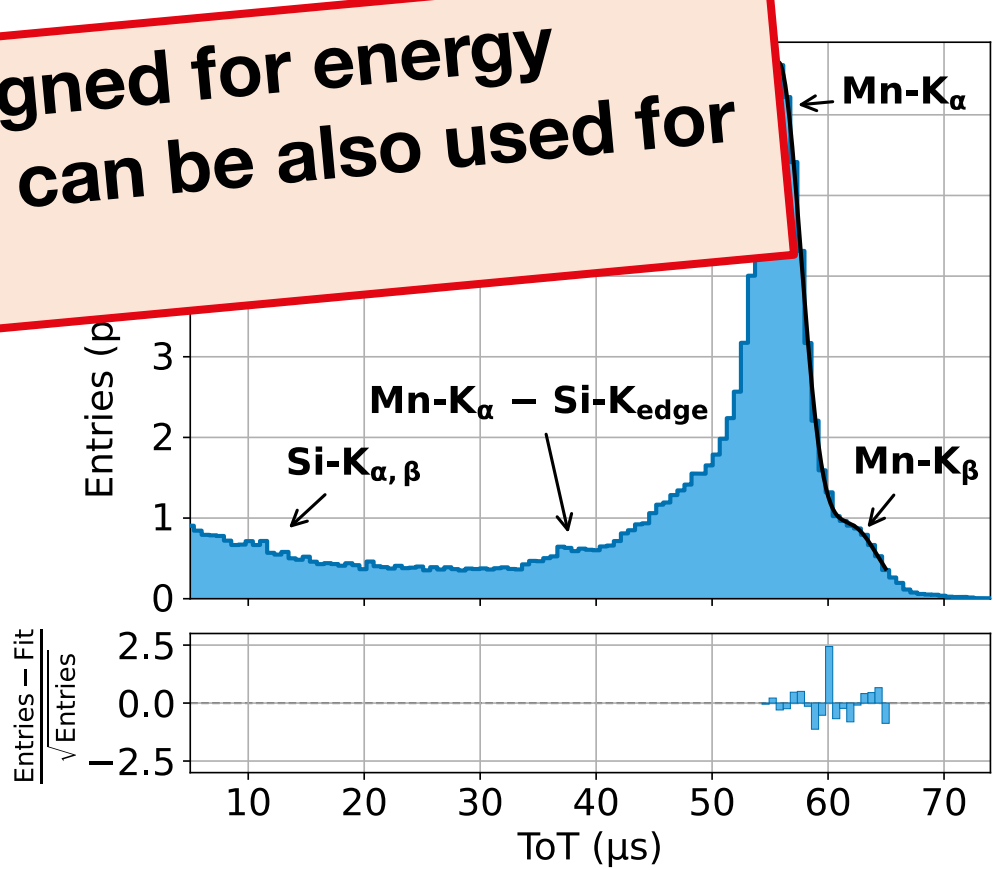


Prototypes not designed for energy measurements, but can be also used for this purpose



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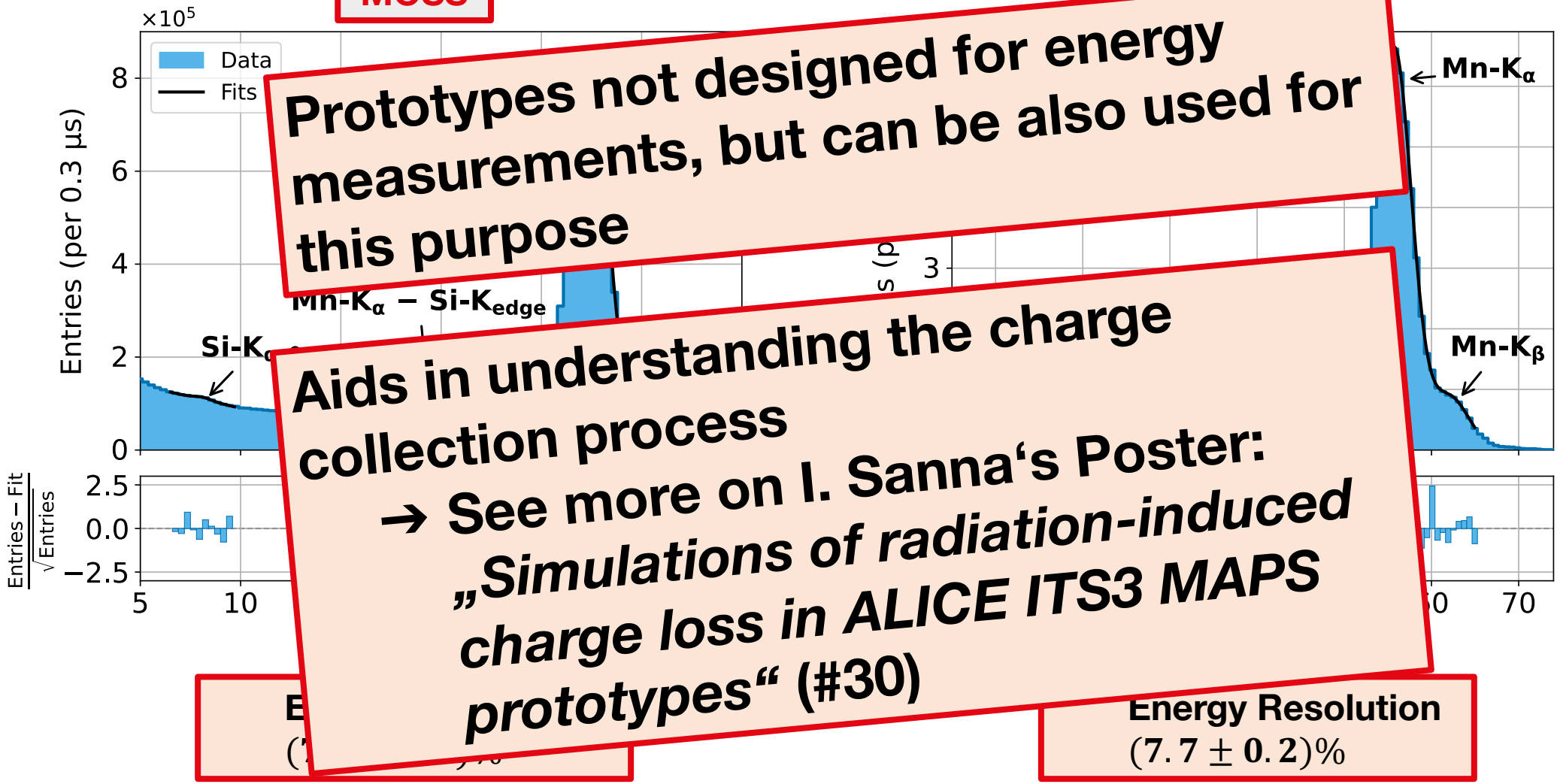

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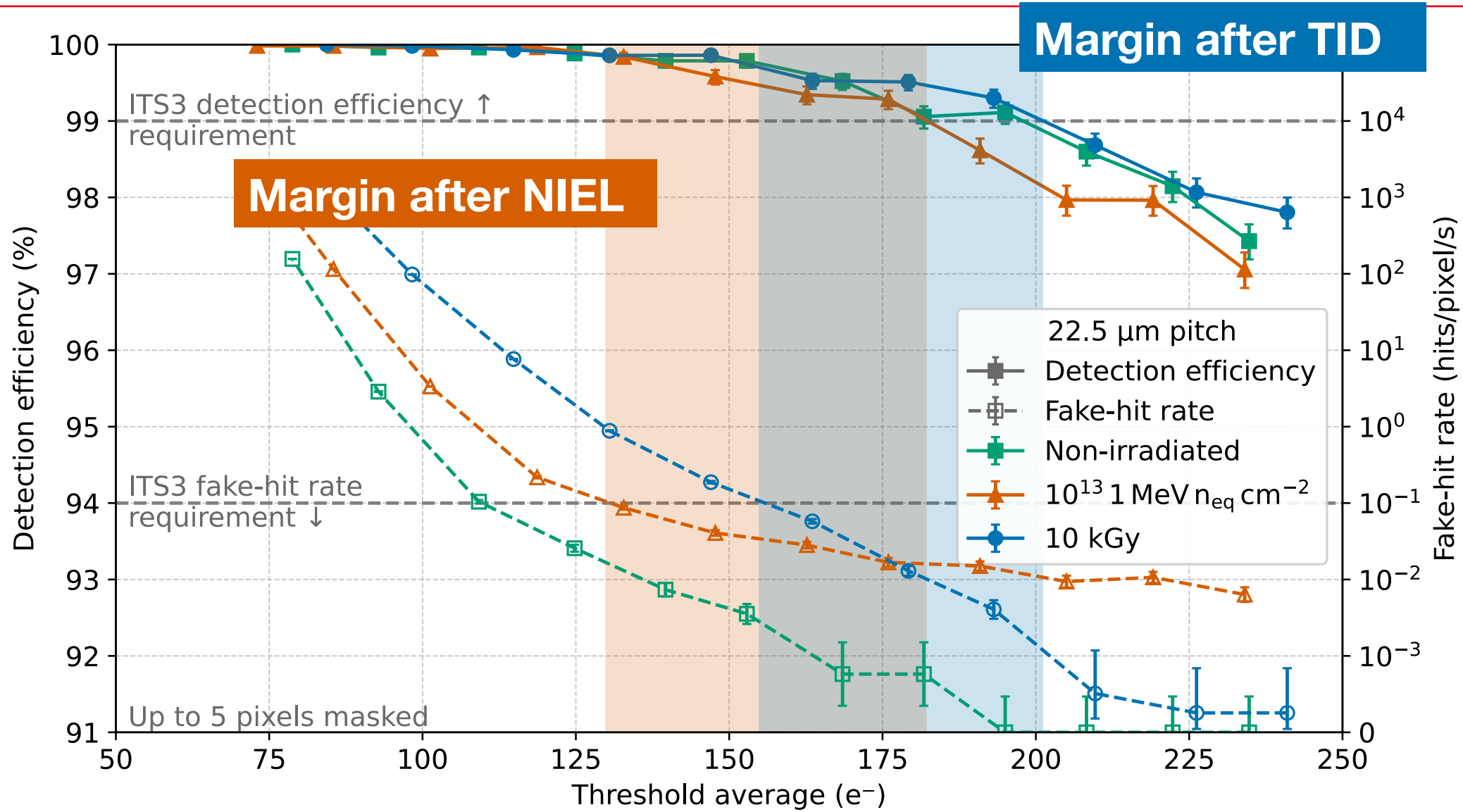
Aids in understanding the charge collection process

➔ See more on I. Sanna's Poster:

„Simulations of radiation-induced charge loss in ALICE ITS3 MAPS prototypes" (#30)

Testbeam Results



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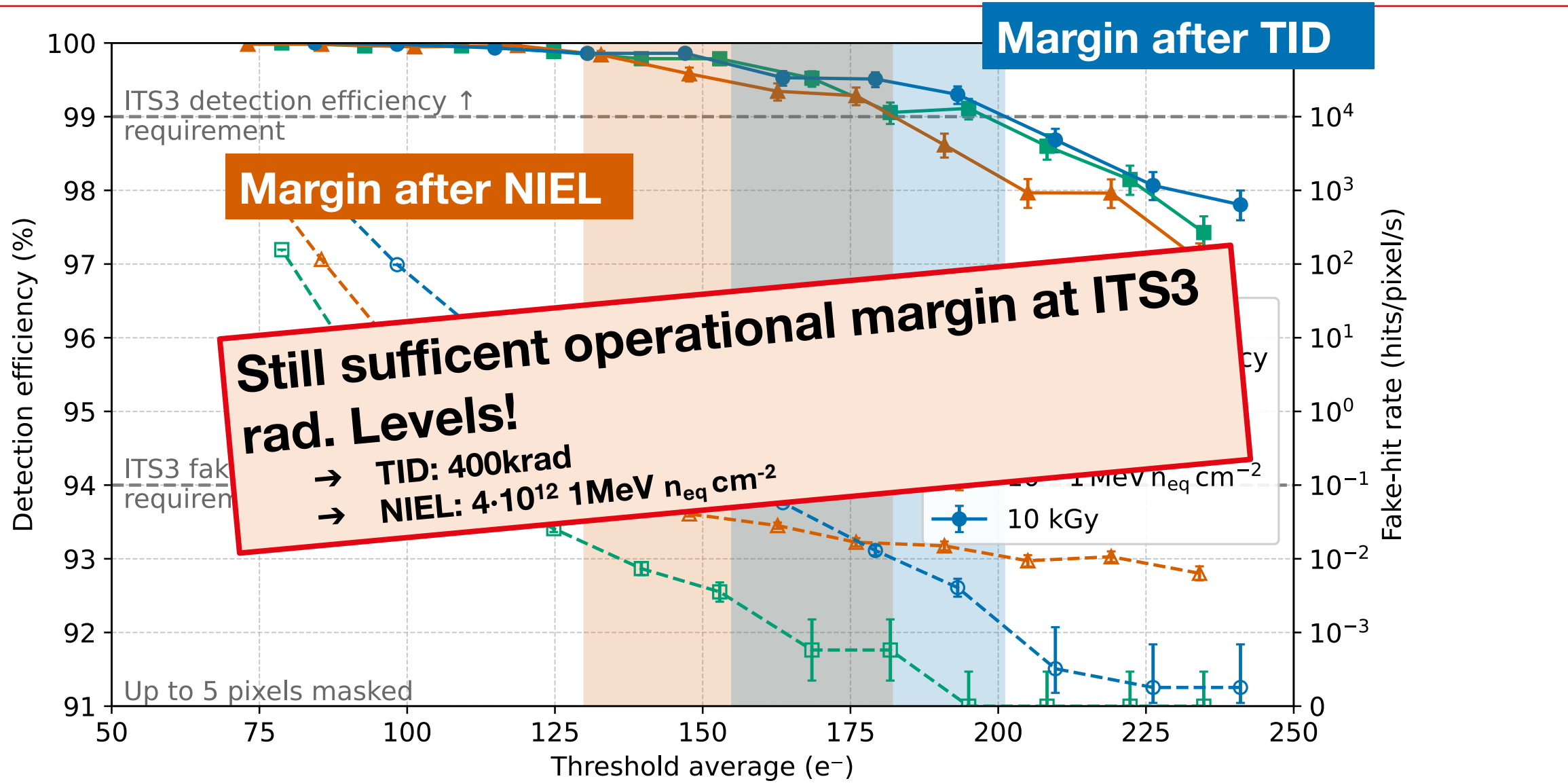
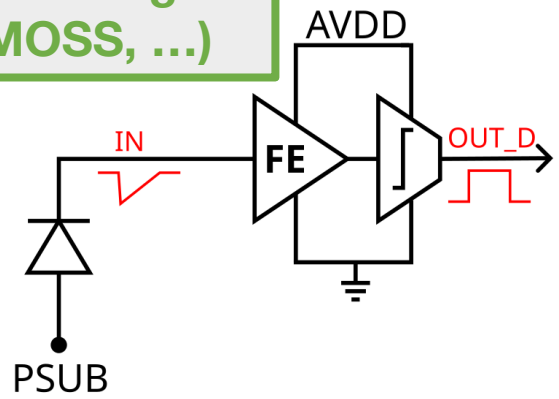


Front-End Shift

- Previous designs: Diode biased by **negative voltage**

Former Designs (i.e. MOSS, …)



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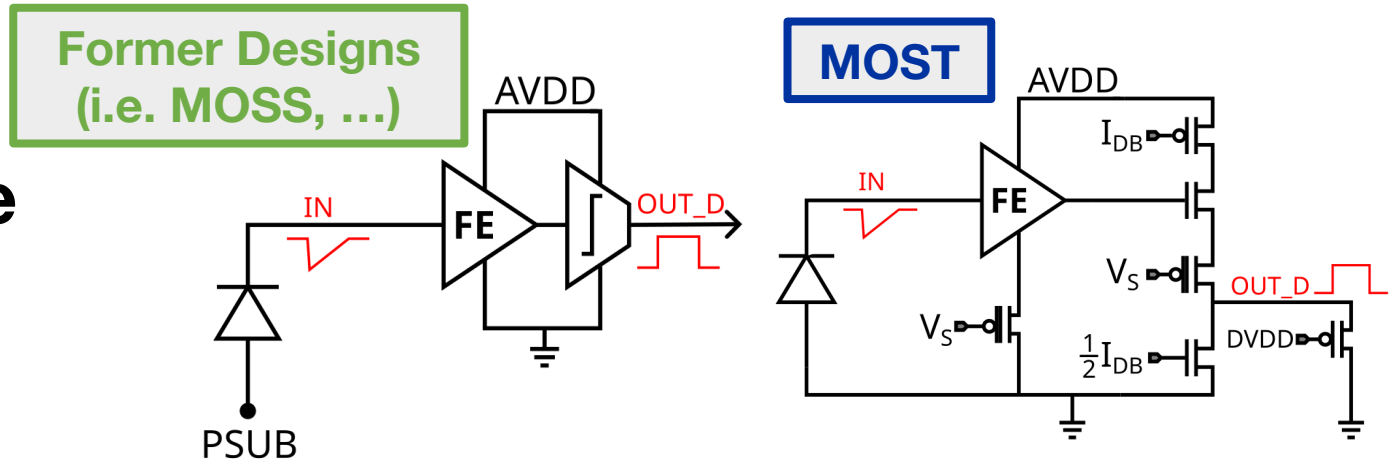
  - Upper rail of FE (AVDD) also needs to increase
  - Switching back to regular domain in discriminator



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- MOST: Alternative diode biasing scheme
  - **FE is shifted up** by VS
  - Upper rail of FE (AVDD) also needs to increase
  - Switching back to regular domain in discriminator
- Applying “effective back-bias” decreases threshold
  - **Works as expected!**

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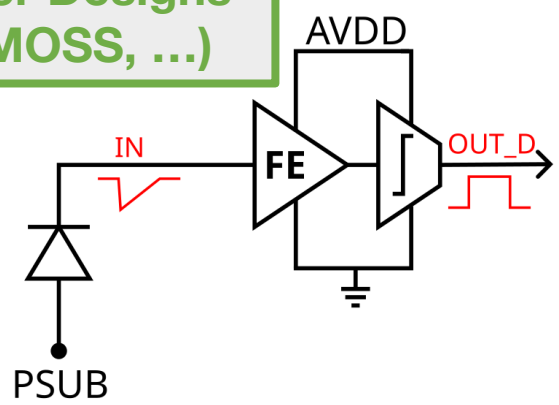

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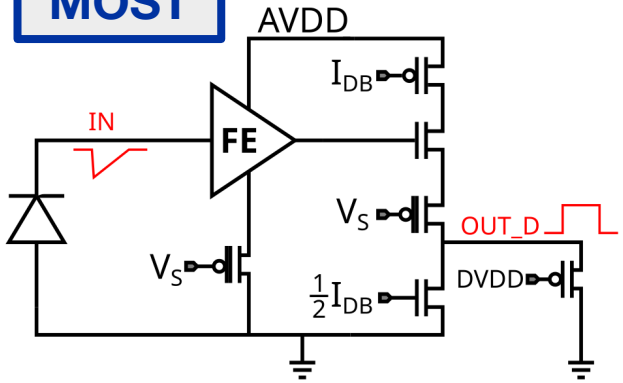
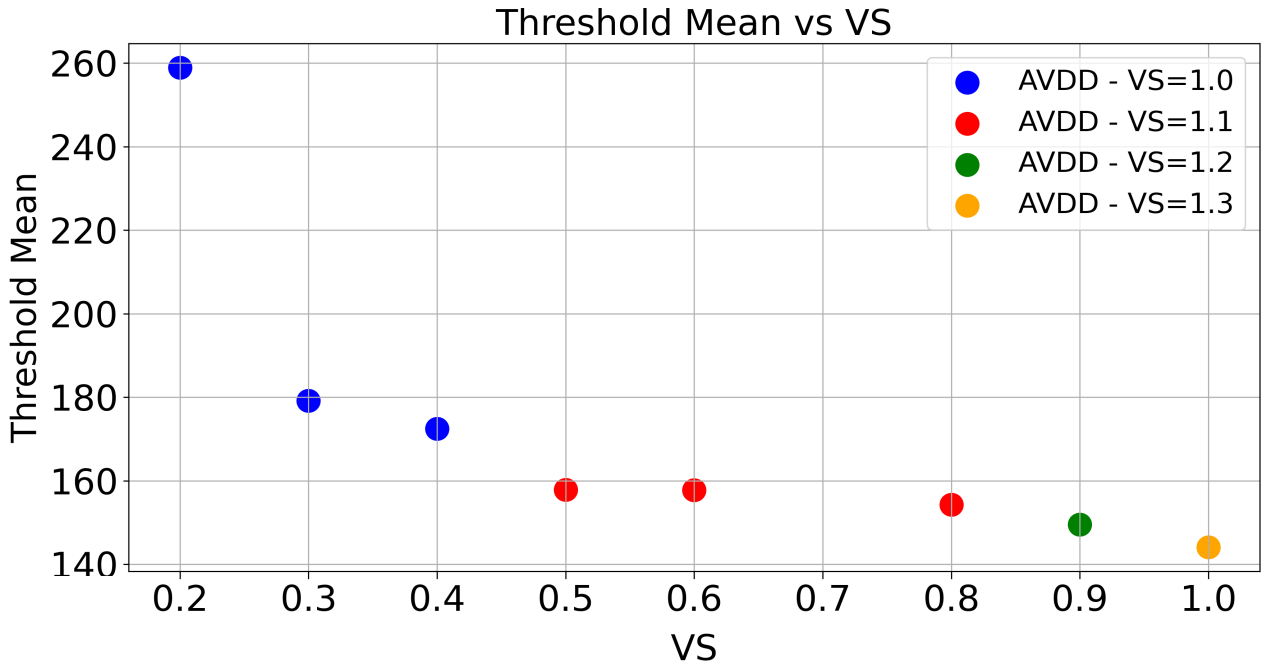
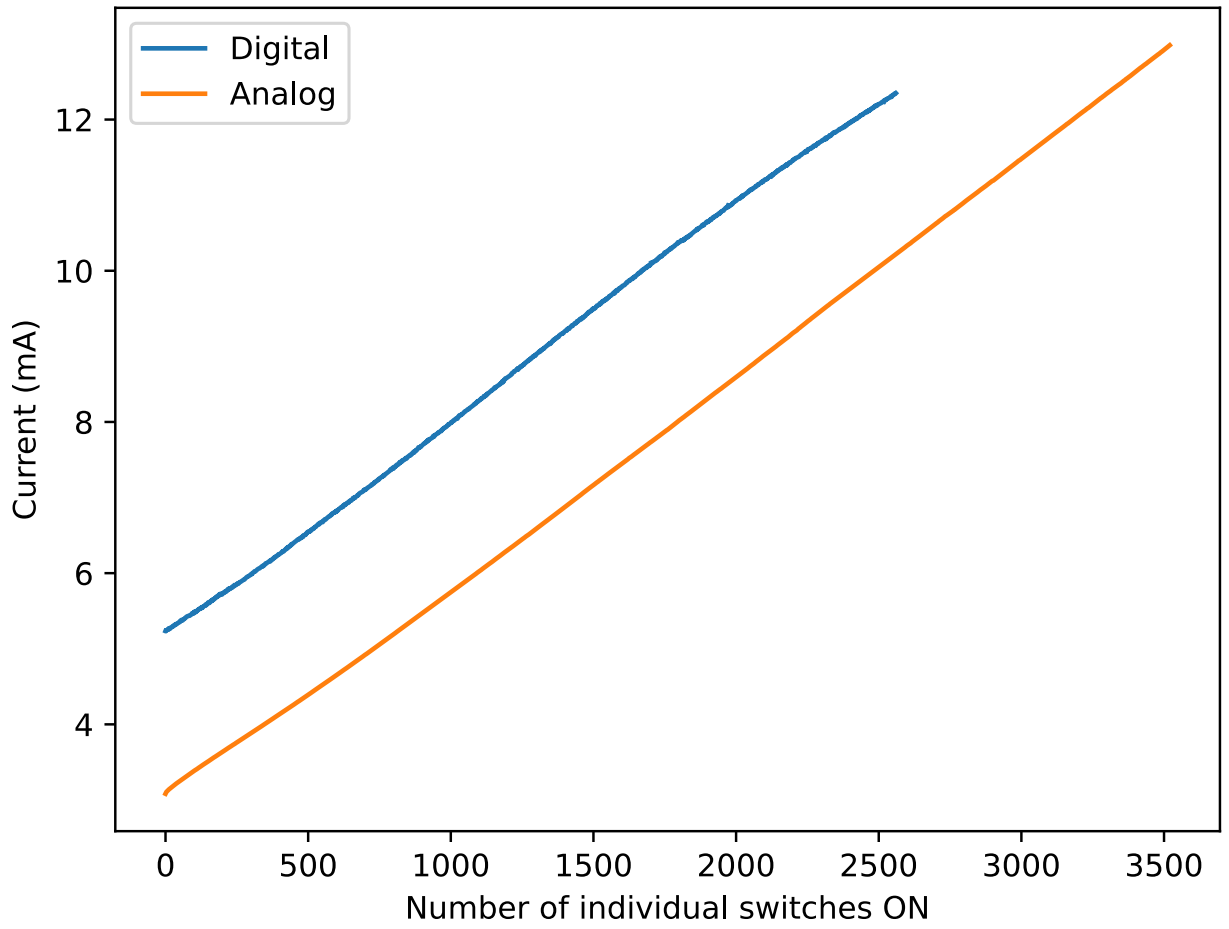




Power Gating

- Analog: 1x switch per 4 rows (256 px)
- Digital: 1x switch per 352 px
- Uniform increase in current consumption, no jumps



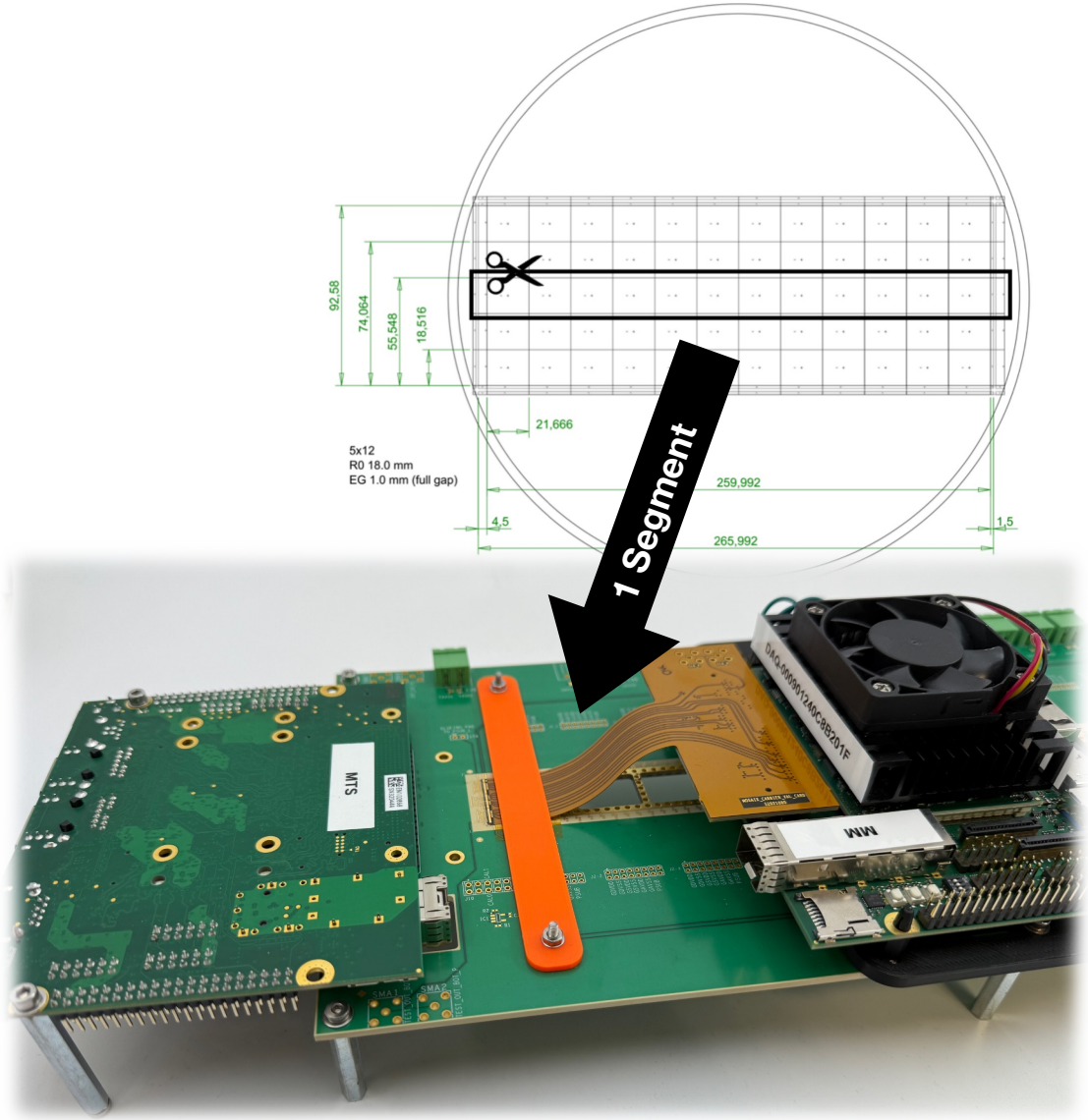
Outlook

Upcoming chip: **MOSAIX**

- Tapeout in July this year
- Full-size fully functional prototype of ITS3 sensor chip

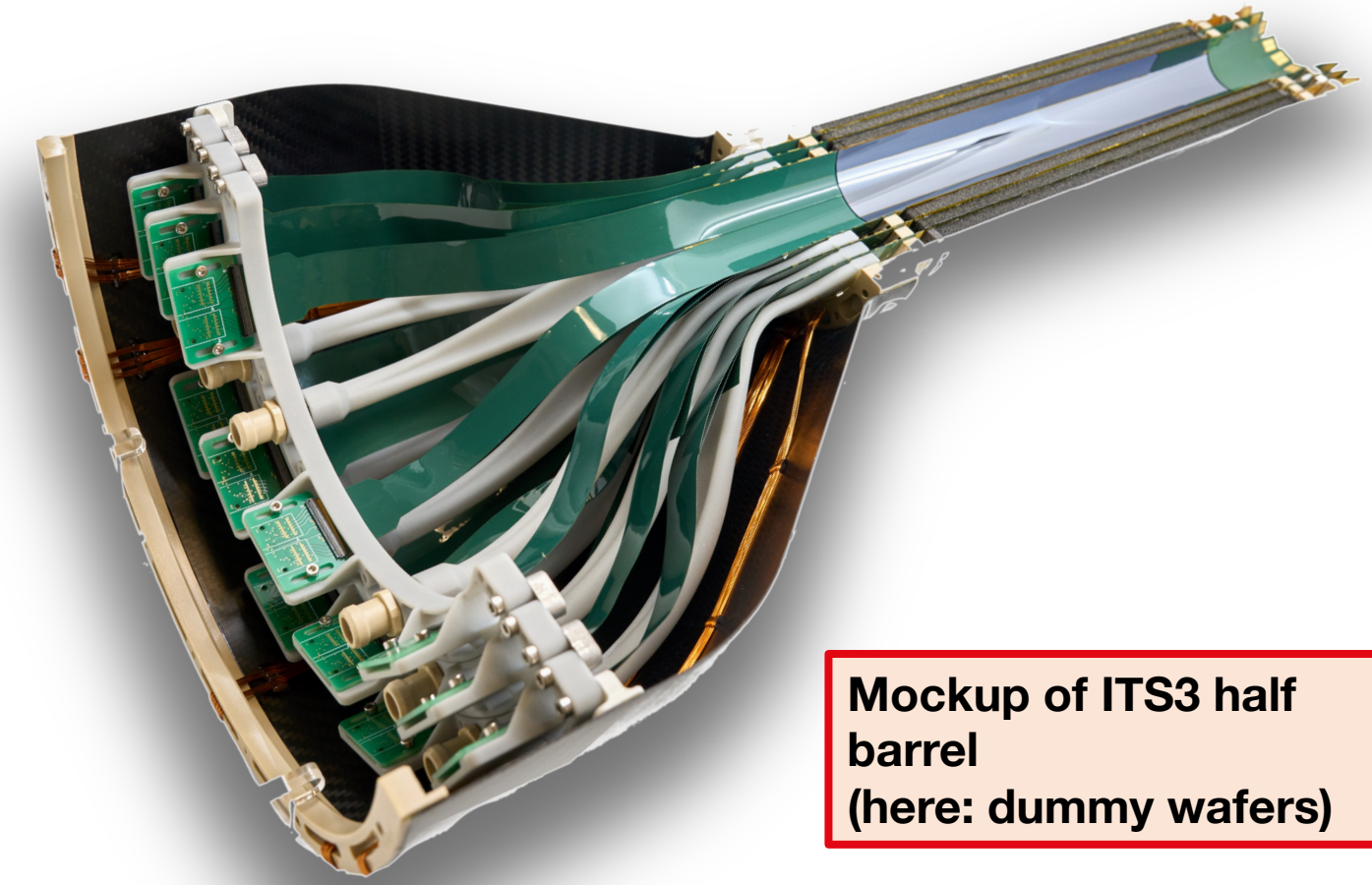
Currently:

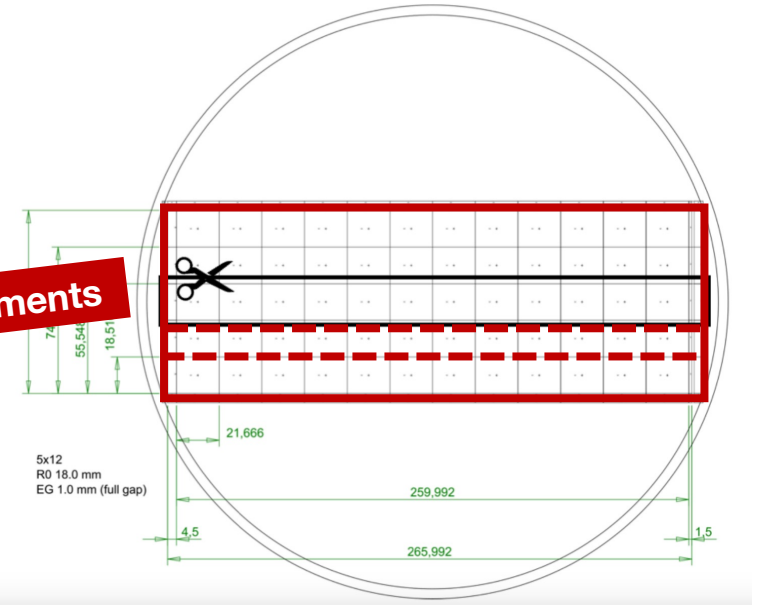
- Preparation of test system Hardware, software, firmware
- Validation of all components (incl. software!) with model of MOSAIX ASIC on FPGA: **MOSAIX *Emulator***



Outlook

Allow testing of **full-scale prototype** including bending



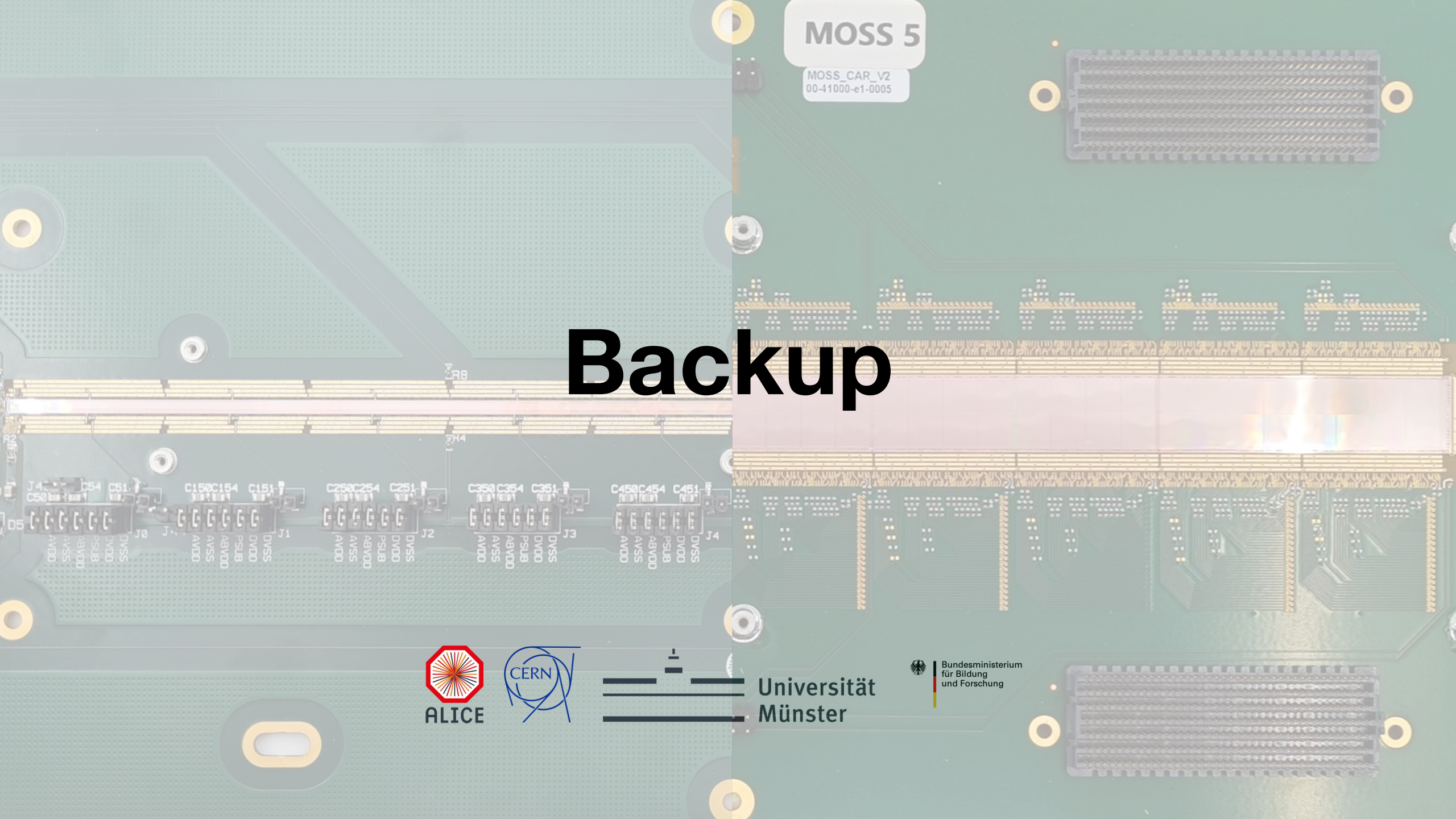


Mockup of ITS3 half barrel (here: dummy wafers)

Summary

- Issue in power grid observed
  - **Different power grid design** in next (recent) submission
- Overall **yield in line for ITS3**, when disregarding certain issues related to prototype readout architecture
  - Next chip will have different (final) readout architecture
  - 98% + possibly more, when employing power gating
- Smaller and larger pixel pitch both show **substantial operational margin for ITS3 radiation levels**
  - ➔ TID: 400krad
  - ➔ NIEL: $4 \cdot 10^{12}$ 1MeV n_{eq} cm^{-2}
- Very successful Engineering Run!
  - Stay tuned for MOSAIX…

Backup



ALICE

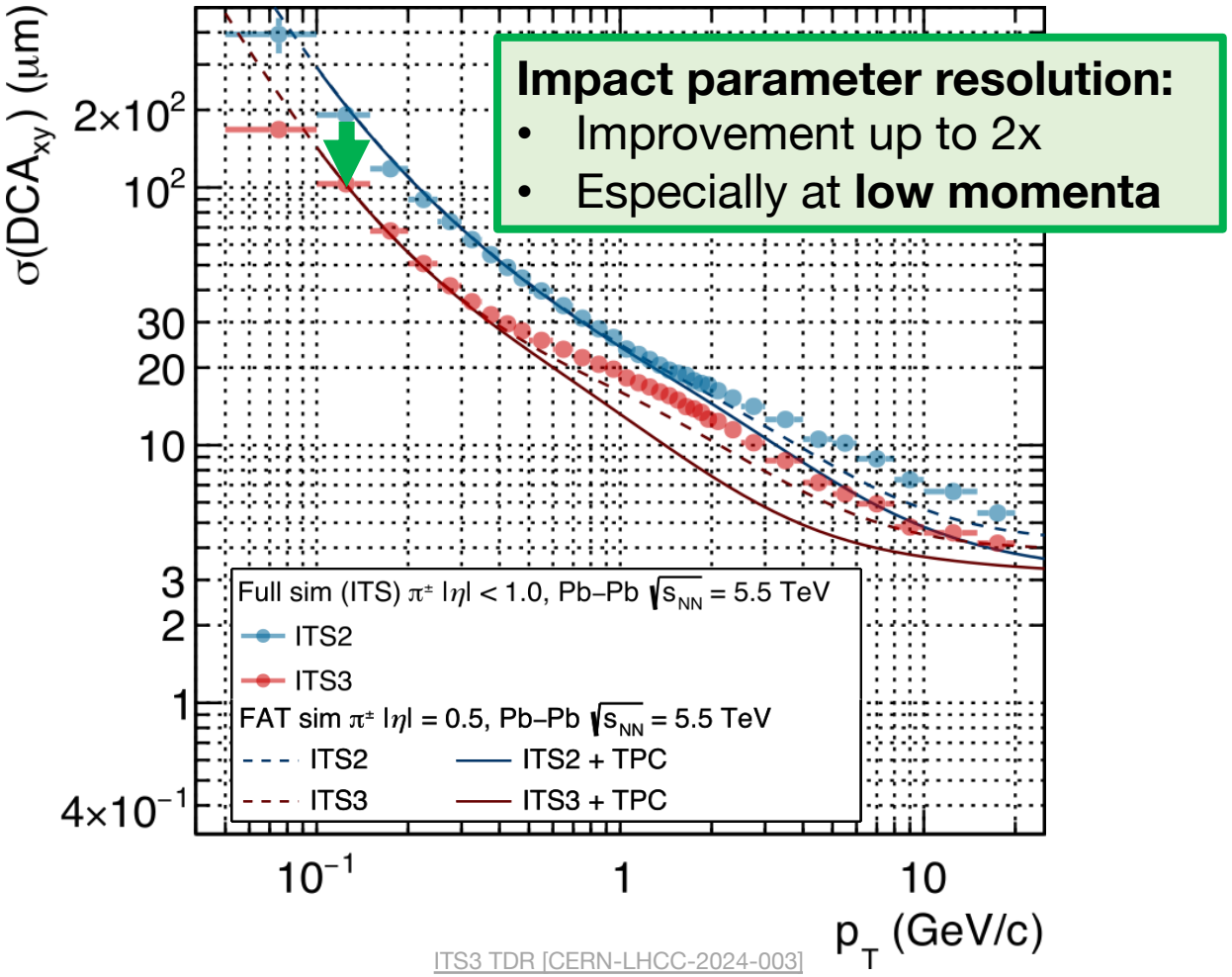
CERN

Universität Münster

Bundesministerium für Bildung und Forschung

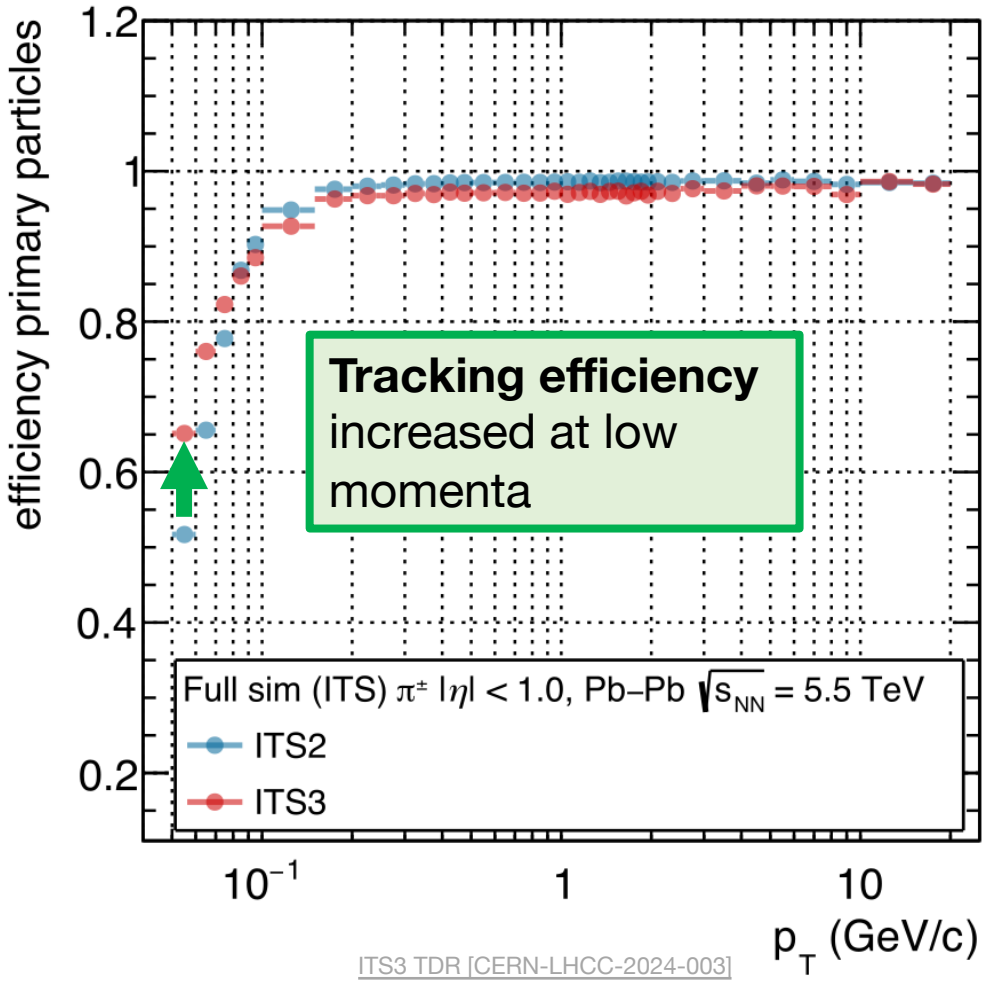
Detector Concept

ALICE: Strong interest in low moment particle reconstruction



Impact parameter resolution:
- Improvement up to 2x
- Especially at **low momenta**

ITS3 TDR [CERN-LHCC-2024-003]



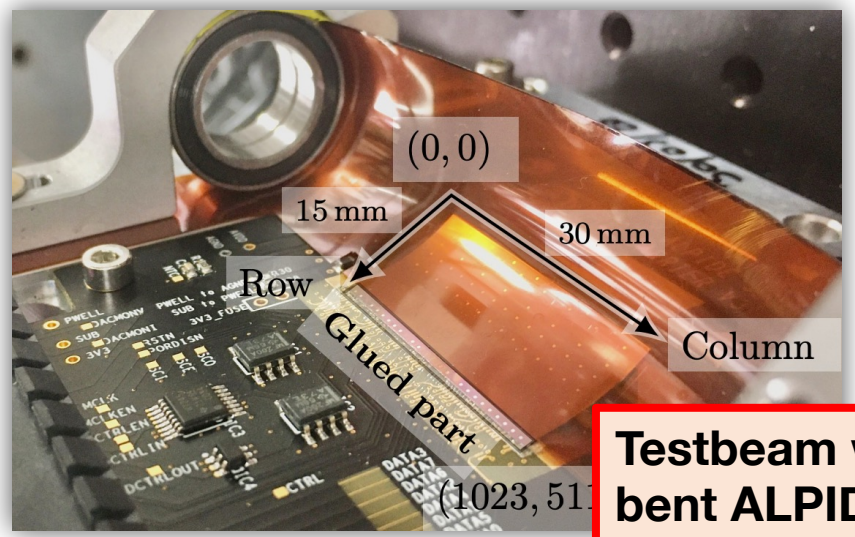
Tracking efficiency increased at low momenta

ITS3 TDR [CERN-LHCC-2024-003]

Detector Concept

- Bend silicon wafer to **half cylinders**
  - Detector size limited by wafer size
- ITS2: 180nm process using 200mm wafers
  - Too small
- Switch to **65nm process** with **300mm wafers**
  - “Bonus”: Smaller feature size → tighter integration

Bent 20µm Si Wafer



Testbeam with bent ALPIDE Chip (ITS2)

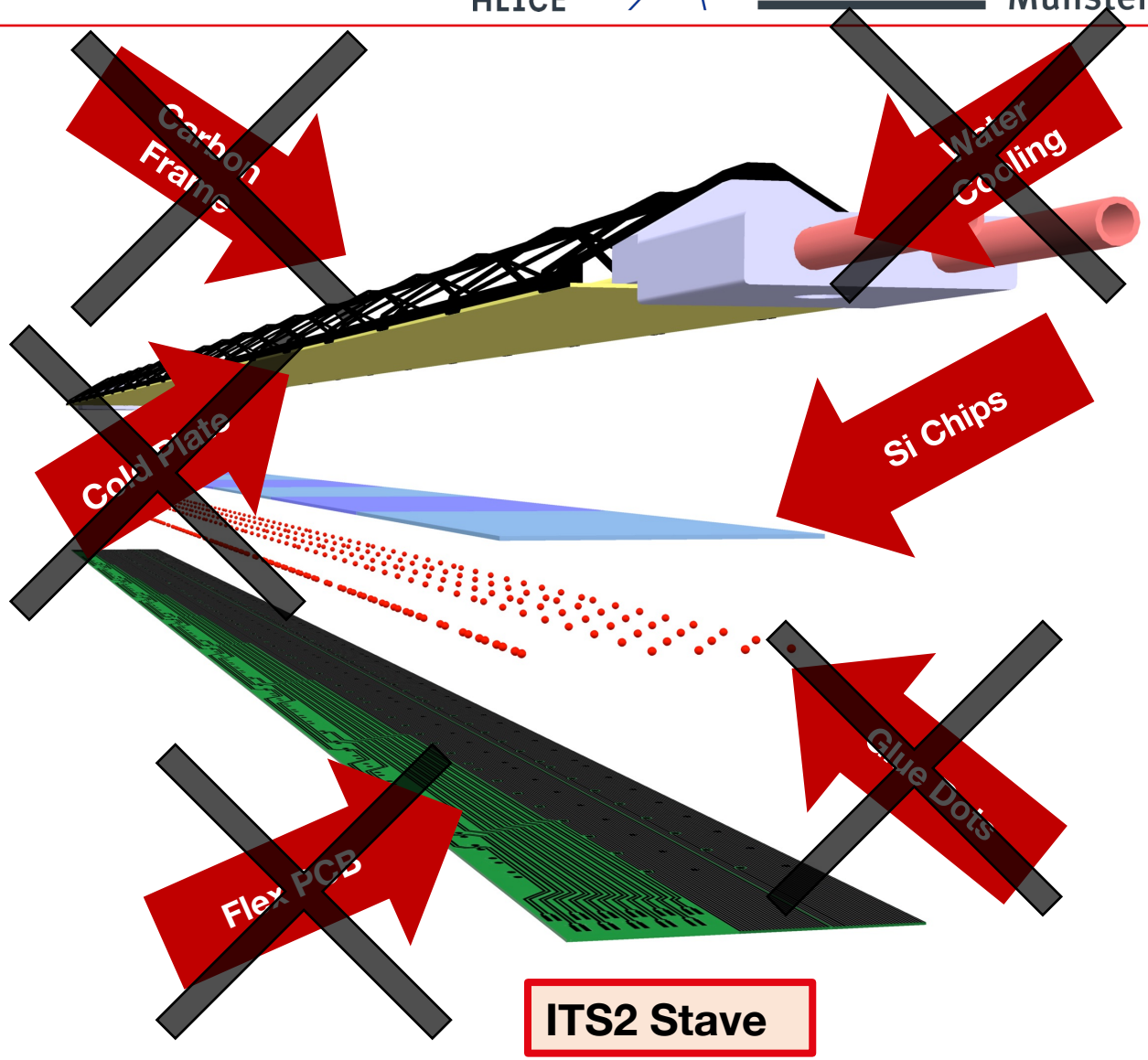
doi:10.1016/j.nima.2021.166280

ALICE ITS

Ideas to save material:

- Lower power consumption → **No water cooling**
- Integrate power and readout lines into chip → **No PCB**
- Bend silicon → Intrinsic stability → **No mechanical support**

Can this be implemented in a single chip?

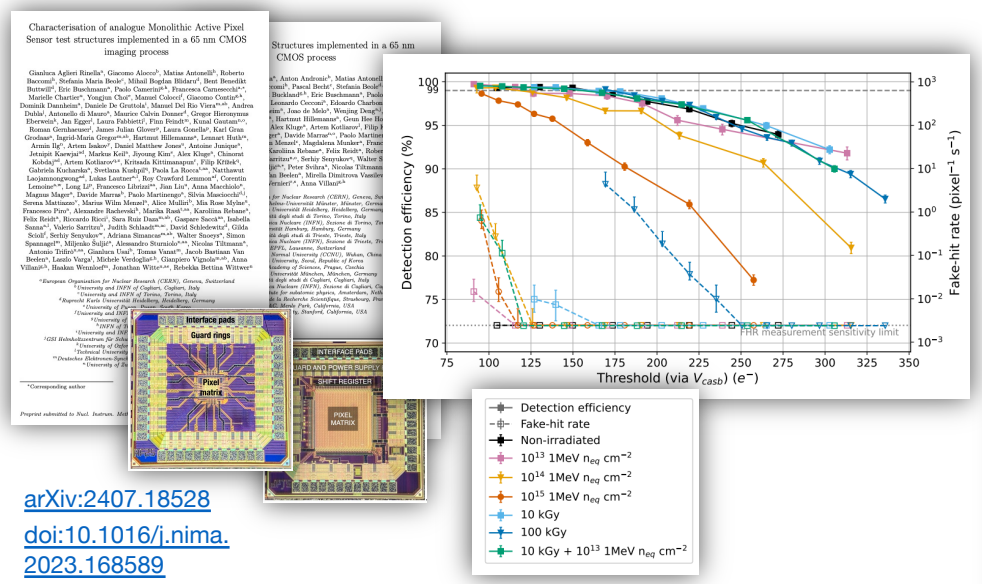


R&D towards ITS3

Key R&D challenges:

Verify efficiency of sensors in TPSCo. 65nm technology

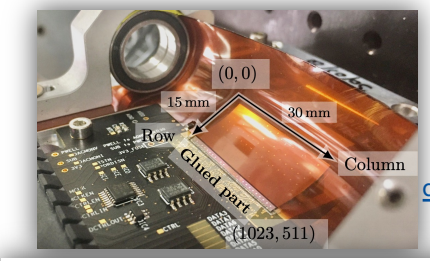
✅ Done with chips from first submission (MLR1)



arXiv:2407.18528
doi:10.1016/j.nima.2023.168589
doi:10.1016/j.nima.2024.169896

Demonstrate operation of bent silicon sensors

✅ Done with bent ALPIDE (ITS2) and MLR1 chips




First demonstration of in-beam performance of bent Monolithic Active Pixel Sensors

ALICE ITS project*

Abstract

A novel approach for designing the next generation of vertex detectors foresees to employ wafer-scale sensors that can be bent to truly cylindrical geometries after thinning them to thicknesses of 20-40 µm. To solidify this concept, the feasibility of operating bent MAPS was demonstrated using 1.5 cm × 3 cm ALPIDE chips. Already with their thickness of 50 µm, they can be successfully bent to radii of about 2 cm without any signs of mechanical or electrical damage. During a subsequent characterisation using a 5.4 GeV electron beam, it was further confirmed that they preserve their full electrical functionality as well as particle detection performance.

In this article, the bending procedure and the setup used for characterisation are detailed. Furthermore, the analysis of the beam test, including the measurement of the detection efficiency as a function of beam position and local inclination angle, is discussed. The results show that the sensors maintain their excellent performance after bending to radii of 2 cm, with detection efficiencies above 99.9 % at typical operating conditions, paving the way towards a new class of detectors with unprecedented low material budget and ideal geometrical properties.

Keywords: Monolithic Active Pixel Sensors, Solid state detectors, Bent sensors

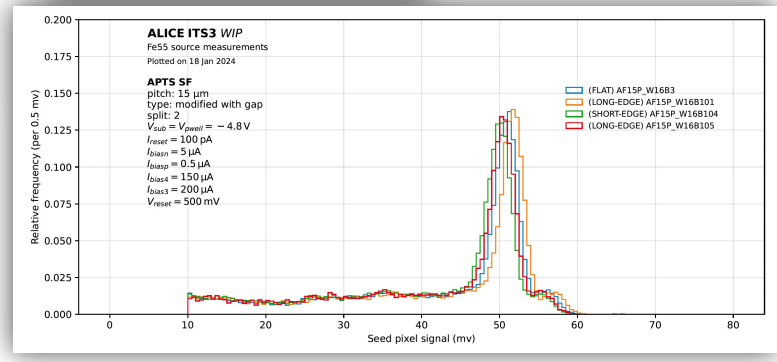
1. Introduction

The precision of barrel vertex detectors is mainly determined by three contributions: their radial distance to the interaction point, their material budget, and their intrinsic sensor resolution. In order to achieve hermiticity, they are typically built out of detector staves placed in layers around the beam pipe. This arrangement effectively sets a practical limit on the first two factors. ALICE, for instance achieves an average radial position of 24 mm and a material budget of 0.3 X_0 for its new Inner Tracking System (ITS2) [1]. More than 80 % of the material is due to the support structure, and the average distance is determined

*See Appendix Appendix A for the complete list of authors.

Preprint submitted to Nucl. Instrum. Methods Phys. Res. A August 18, 2021

doi:10.1016/j.nima.2021.166280



Demonstrate stitching

➡️ Done with chips from second submission (ER1)

➡️ Next slides!

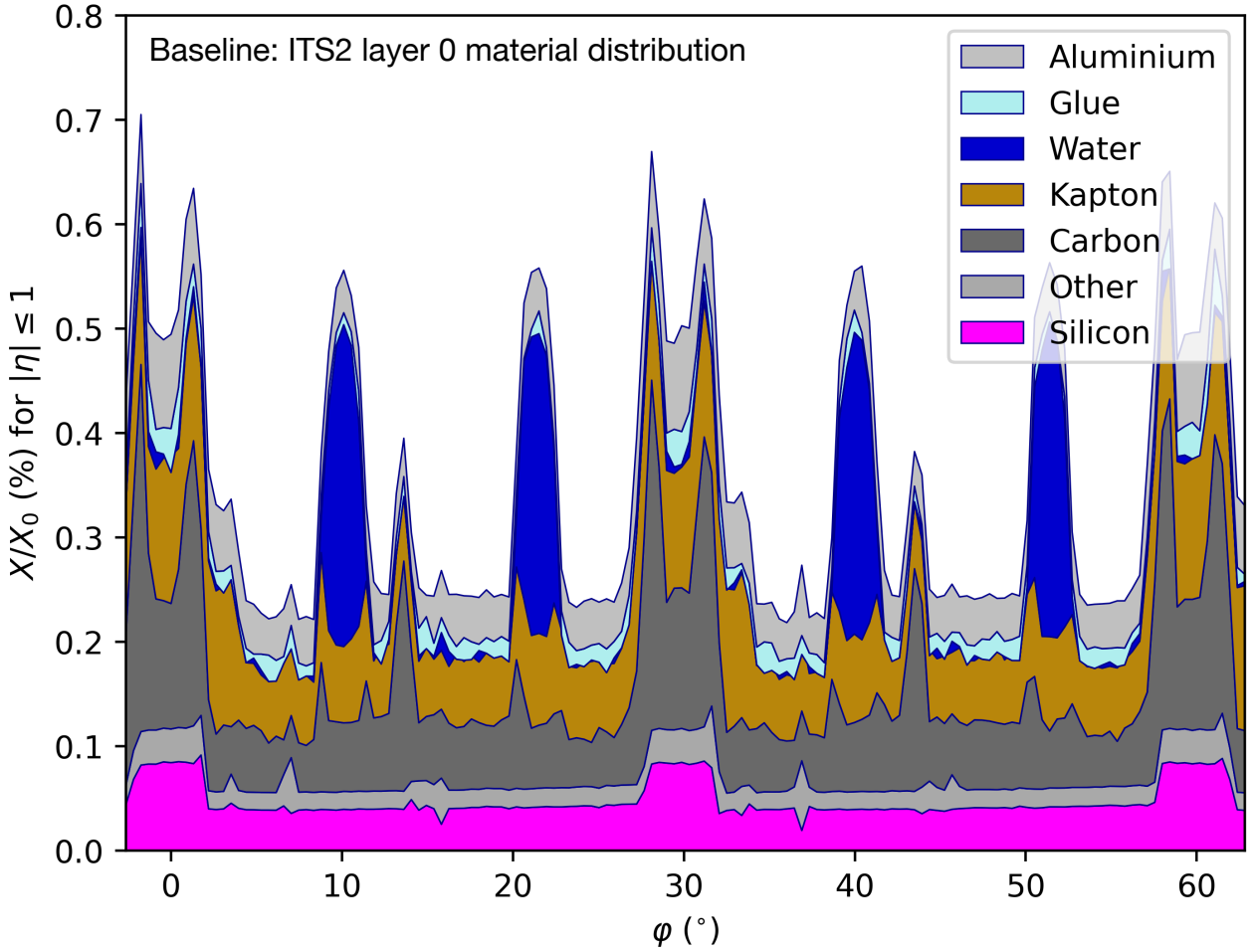
➡️ **Lead to completion of Technical Design Report (TDR)!**
CERN-LHCC-2024-003

ALICE ITS

Ideas to save material:

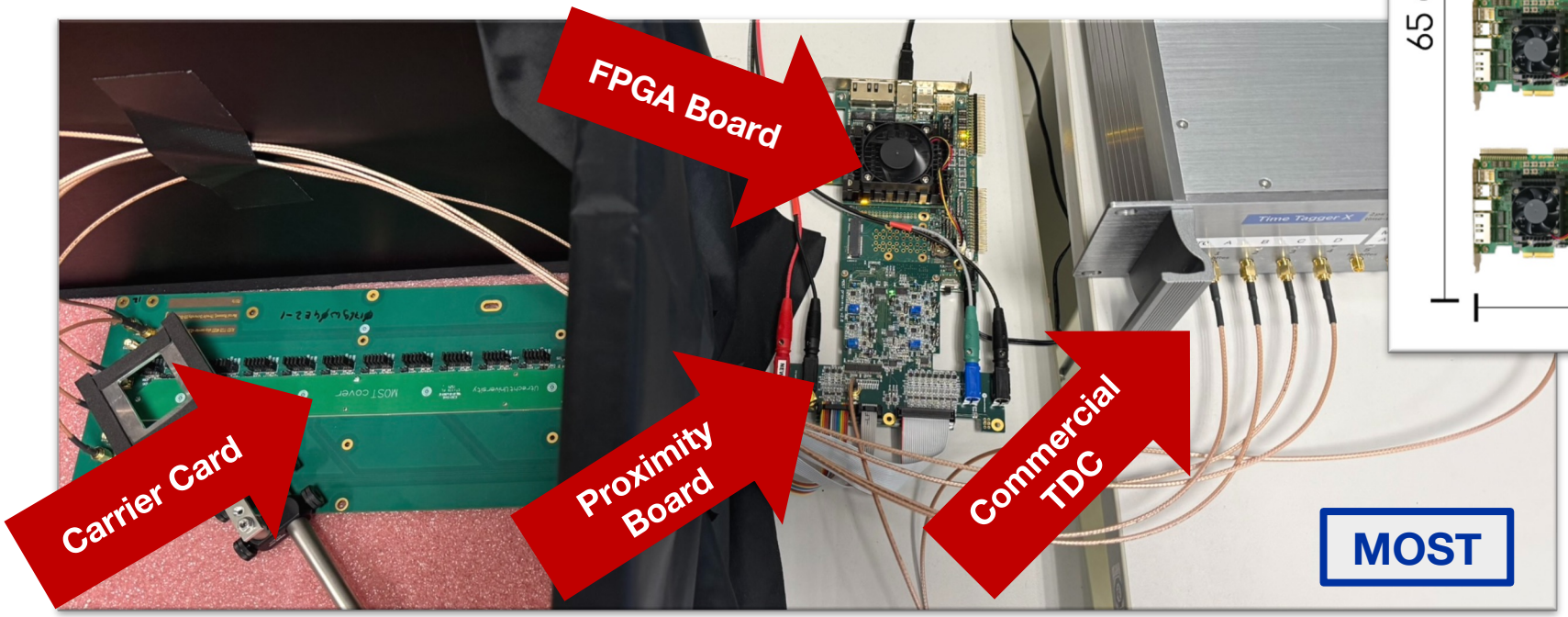
- Lower power consumption → **No water cooling**
- Integrate power and readout lines into chip → **No PCB**
- Bend silicon → Intrinsic stability → **No mechanical support**

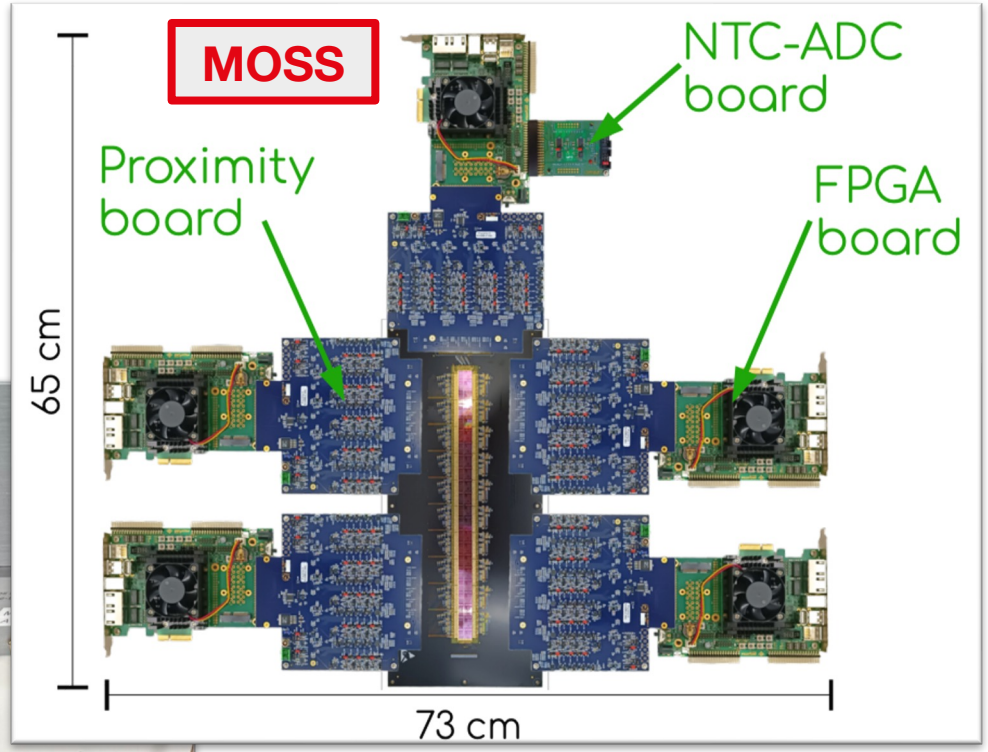
Can this be implemented in a single chip?



Test System Lab Tests

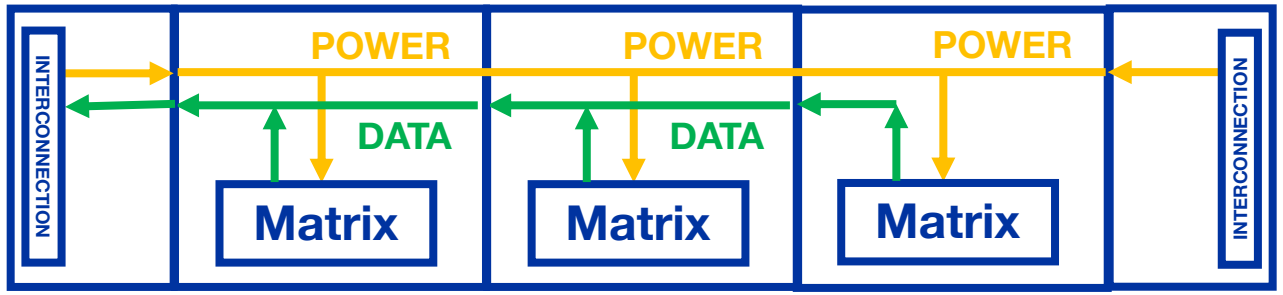
- Commercial FPGA boards
- Custom Proximity Board with ADC, DAC, …

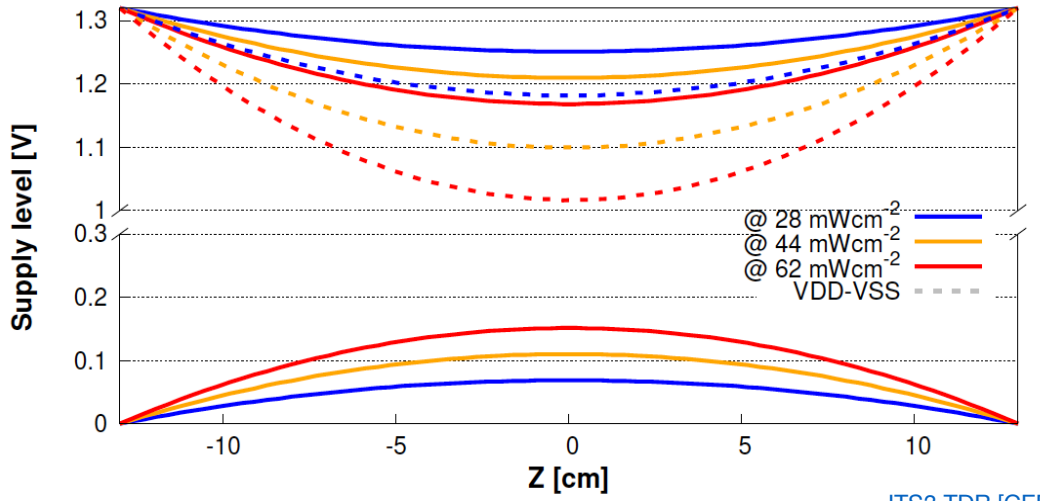




Ongoing R&D

- Power is distributed by metal strips on-chip
- Voltage drop scales…
  - …quadratically with distance
  - …linearly with power density
- Power chip from both endcaps!
- Keep power density low!
  - Max. ≈40mWcm $^{-2}$ in matrix for 0.2V voltage drop



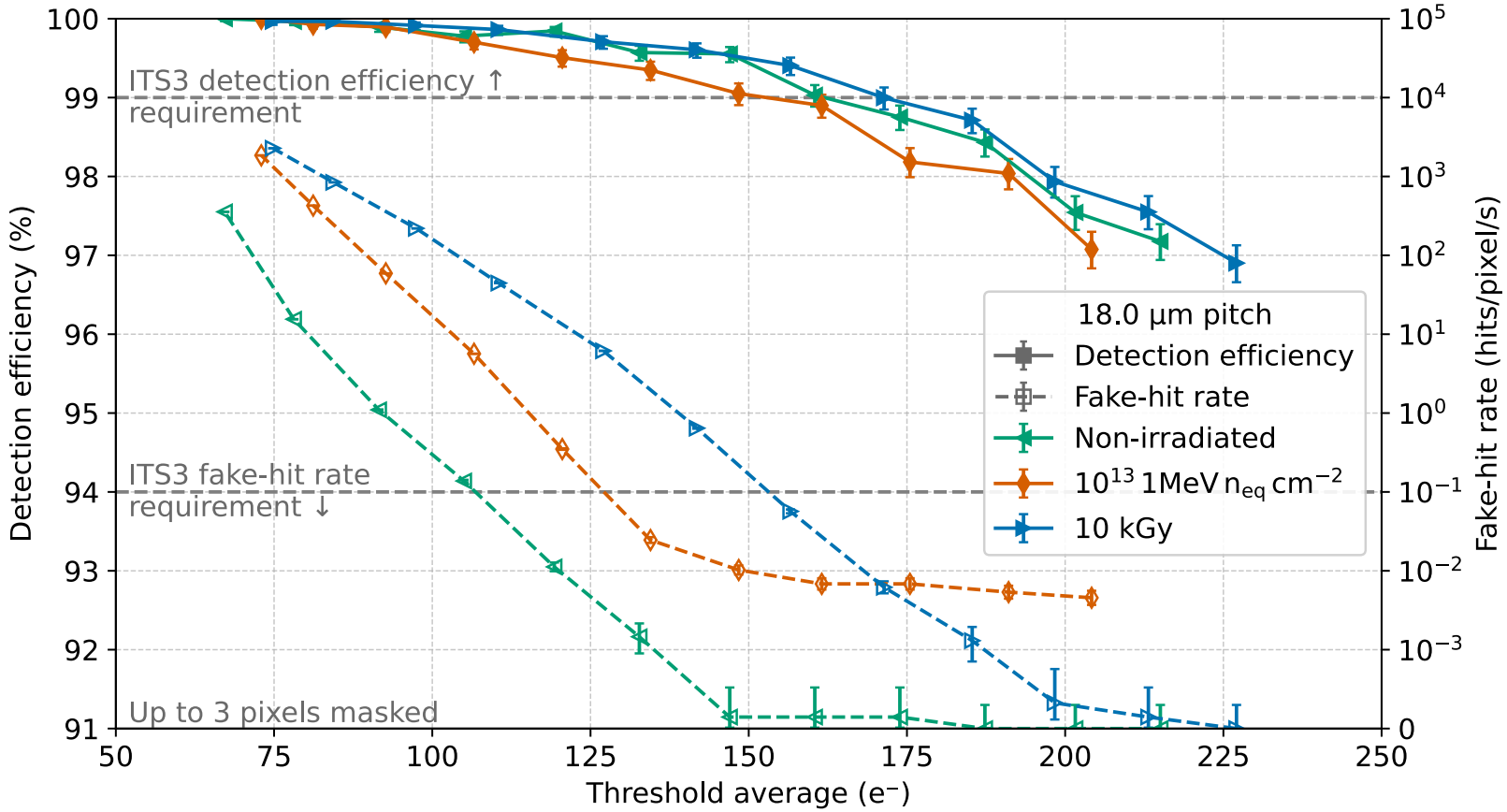


(n.b. this already includes modified (thicker) metal stack for ER2/MOSAIX)

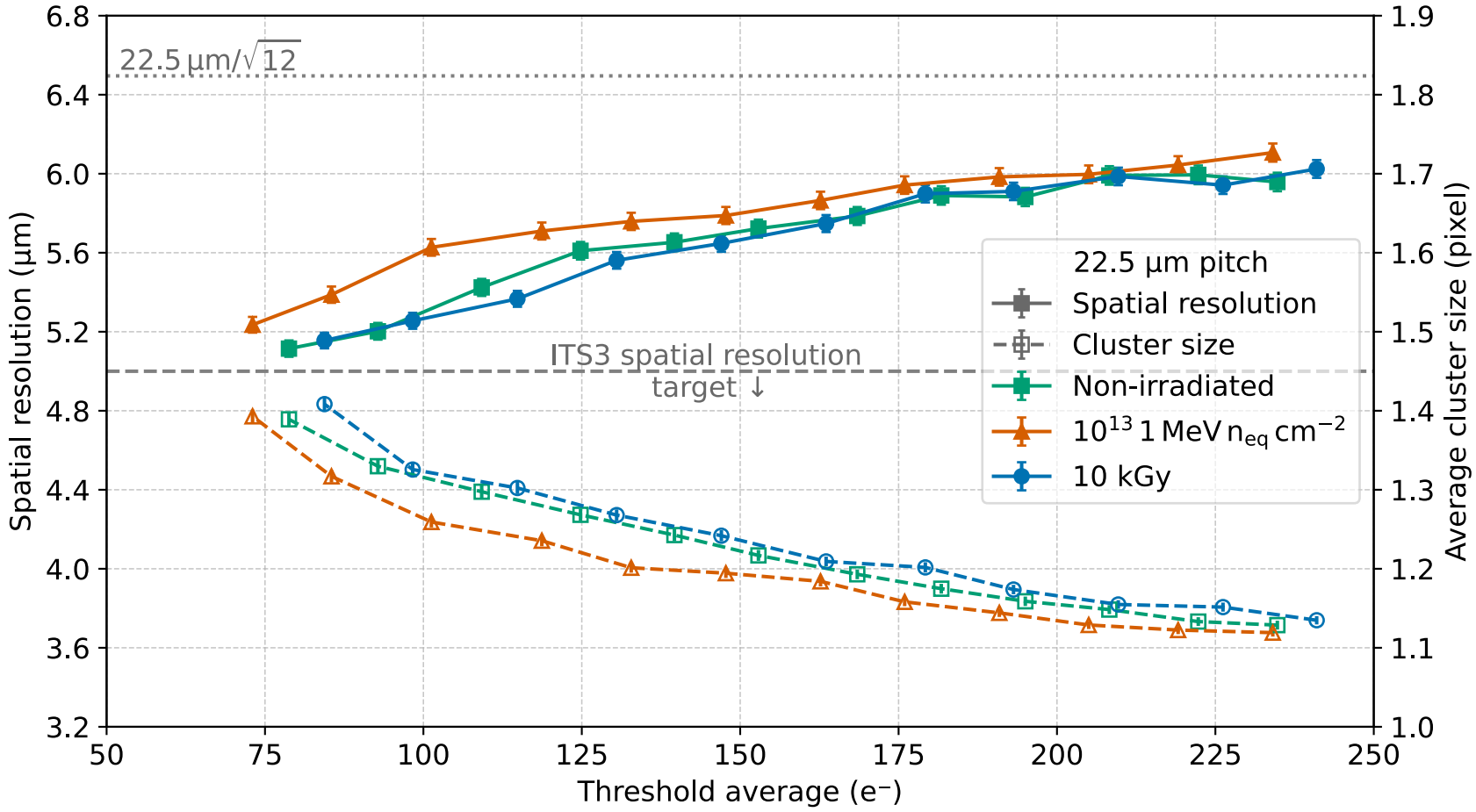
ITS3 TDR [CERN-LHCC-2024-003]

Testbeam Results

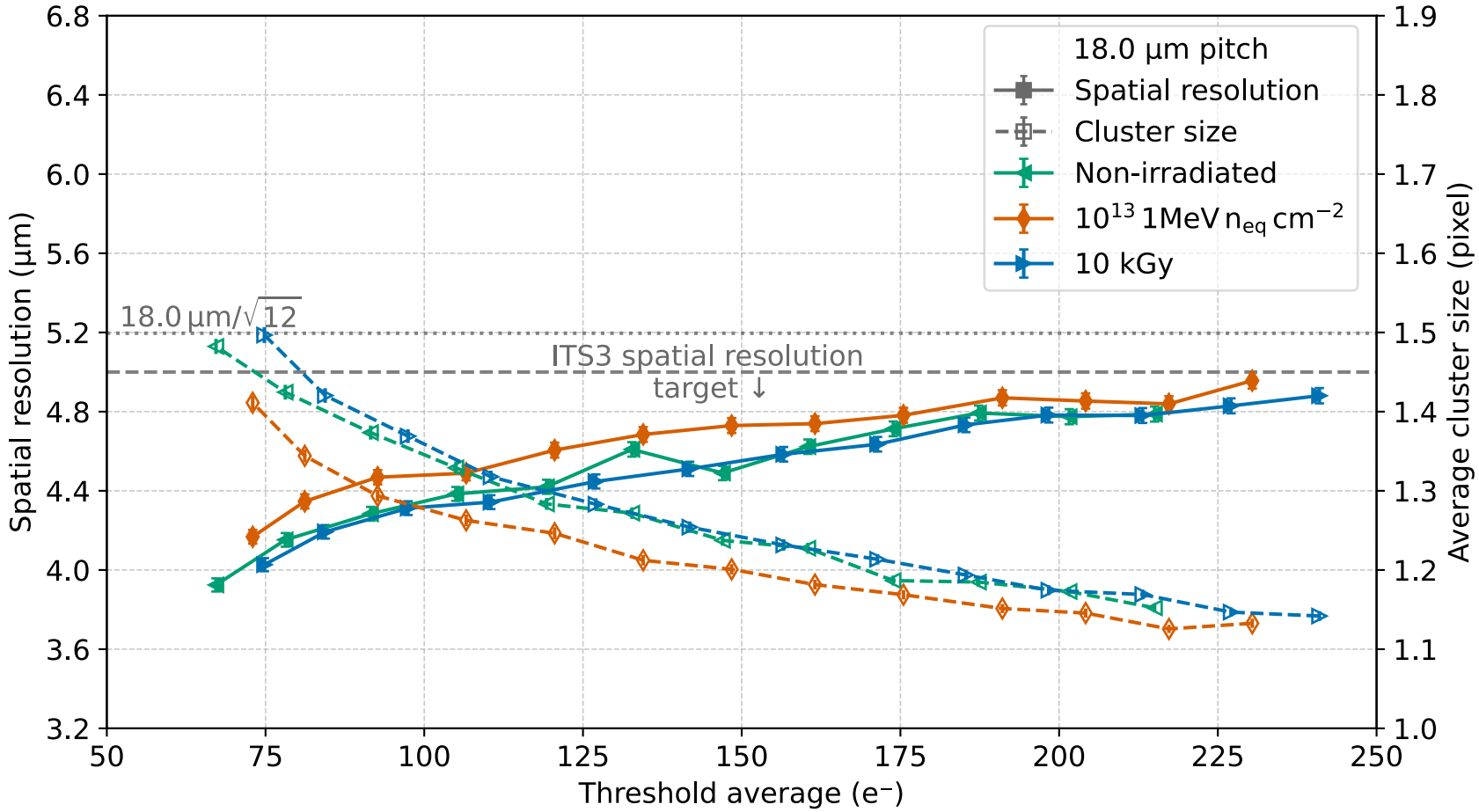
- Extensive effort of in-beam characerization
  - 16 weeks of beam time in 2024 and 2025
- Degradation of efficiency after NIEL
- Degradation of FHR after TID
- Still **sufficent operational margin** at **ITS3 rad. Levels!**



Testbeam Results

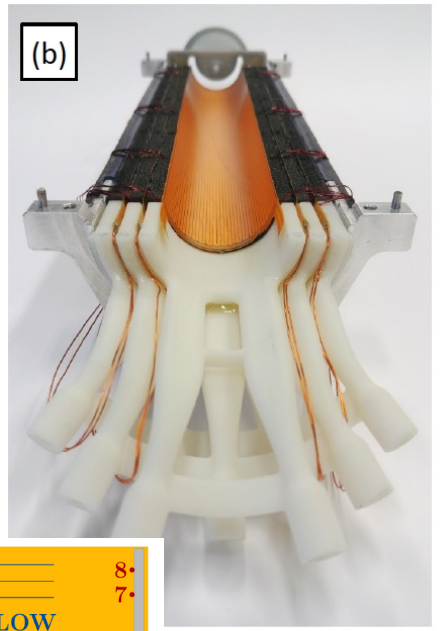


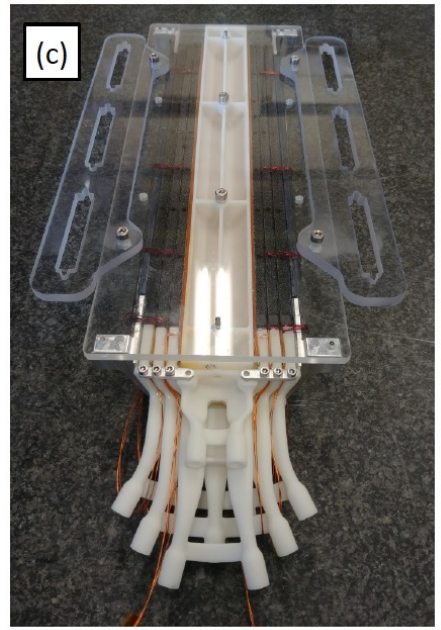
Testbeam Results

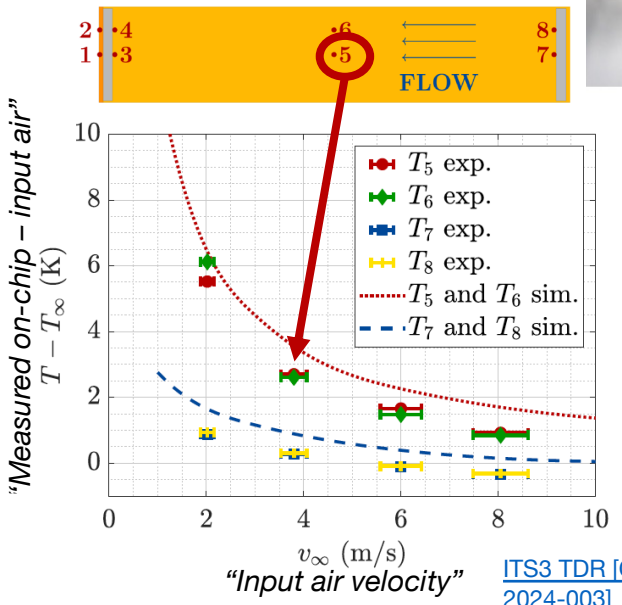


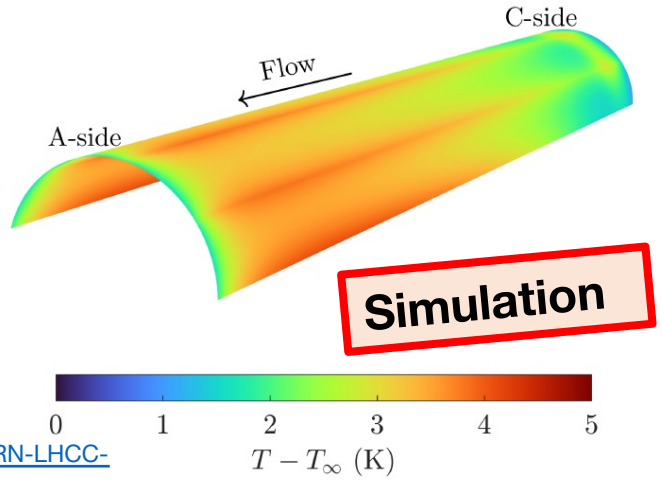
Ongoing R&D

- Low power density also needed for air cooling
- Breadboard model for thermal characterization
  - Copper heating traces on silicon in polyimide
  - Validates simulation model
- Detailed simulation
  - Advanced model: Additional periphery in z-direction
  - **Temperature variation can be kept <5K** for different power densities



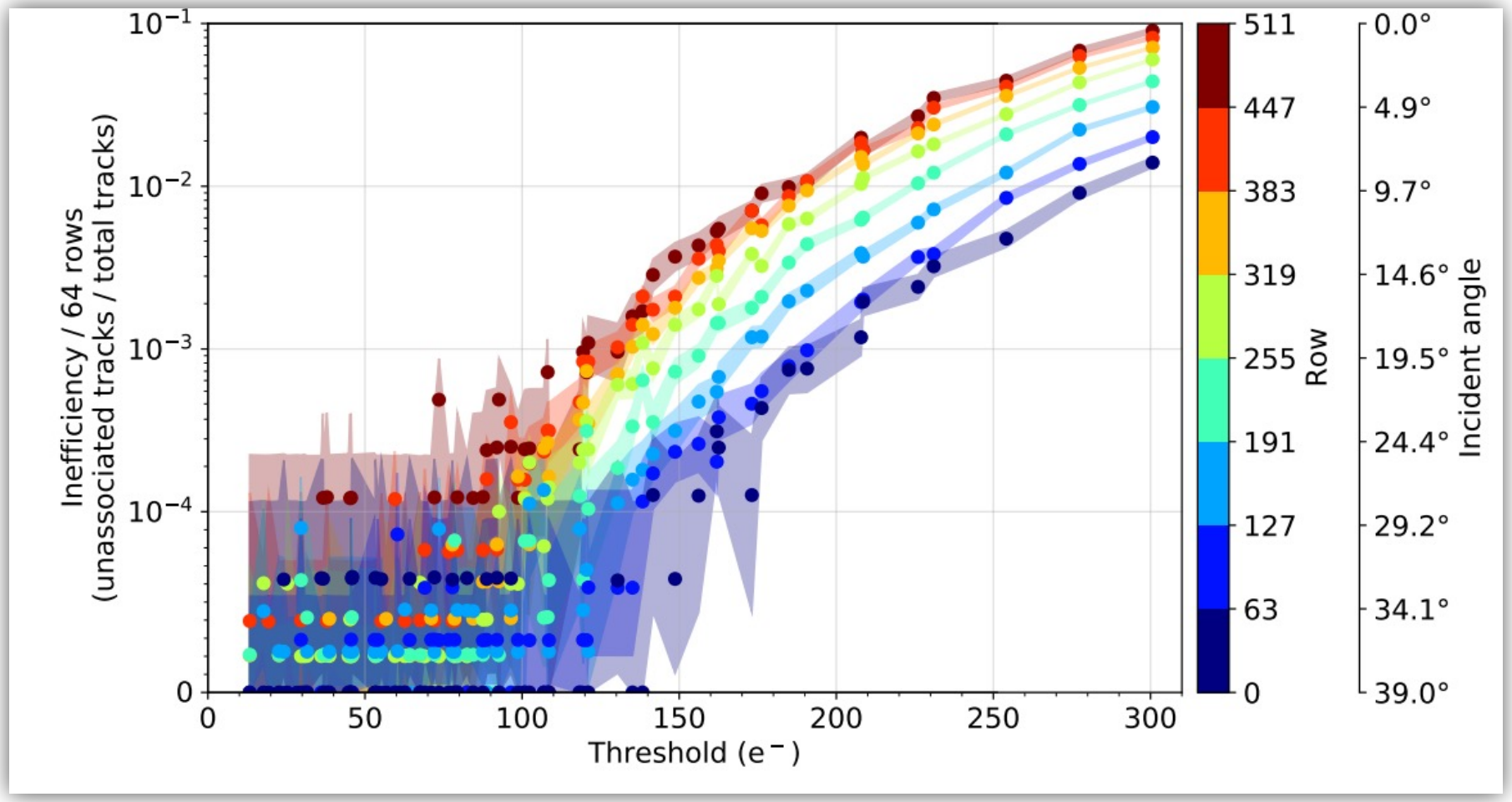






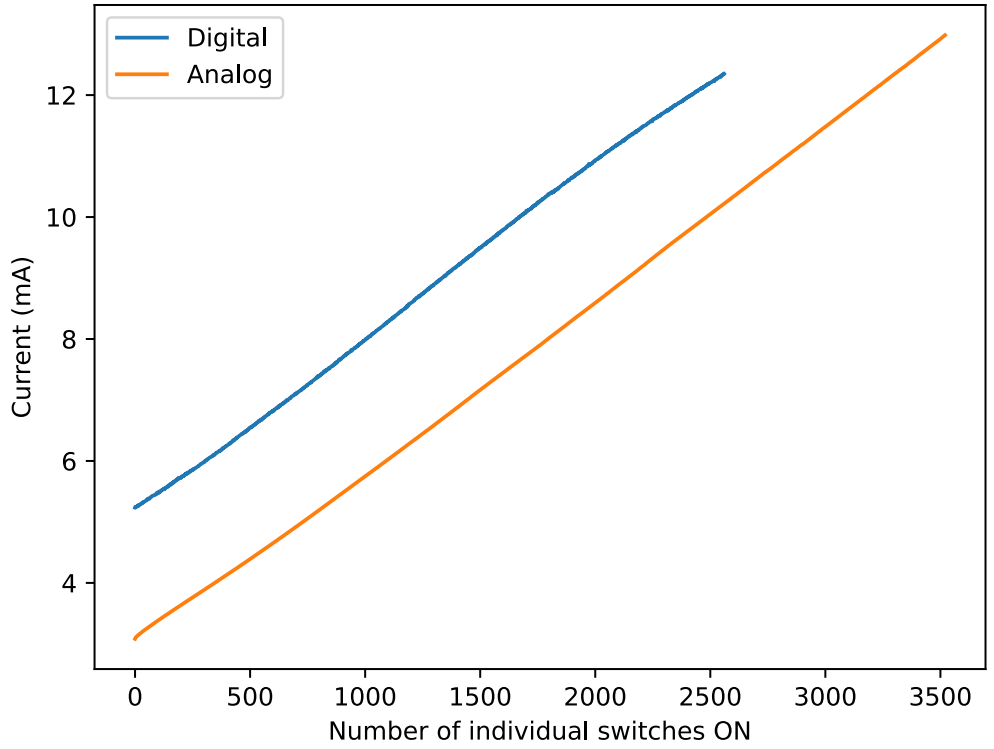
[ITS3 TDR [CERN-LHCC-2024-003]]

Bent ALPIDE


Inefficiency / 64 rows
(unassociated tracks / total tracks)
10^{-1}
10^{-2}
10^{-3}
10^{-4}
0
0
50
100
150
200
250
300
Threshold (e^-)
511
447
383
319
255
191
127
63
0
Row
0.0°
4.9°
9.7°
14.6°
19.5°
24.4°
29.2°
34.1°
39.0°
Incident angle

Power Gating

- Analog: 1x switch per 4 rows (256 px)
- Digital: 1x switch per 352 px
- Uniform increase in current consumption, no jumps



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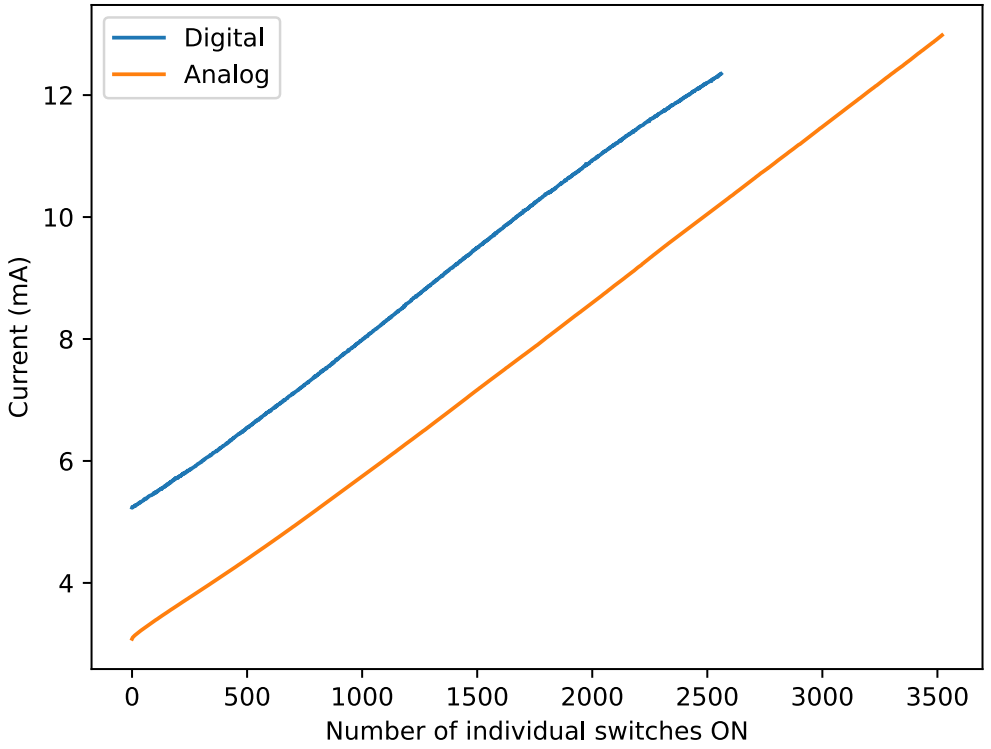
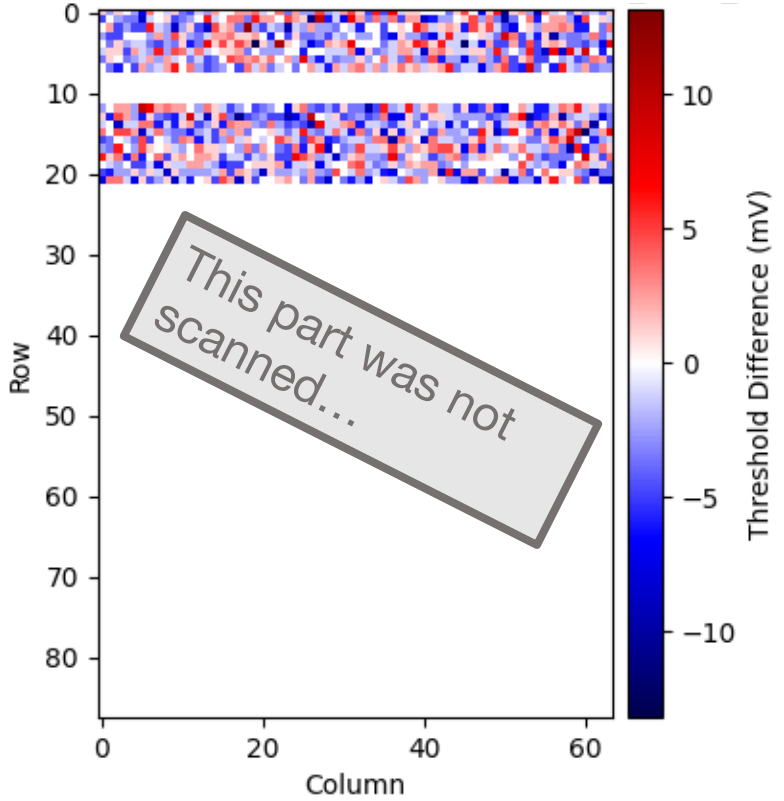




Threshold scan of 22 rows:

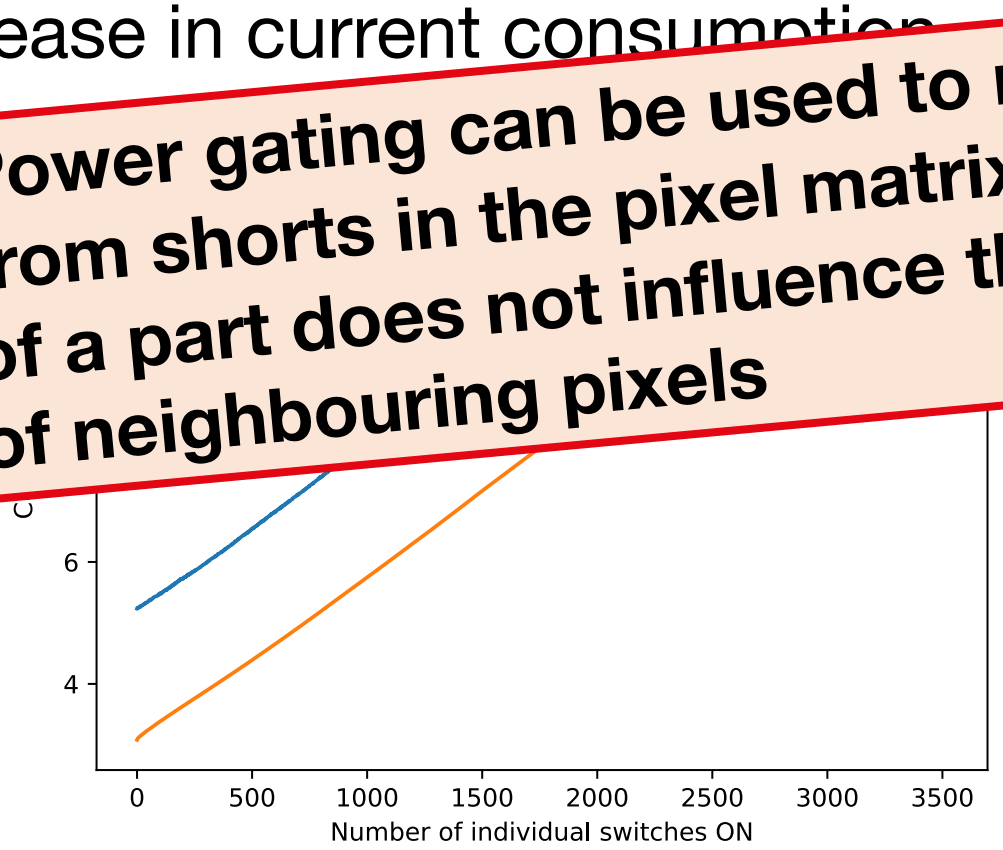
a) Rows 8-11 **masked** (front-end digital output not propagated)

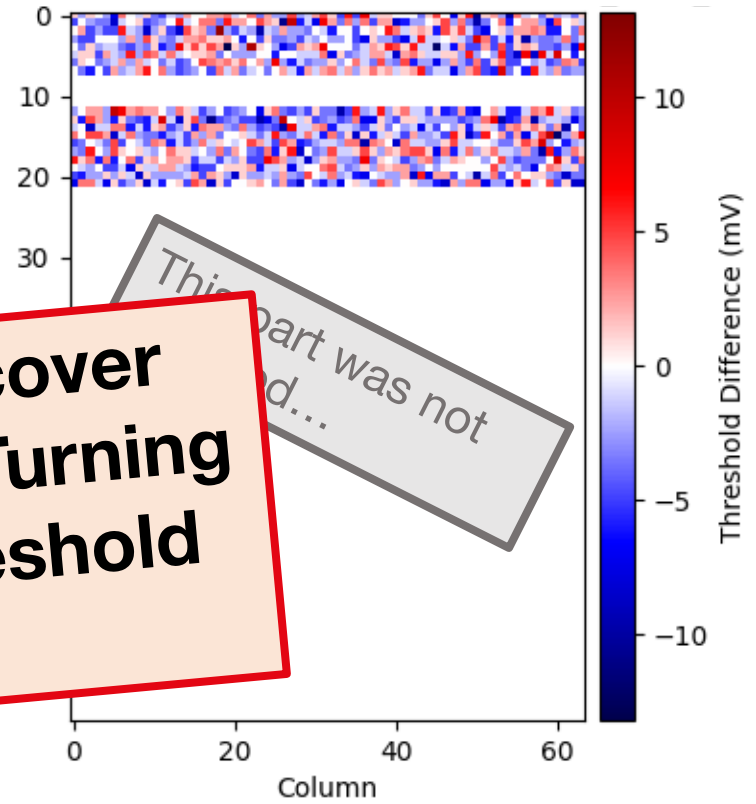
b) Rows 8-11 **off** (analog front-end not powered)

Power Gating

- Analog: 1x switch per 4 rows (256 px)
- Digital: 1x switch per 352 px
- Uniform increase in current consumption, no jumps

Power gating can be used to recover from shorts in the pixel matrix. Turning of a part does not influence threshold of neighbouring pixels





Threshold scan of 22 rows:

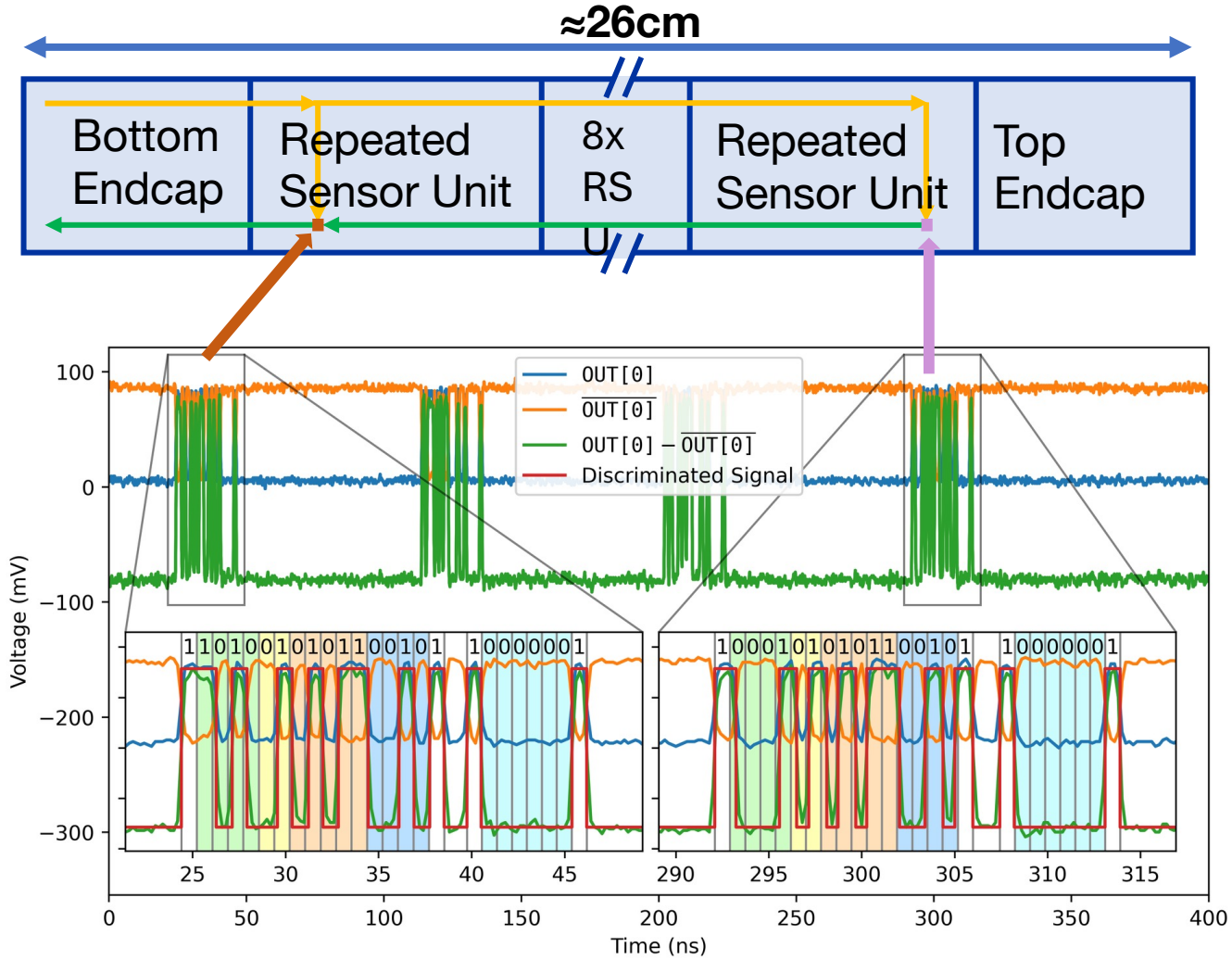
a) Rows 8-11 **masked** (front-end digital output not propagated)

b) Rows 8-11 **off** (analog front-end not powered)

On-Chip Data

MOST: Verification of data transmission across **long on-chip lines**

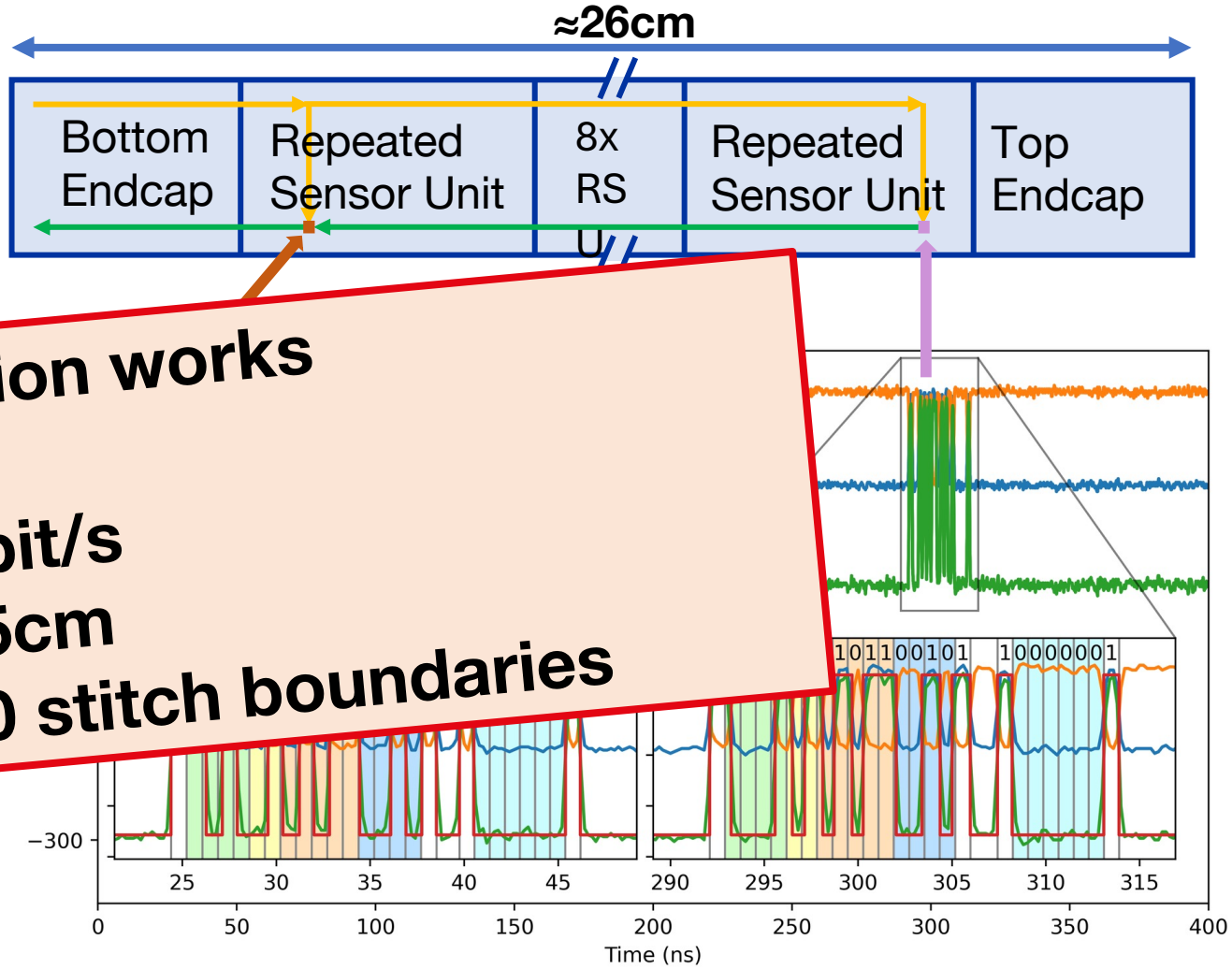
- Pulsing and readout of pixel in different stitches
- Propagation delay (pulsing + readout) approx. 300 ns
  - Caused by buffering on chip
- Signal integrity maintained!



On-Chip Data

MOST: Verification of data transmission across **long on-chip lines**

- Pulsing and readout from
  in different s
- Propagation
  + readout) ap
  - Caused by
- Signal integrity maintained!



Data transmission works

a) on-chip
b) with ≈1Gbit/s
c) along ≈25cm
d) across 10 stitch boundaries