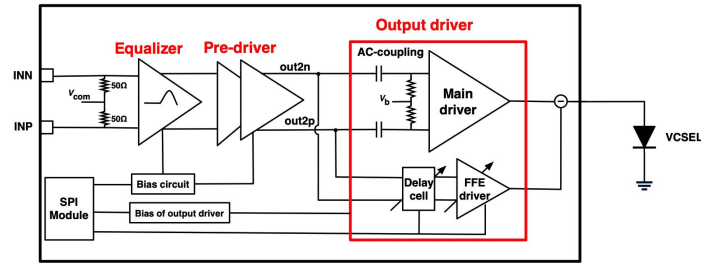
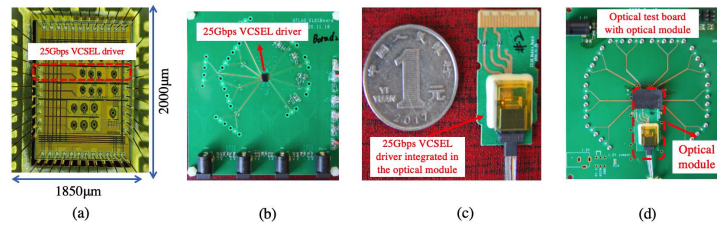


# Supporting document



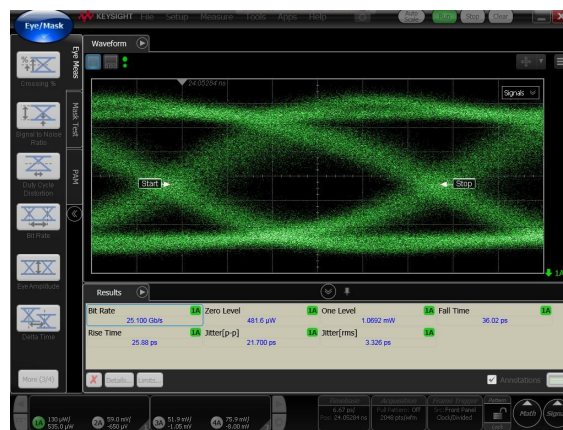
**Figure 1 Block diagram of 25Gbps VCSEL Driver ASIC**

The block diagram of the 25 Gbps VCSEL driving ASIC is shown in Figure 1. It includes an input equalizer stage, a pre-driver stage and a novel output driver stage. The proposed output driver stage includes a main driver, an adjustable delay cell and an emphasis driver (FEE driver). The main driver converts the amplified differential voltage signals from the pre-driver to single-ended high speed current signal, and drives the external VCSEL.



**Figure 2 Test chip micrograph**

The chip micrograph is shown in Figure 2 (a). The 25 Gbps VCSEL driver has been tested in both the electrical test and the optical test, and two corresponding test boards have been designed, as shown in Figure 2 (b)-(c).



**Figure 3 25Gbps optical eye diagram**

In the optical test, the 25 Gbps VCSEL driver is integrated with the real VCSEL, and the final optical eye diagrams have been recorded. Figure 3 shows the recorded 25 Gbps optical eye diagram at the optimized settings. The measured RMS jitter of 25 Gbps optical eye is 2.9 ps and the peak-to-peak jitter is 19.5 ps.