

## **Monolithic integration of cooling microchannels in silicon wafers with BEOL layers**

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### **Abstract**

Future vertex colliders will require detector solutions that minimize material budget, which will be achieved by further integration of detectors, electronics and services. CMOS detectors have been proposed as a breakthrough solution for integration in particle physics experiments. The increased integration level combined with the subsequent higher channel density, and the high-performance processing of the sensor and electronics, will impose important challenges for the heat removal in these systems. Therefore, in order to build successful experiments, the cooling strategy will have to be considered from the beginning and will also need to comply with the low material budget and high integration level required for the whole system. Microchannel cooling has been proposed as a high efficiency, low mass, and high integration, heat removal method for detectors and electronics. Microfluidic cooling solutions have already been implemented in current experiments and in high performance computing (HPC) applications which make use of silicon cooling plates or cooling interposers attached very close to the detectors and electronics, which provide very high heat transfer efficiency and good integration features.

The next step in integration and heat removal capabilities is the full monolithic integration of the cooling microchannels in the CMOS substrate. Our work aims to this solution in which microchannels are incorporated in a 'post-processing' step to the CMOS detector substrate for particle physics applications. The work we will present here is a fundamental step in this direction, in which microchannels are incorporated in a "pure post-processing" way, to silicon wafers with aluminum tracks already created on them. This is a critical achievement because the Back-End of Line (BEOL) layers of the CMOS technology are the most sensitive to the processes involved in the creation of microchannels (DRIE or wafer bonding) due to the use of plasma processes, high pressures, high voltages, or temperature steps. Front-End of Line (FEOL) layers, like implants or isolation layers, as oxides or nitrides, are insensitive to these post-processing treatments. We will present the technological steps needed, the different technological options available, and the protective measures taken for the post-processing integration of cooling microchannels in silicon wafers with BEOL layers already present. We will also discuss the results obtained from the fabricated prototypes and the different challenges for the future monolithic integration of microchannel cooling in CMOS detectors.