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Monolithic Integration of Cooling Microchannels in Silicon Wafers with BEOL layers

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…and the invaluable contribution of the personnel of IMB-CNM's Micro-Fabrication Facility

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Outline

1. Framework / Motivation
2. Heterogeneous and Monolithic Integration
3. Past and Current Work
4. Fabrication
5. Challenges
6. Results
7. Summary
8. Future Work

Framework / Motivation

- Requirements on the dimensions of integrated circuits are pushing the limits of manufacturing
  - Electronic devices becoming smaller
  - Growth of integration densities

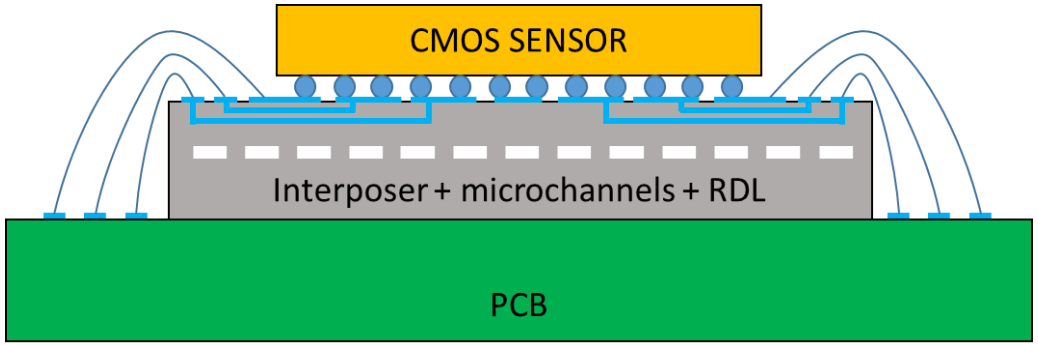
  → **Increase of power densities**
- Need to keep silicon detectors at low temperature in High Energy Physics (HEP) experiments
  - Radiation damage
  - Temperature

  → **Increase of leakage current** →
  - Partial depletion
  - Thermal runaway
- Different cooling solutions (air, liquid, bi-phase), but usually require **complex setups at module level**
  - Technology limits for pipe reduction and coverage
  - Thermal connection with sensors and electronics
  - Complex assembly process

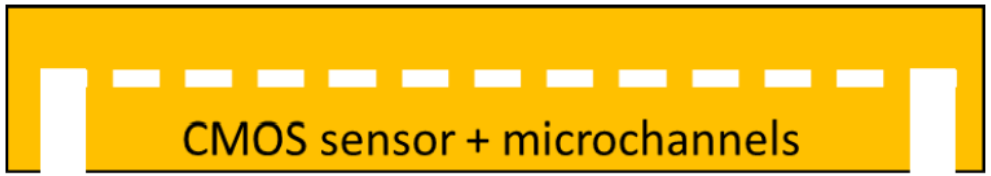
➢ **Microchannel technology provides local and high-efficient cooling**
  - In electronics: Handling high power densities, Efficient heat transfer, Scaling, …
  - In HEP and other Physics facilities: Material/Mass reduction, Minimum CTE mismatch, Cooling of large areas, Non-uniform heat removal, High heat removal capacity, …

Heterogeneous and Monolithic Integration

- Investigating different applications:
  1. **Heterogeneus Integration**: Silicon interposers with embedded microchannels and integrated signal and power routing (re-distribution layer, RDL)

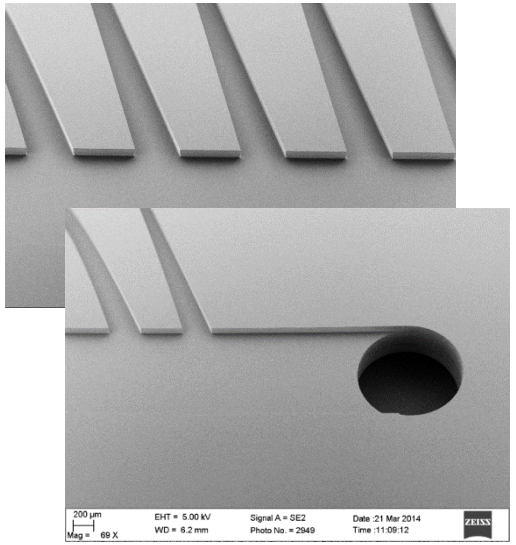


  2. **Monolithic Integration**: Wafer-level post-processing to incorporate micro-channels in CMOS sensors



Past and Current Work

- ✓ Basic technology: Development of embedded microchannel cooling for HEP detectors
  - N. Flaschel, et al. NIMA, vol. 863, pp. 26-34, 2017. http://dx.doi.org/10.1016/j.nima.2017.05.003
  - Ph.D Thesis Nils Flaschel. Hamburg University. 2017. https://bib-pubdb1.desy.de/record/396403

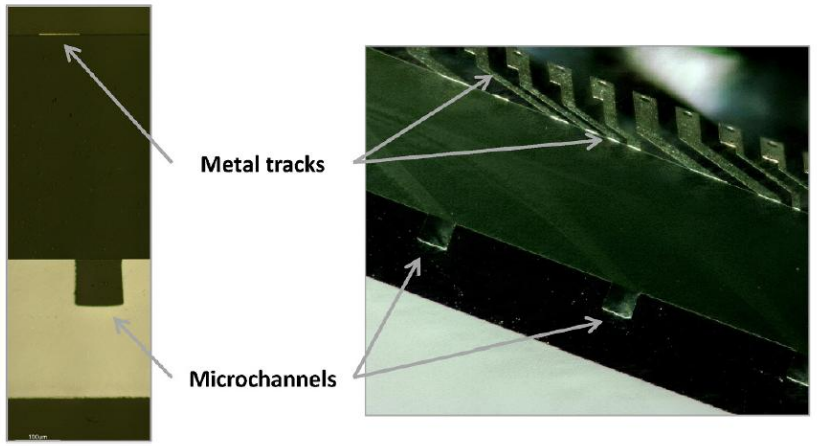


Developments in collaboration with:

DESY. | IFIC INSTITUT DE FÍSICA CORPUSCULAR

Participation in:
- AIDAInnova
- DRD7 (3D Integration)
- DRD8 (Cooling)

- ✓ Heterogeneous integration: Successful integration of microchannels in silicon interposers with signal/power re-distribution layer (RDL)
  - M. Ullán, et al. NIMA, vol. 1065, 169490, 2024. https://doi.org/10.1016/j.nima.2024.169490



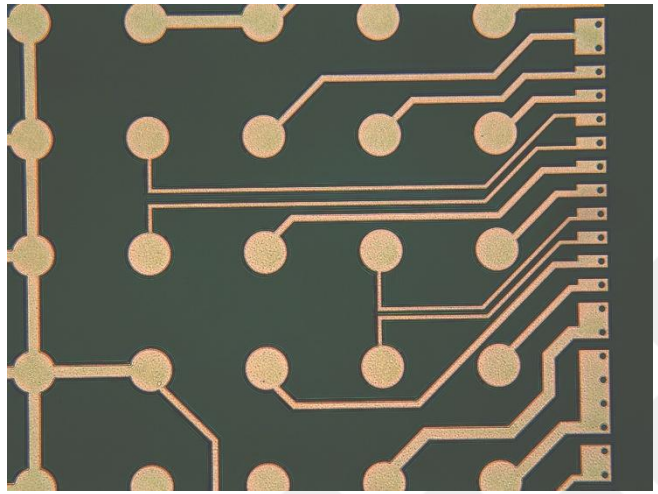
- ❑ **Monolithic integration: This work presents the developments for the full monolithic integration of cooling microchannels in a CMOS substrate**

Fabrication – CMOS Metal

- **CMOS compatibility**
  - **Back-End of Line (BEOL) layers** of the CMOS technology are **the most sensitive to the processes involved** in the creation of microchannels (plasma processes, high pressure/voltage/temperature)
  - **Front-End of Line (FEOL) layers** (implants or isolation layers) **insensitive** to these post-processing treatments
  - 'Post-processing': Microchannels incorporated to silicon substrate with aluminum tracks
  - Quality of the metal at the end of the fabrication is a **critical achievement towards CMOS compatibility**

<u>Objective</u>: Emulation of Back-End of Line (BEOL) metal layer of a CMOS sensor

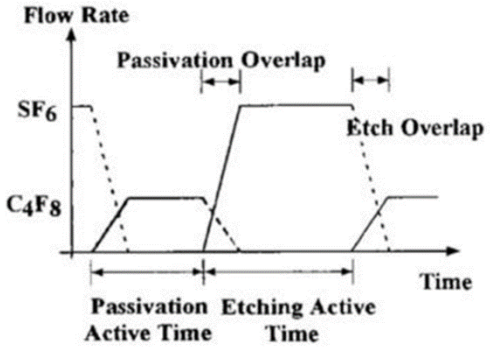
- Sputtering process with *Kenosistec KS800H*
  - Sputtering system to deposit metallic layers
  - Target used: Al (99.5%) / Cu (0.5%)
  - Other targets available: Au, W, Ti, …
  - Better adherence than evaporative process

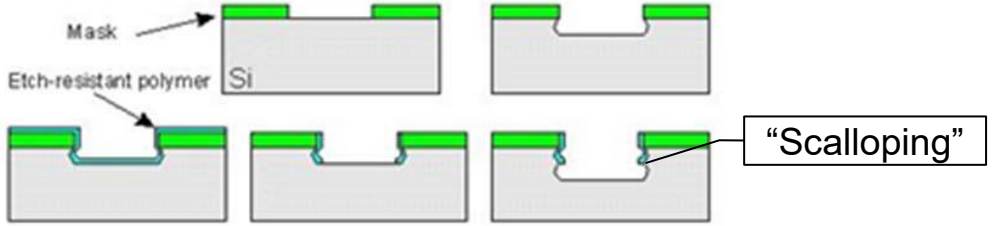


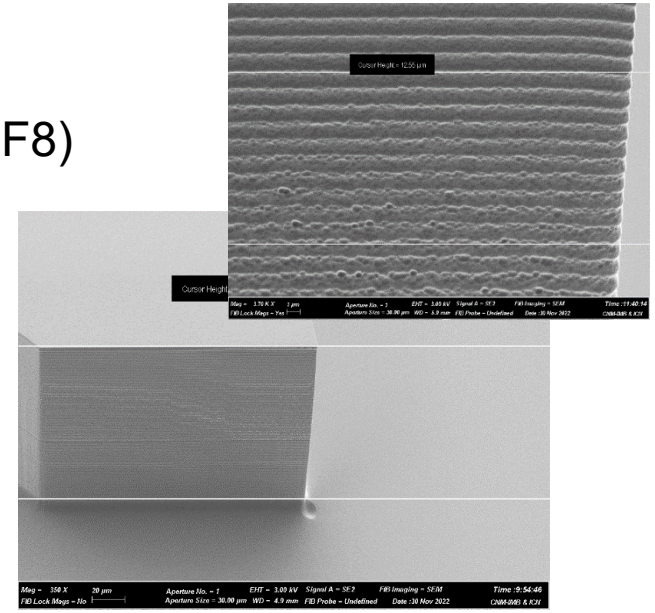
Fabrication – Microchannels/Holes

<u>Objective</u>: Creation of microchannels (trenches) and coolant I/O (through holes)

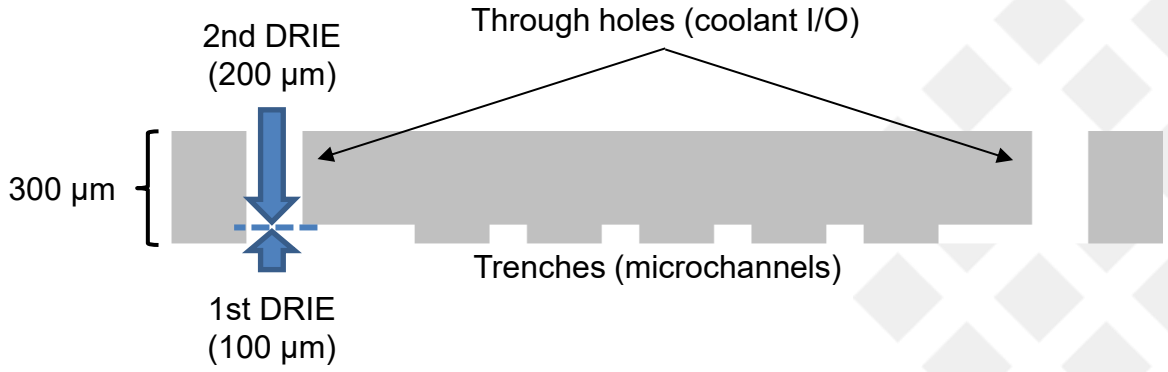
- Deep Reactive-Ion Etching (**DRIE**) with *Alcatel 601E*
  - Chemical-Physical etch of silicon
  - Very anisotropic → high aspect ratio (deep and vertical holes)
  - Bosch process: alternating between etching (SF6) and passivation (C4F8)







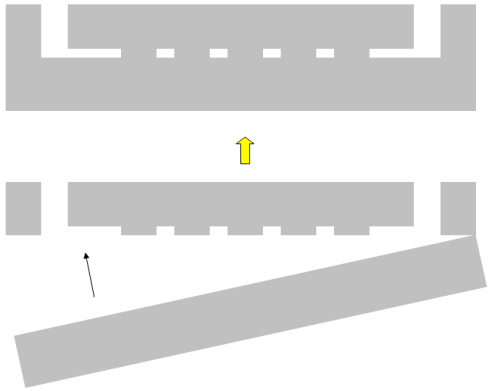
- **Two Si-etching processes**
  - 1st to create the channels (100 µm deep)
  - 2nd to form the inlet and outlet:
    - Through hole
    - "double-side" alignment

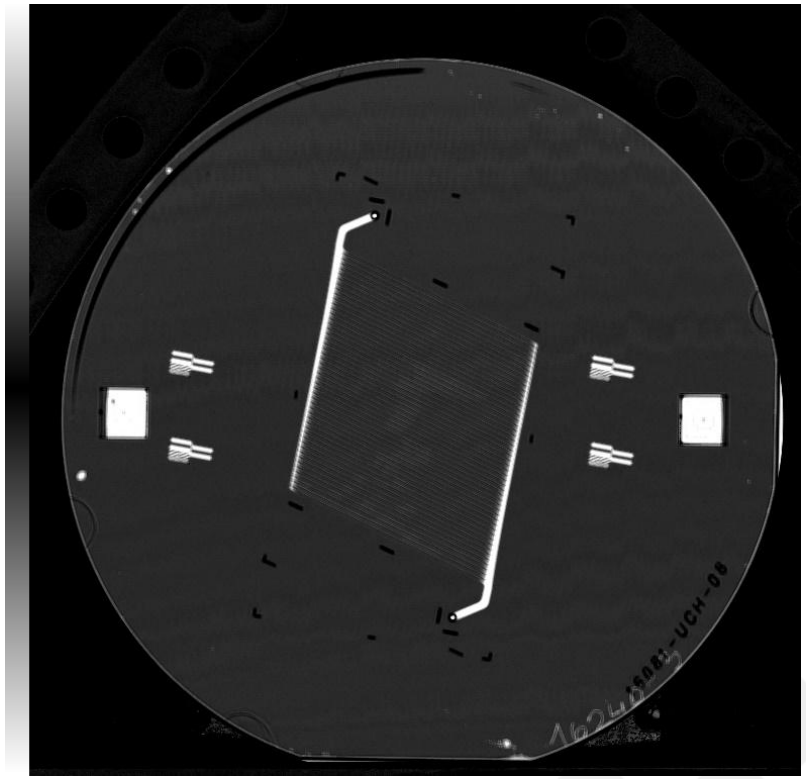


Fabrication – Wafer Bonding

Objective: Wafer bonding to complete the buried microchannels

- Wafer bonding with *Süss Microtec SB 6e Substrate Bonder*
- **Anodic bonding** (Borosilicate Glass – Si)
  - High V (1000 V)
  - Low T (~350 ºC)
  - PYREX®, MEMpax®
- Process **optimized for 4-inch wafers at 350 ºC**

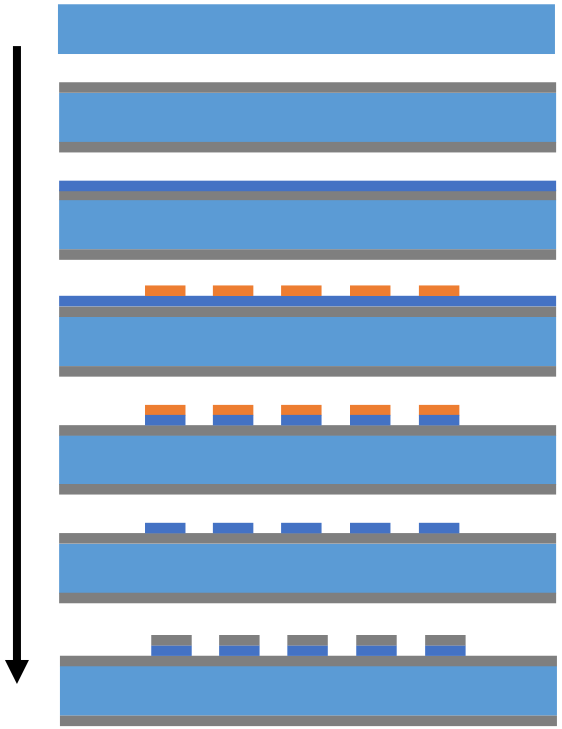




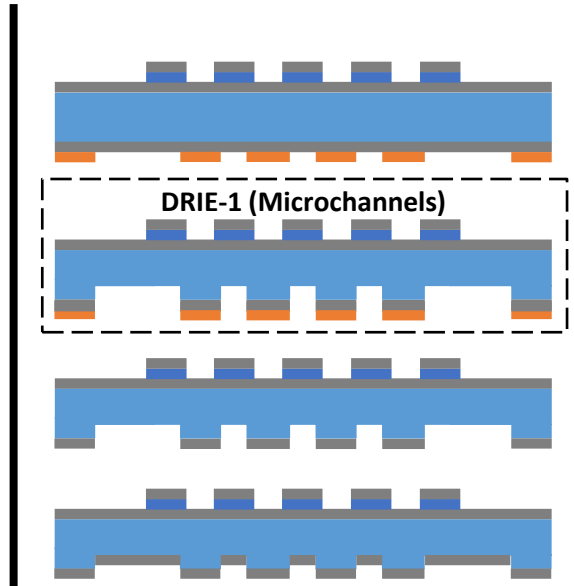
- Also, **investigating alternative solutions**
  - Different bonding techniques: Eutectic (Si/Metal/Si), Fusion (Si/Si), …
  - 6-inch Wafer2Wafer bonding
  - Die2Wafer / Die2Die bonding

Fabrication – Full Process

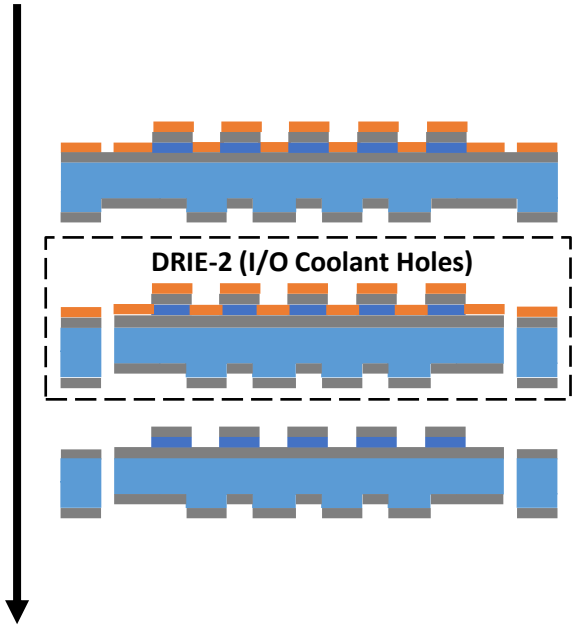
1. Creation of CMOS-like BEOL metal



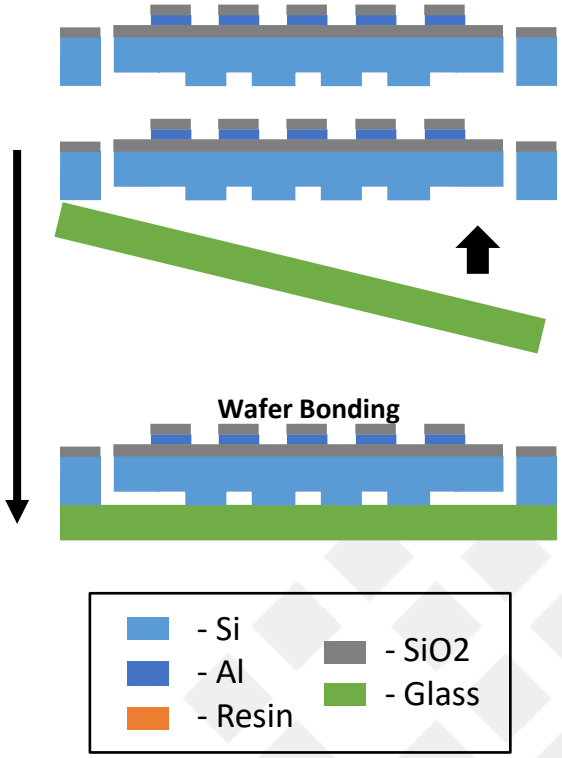
2. Creation of microchannels



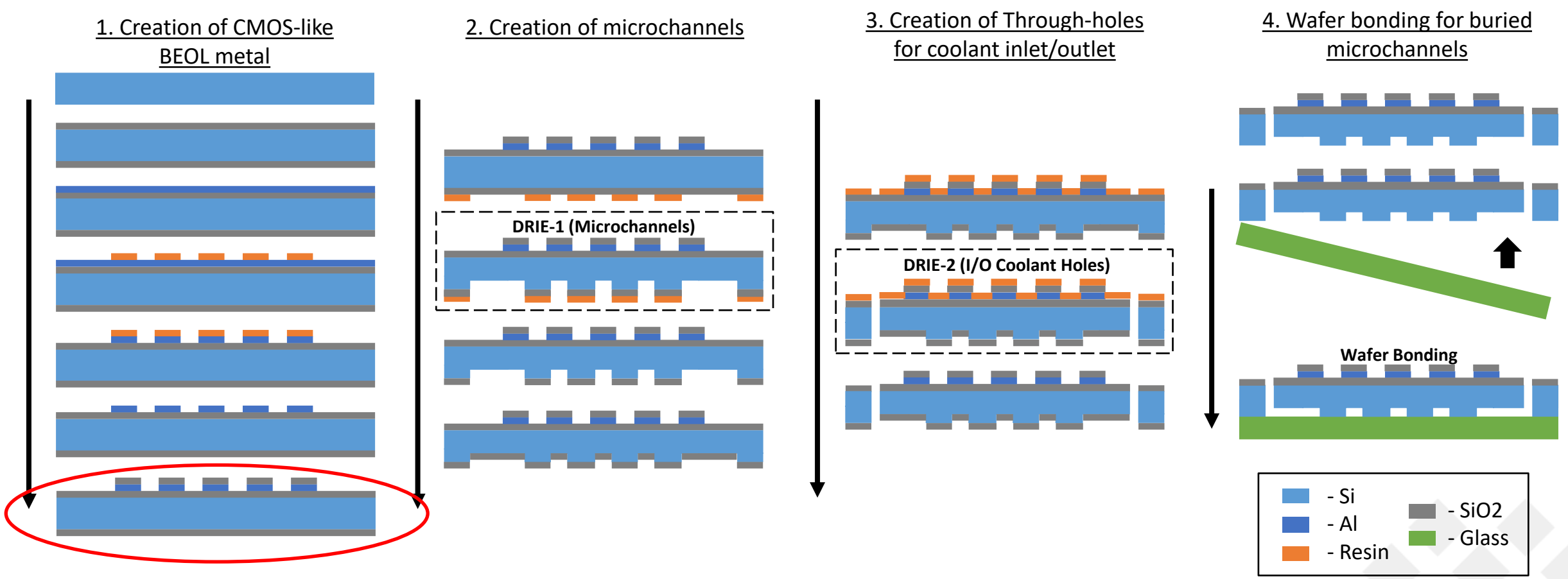
3. Creation of through-holes for coolant inlet/outlet



4. Wafer bonding for buried microchannels



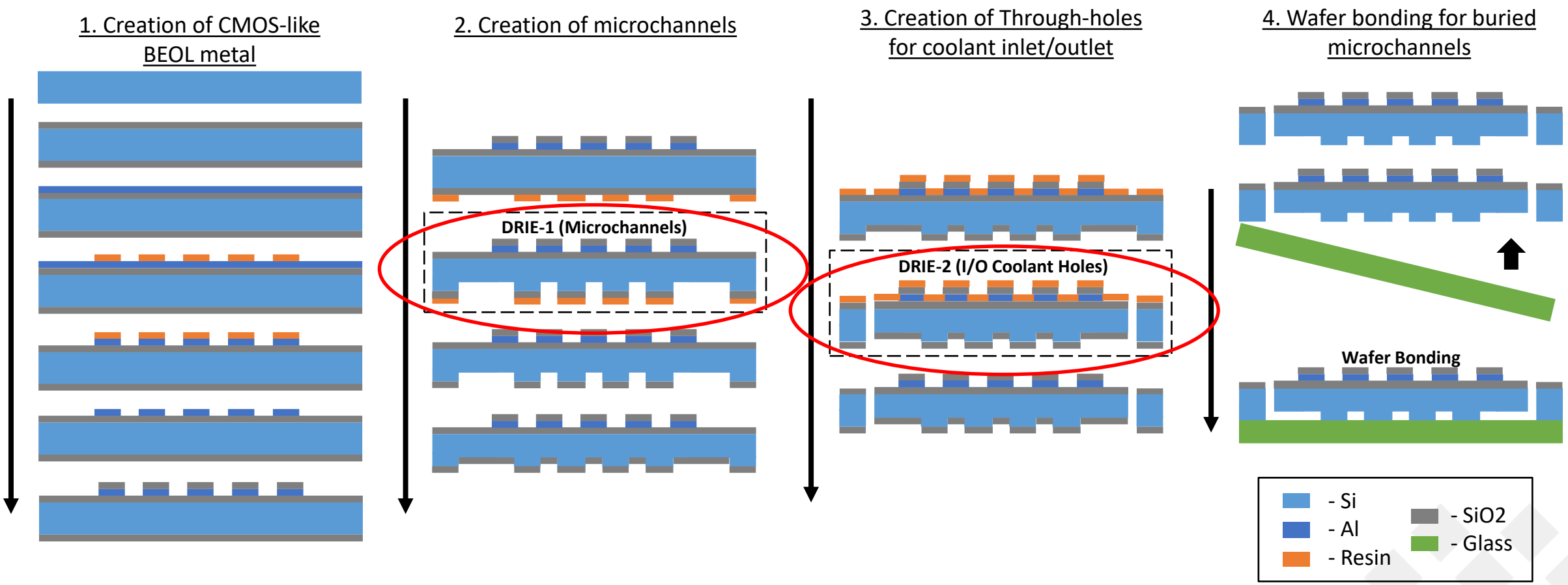
Challenges – Protection CMOS Metal



Protection Back-End Of Line (BEOL) metal:

- External (or in-house) CMOS sensors received passivated, but with openings (e.g.) for contact pads
- Full passivation cover needed to protect metal during the creation of the microchannels and wafer bonding
- Passivation opening at the end of the fabrication process

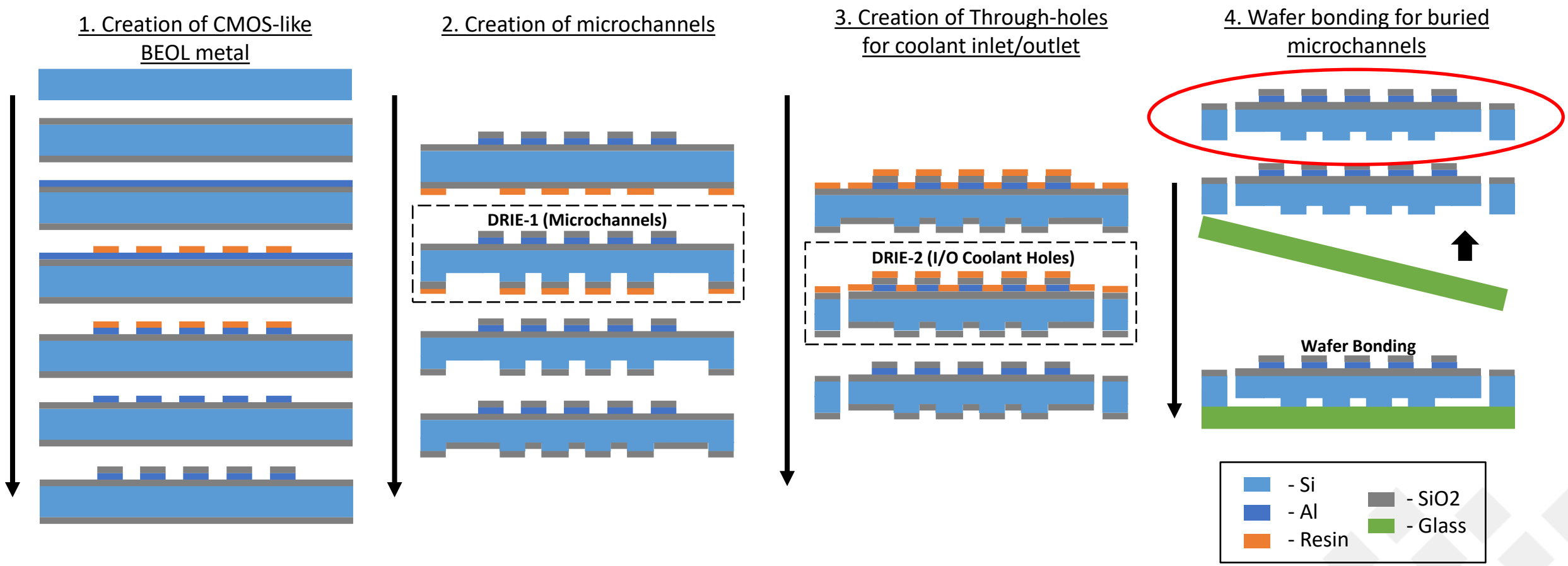
Challenges – DRIE



Protection for the creation of microchannels and I/O coolant holes:

- Requires proper protection layer for the silicon (CMOS devices) during DRIE
- Silicon oxide and resist used as mask layer

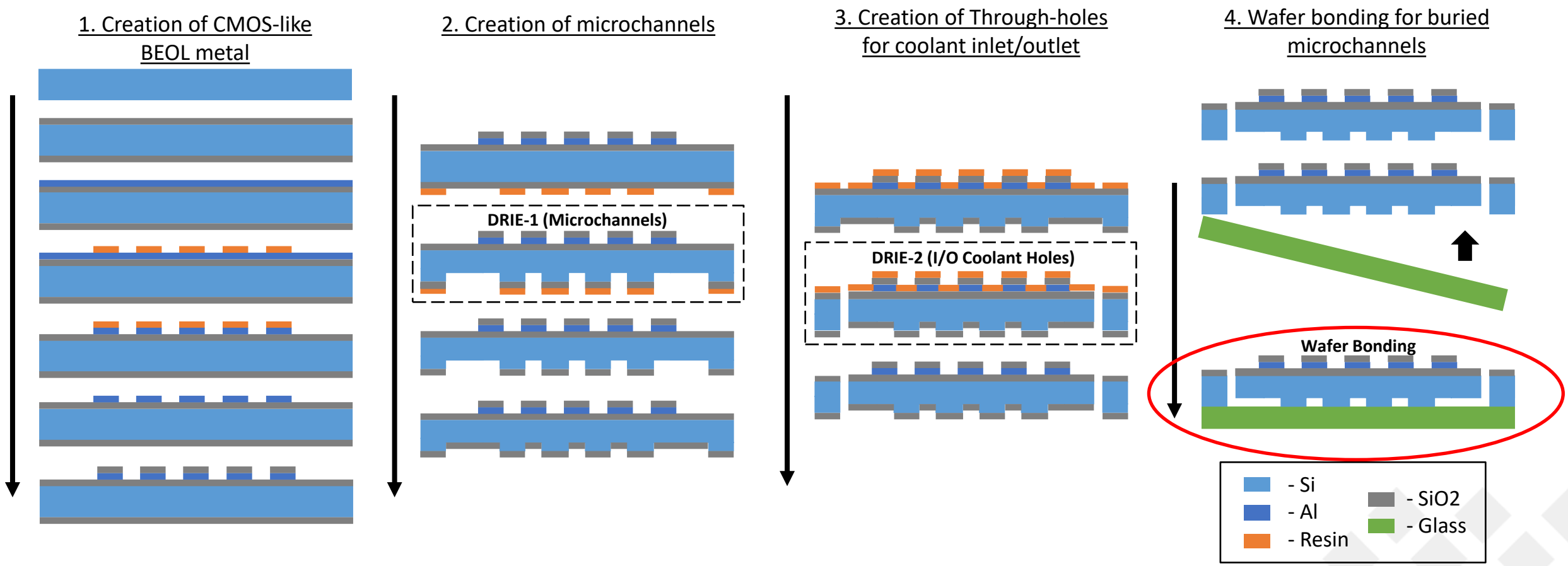
Challenges – Surface Bonding



Preparation of Silicon surface for wafer bonding:

- High quality wafer bonding requires optimal wafer surface conditions
- Oxide etching and cleaning before bonding is critical to achieve good results
- At the same time, cleaning should not degrade the metal (CMOS)

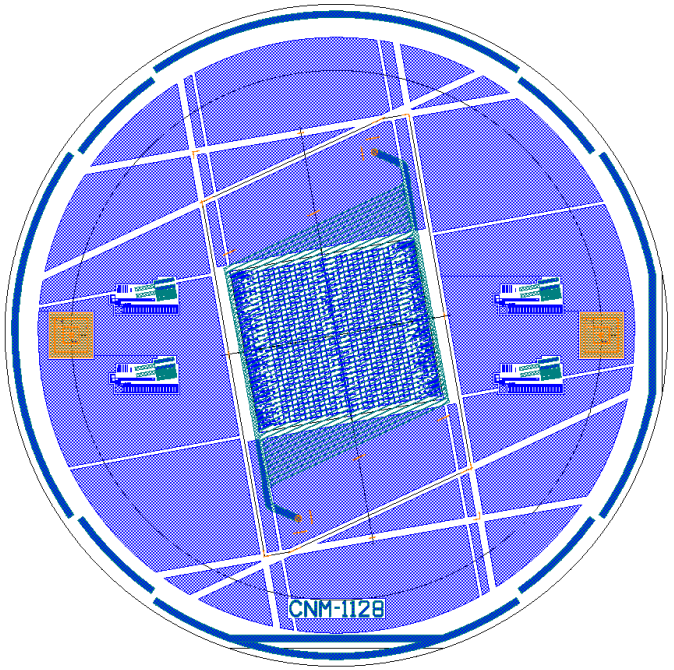
Challenges – Temperature Bonding



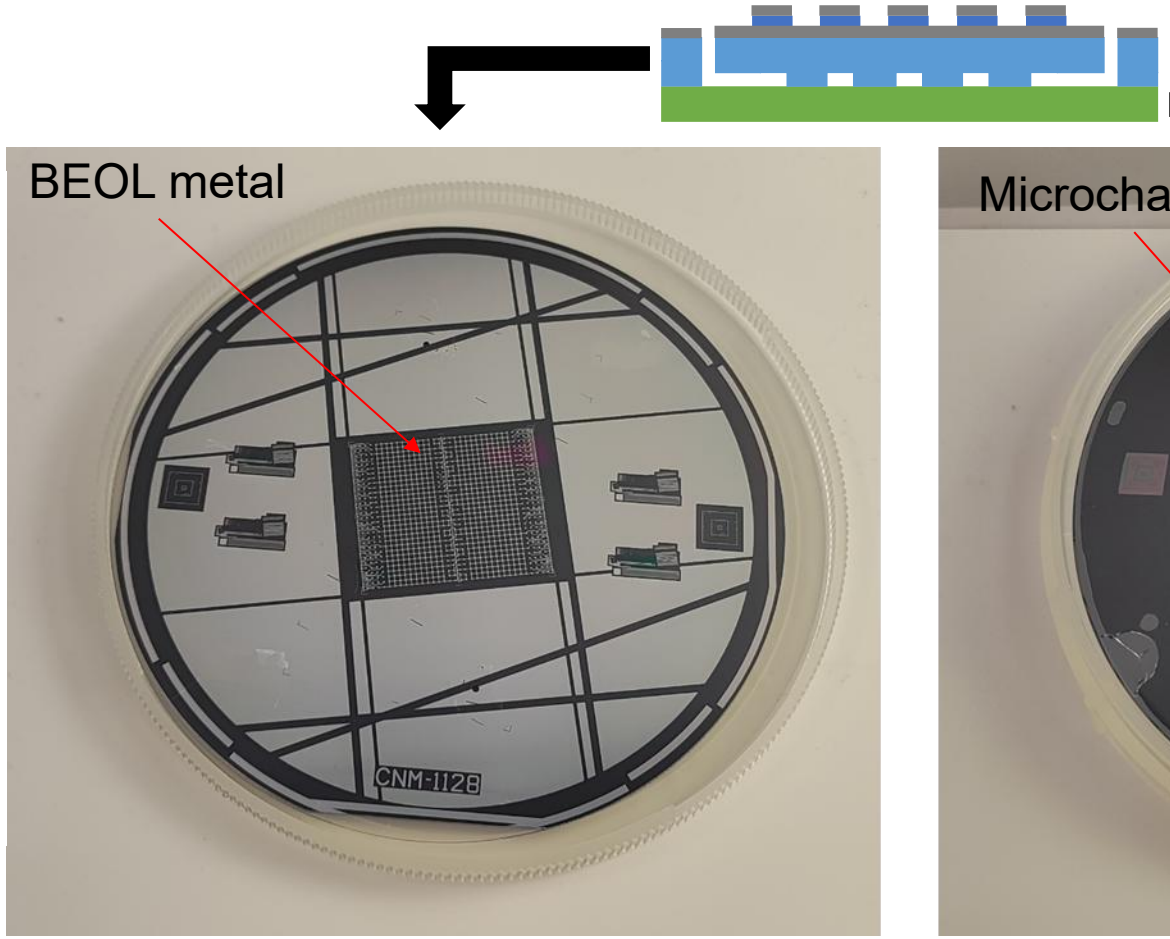
Optimization temperature anodic wafer bonding:

- BEOL (CMOS-like) metal can be deteriorated for temperatures above 380-400ºC
- Anodic wafer bonding technique at IMB-CNM optimized to only 350ºC

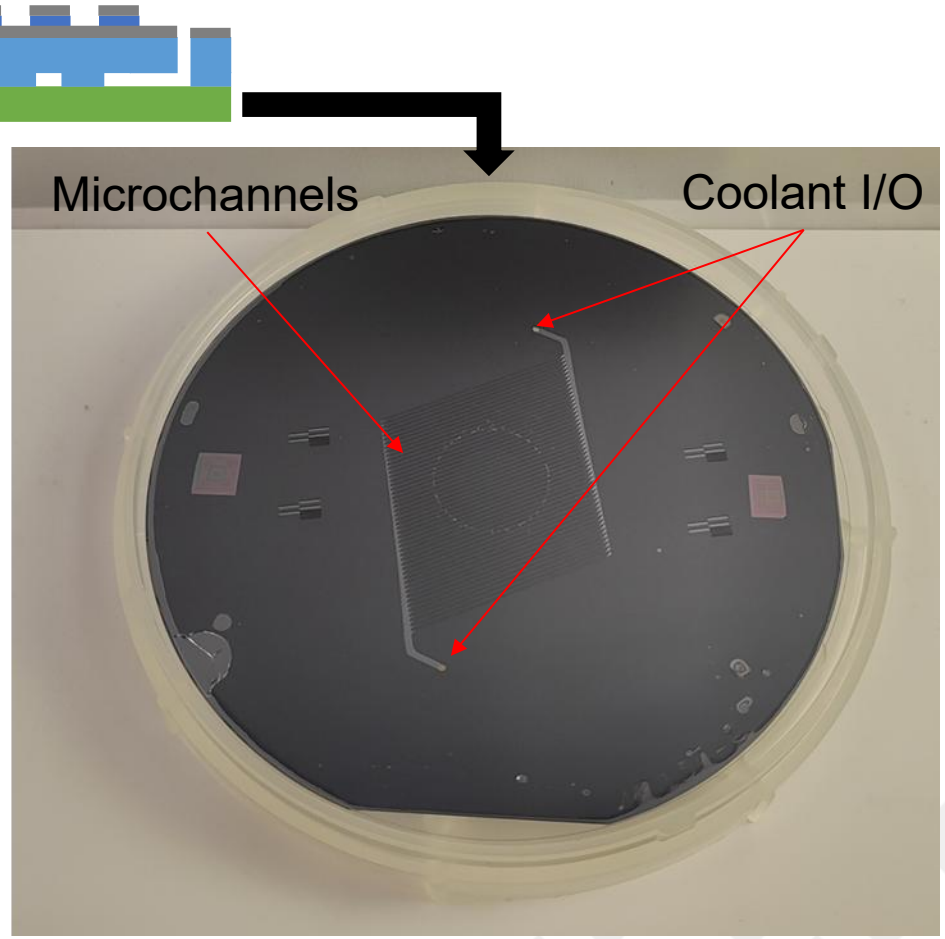
Results – Pictures Final Assembly



LAYOUT



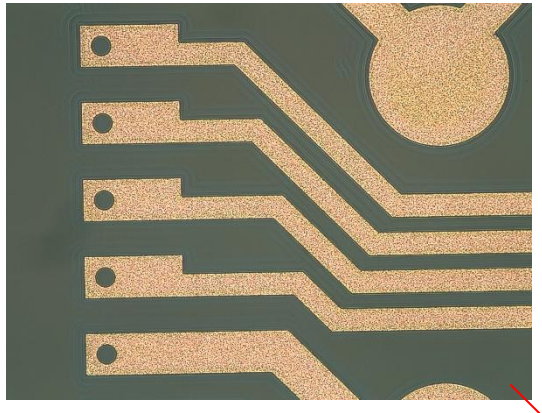
FRONT SIDE (CMOS-like)
Silicon wafer with BEOL metal (top), coolant I/O (top) and microchannels (bottom)

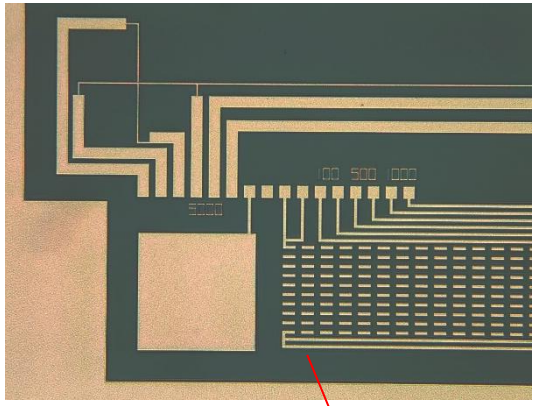


BACK SIDE
Blanket glass wafer

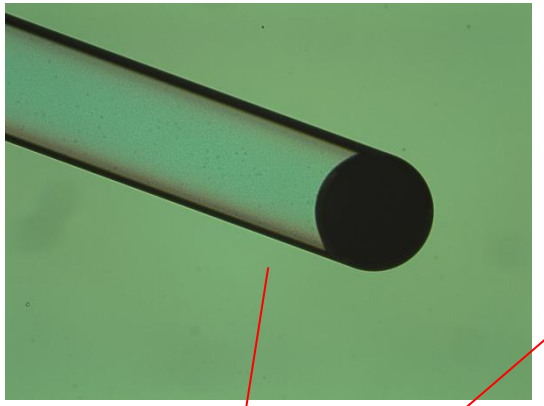
Results – Pictures BEOL and Microchannels

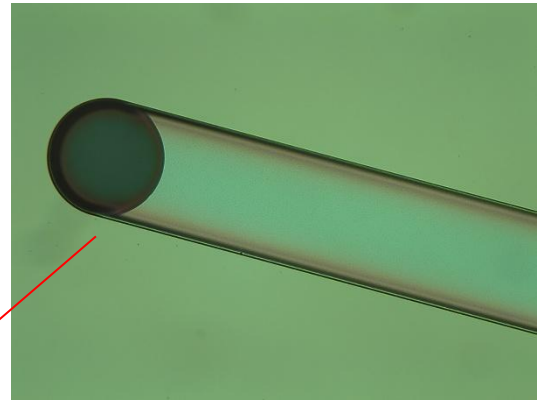
BEOL metal

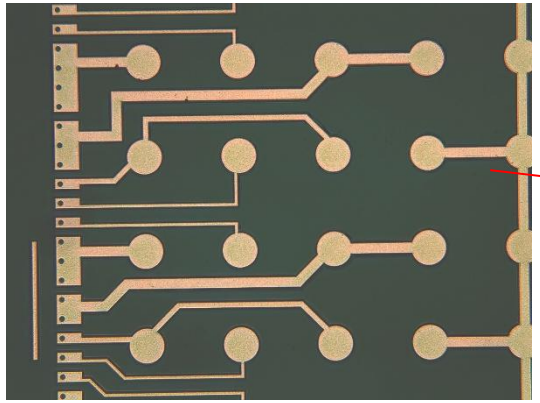


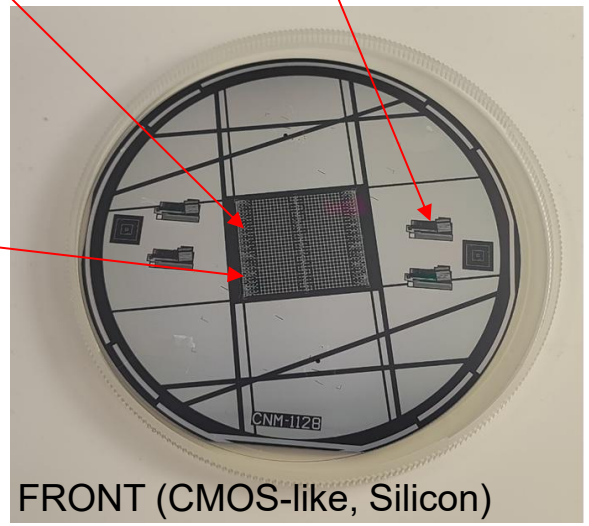


Coolant I/O

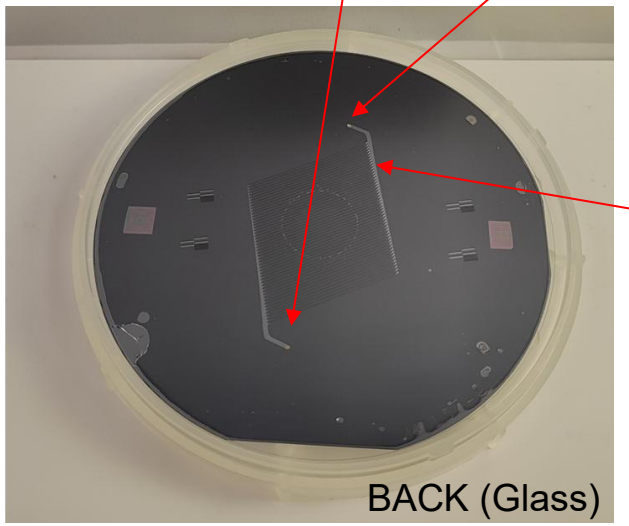






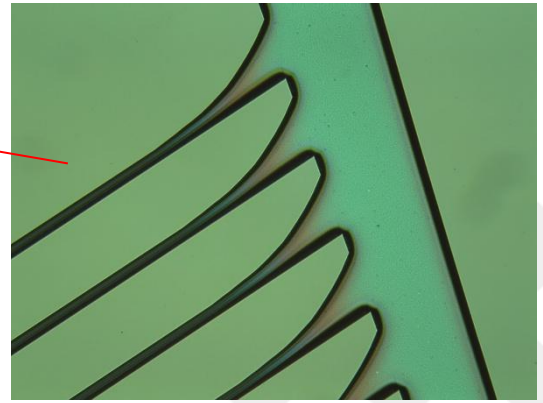


FRONT (CMOS-like, Silicon)



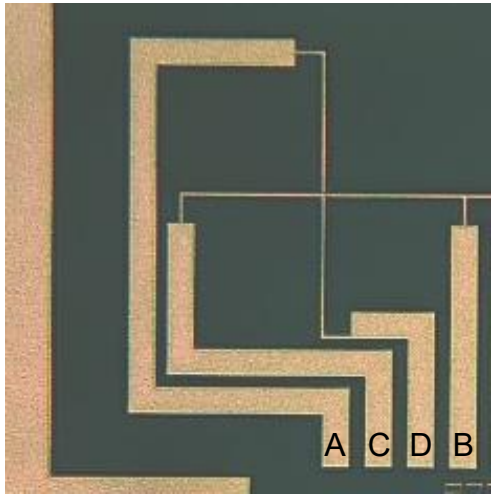
BACK (Glass)

Microchannels



Results – BEOL Metal Evaluation

Sheet Resistance BEOL Metal

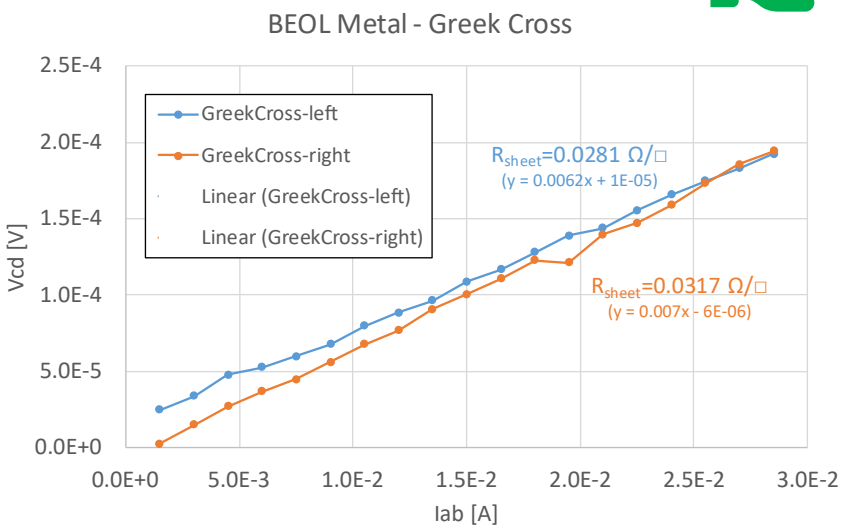


- Measurement of sheet resistance using Greek Cross test structure:
  - Expected 27 mΩ/□
  - Measured 29.9±0.9 mΩ/□

✓ **Good quality of BEOL metal at the end of the process of microchannel integration and wafer bonding**

$$R = \frac{V_{DC}}{I_{AD}}$$

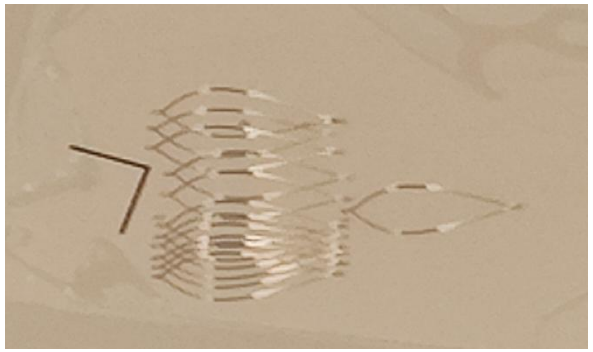
$$R_s = \frac{\pi R}{\ln 2} \quad \Omega/\square$$

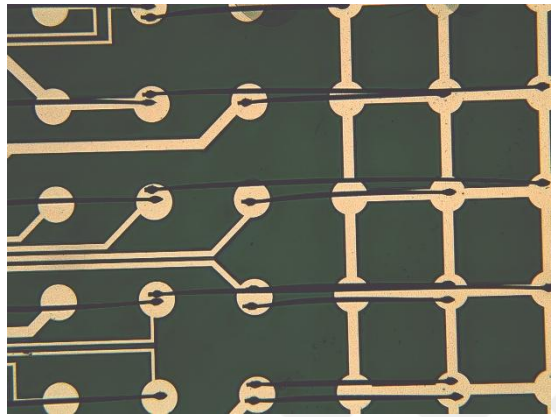


Wire-Bonding

- Wire-bonding performed to evaluate possible degradation of BEOL metal
- Several wire-bonds in different areas of the wafer

✓ **No issues observed, good metal quality for wire-bonding**





Additional Tests

- ❑ Pull tests wire-bonding (on-going at IMB-CNM)
- ❑ Thermal and fluidic tests (on-going at DESY)
- ❑ Cross-sections of the final assembly

Summary

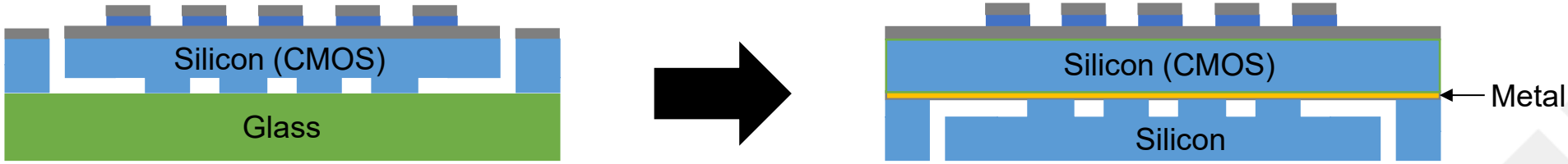
- **Technology** for embedded microchannel fabrication and integration **well established at IMB-CNM**
  - In previous works, **demonstrated** successful integration of micro-channels in silicon interposers with signal/power re-distribution layers for **heterogeneous integration**
- Successful integration of micro-channels in silicon wafers with CMOS-like Back-End Of Line (BEOL) metal for **monolithic integration**
- **Some technological challenges faced** (and overcome) during fabrication process:
  - Protection of BEOL (CMOS) metal
  - Protection of Silicon surface for DRIE (creation microchannels and holes)
  - Preparation of Silicon surface for wafer bonding
  - Optimization temperature anodic wafer bonding
- **CMOS Compatibility: Evaluation of BEOL metal** at the end of the fabrication process **show good results**
  - No deterioration observed
  - Proper metal sheet resistance values after integration of microchannels
  - Excellent metal bondability

Future Work

- Working on **alternative technologies** for monolithic integration and final demonstrators

❑ **Integration of microchannels in "back side" Silicon wafer**, instead of "front side" CMOS wafer

- Use of eutectic (Si/Metal/Si) wafer bonding technique, available at IMB-CNM
- Less critical/invasive for CMOS sensor, as DRIE is done in the other wafer and CMOS substrate remains intact
- Coolant I/O can be done through back side wafer
- Temperature optimization might be needed for eutectic wafer bonding (~400ºC) to avoid deterioration of BEOL metal



❑ **Integration of microchannels in** IMB-CNM **CMOS sensors** (mid-term), and external CMOS sensors (long-term)

- Use of real CMOS wafers to produce final demonstrators with microchannels integrated
- Possibility to integrate microchannels to CMOS sensors diced (Die2Wafer bonding instead of Wafer2Wafer)

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Thanks for your attention

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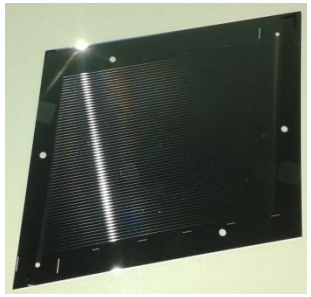
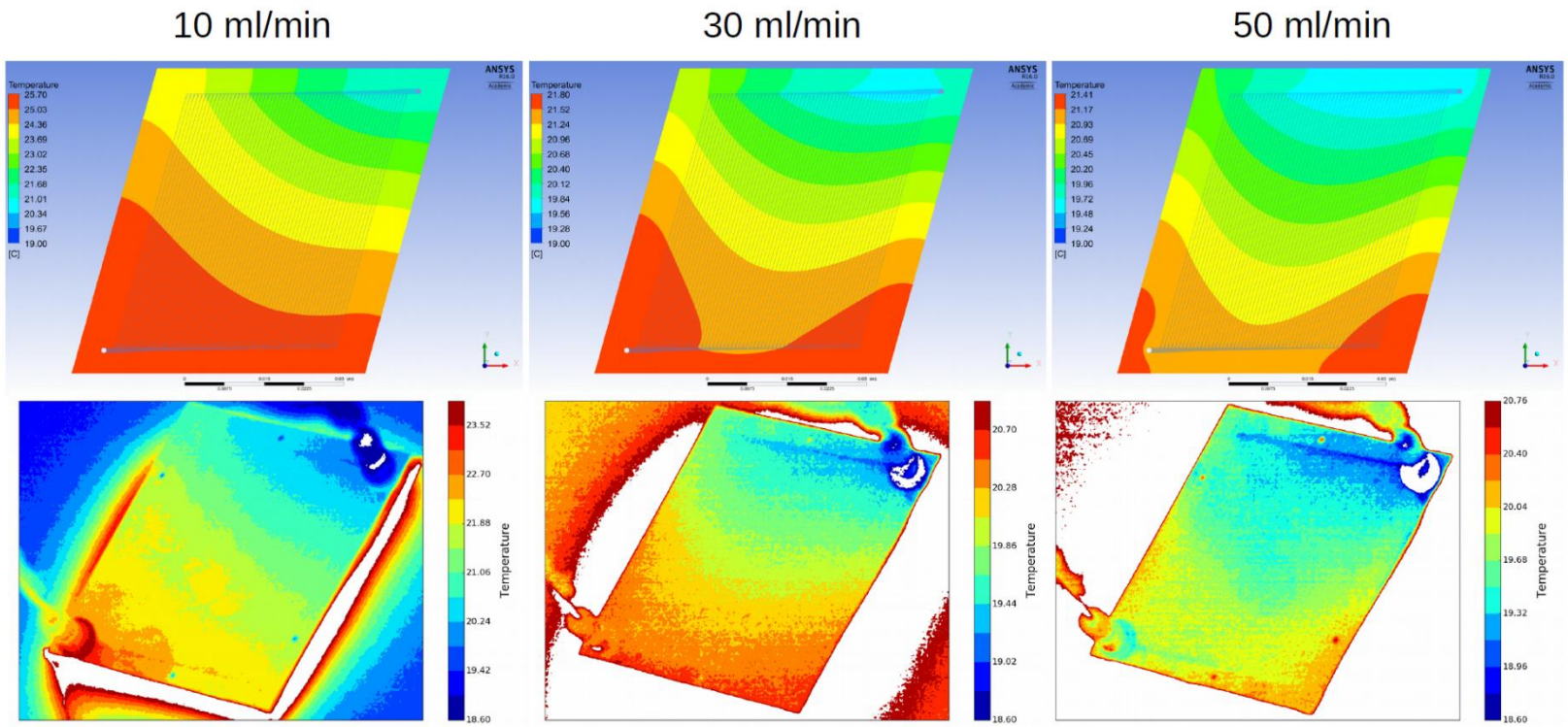
BACKUP

Fluidic and Thermal Tests

- Laminar flow
- Good agreement with simulation
- Thermal homogeneity across the sample,
  < ±1 ºC (for lowest flow rate)





N. Flaschel, et al. NIMA, vol. 863, pp. 26-34, 2017. http://dx.doi.org/10.1016/j.nima.2017.05.003