Supporting document

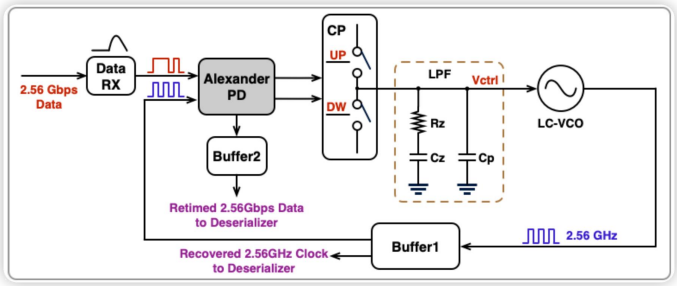

Figure 1 Block diagram of CDR ASIC

The CDR ASIC block structure is shown in figure 1. The CDR ASIC consists of an input equalizer stage, a bang-bang phase detector (BBPD), a charge pump circuit (CP), a low-pass filter (LPF) and a LC voltage-controlled oscillator (LC-VCO) circuit.

Figure 2 Test setup and results

In the test setup, a BERT (SinoLink SL3004A) that can provide 2.56 Gbps high-speed PRBS data to the CDR ASIC. The 2.56 GHz clock recovered by the CDR ASIC and the retimed 2.56 Gbps data are transmitted to a high-speed oscilloscope (DPO75902SX) through chip PADs, bonding wires, PCB transmission lines, and cables to observe the data and clock eye diagrams and the BER. Meanwhile, the clock is also sent to a spectrum analyzer (NA9020A) for phase noise testing, as shown in figure 2.

The CDR ASIC has been fabricated in a 55 nm CMOS process. The phase noise test results show that the CDR ASIC outputs the 2.56 GHz clock with a phase noise of -110 dBc/Hz at 1 MHz offset and a rms jitter of 857 fs. The logic test results show that the recovered 2.56 Gbps data is correct and the BER less than 10−12 is achieved in all tests.