A Low-Noise Analog Front-End Readout ASIC for High-Rate Applications in Pixel Detectors

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Abstract

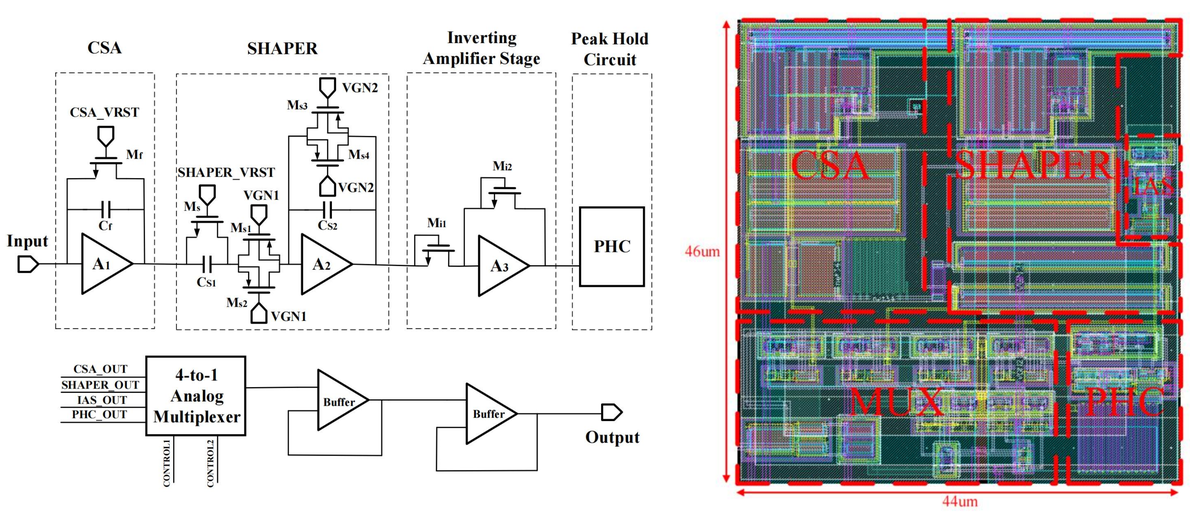
This paper presents the design and implementation of an analog front-end readout chip tailored for silicon pixel detectors, aiming to meet the requirements of energy extraction and signal shaping under high event rate particle detection scenarios. Fabricated using the GSMC 130nm CMOS process, the chip integrates key functional modules including a charge-sensitive amplifier, a CR-RC shaper, an inverting amplifier, a peak holder, and an analog multiplexer. The charge-sensitive amplifier converts transient charge signals generated by incident particles into voltage signals proportional to the deposited energy, providing the initial signal amplification and conversion. The CR-RC shaper performs signal filtering and shaping, producing a pulse width of approximately 10μ s, which allows the chip to handle an instantaneous maximum event rate of about 100 kHz. The inverting amplifier adjusts the signal polarity and amplitude, while the peak holder captures and retains the pulse maximum. A 4:1 multiplexer enables selection of CSA, shaper, inverter, or peak output for monitoring. The measurement results show that the chip exhibits good linearity and stable shaping performance in the dynamic range of 0-20ke$^-$. Under typical operating conditions, the chip consumes 20.8mW of power and achieves an equivalent noise charge of approximately 25.2e−. The core circuit occupies an area of approximately 44μ m × 46μ m. These features endow the chip with superior energy resolution and dynamic range, making it suitable for front-end analog readout in high-resolution silicon pixel arrays, and applicable to integrated nuclear detection systems and X-ray polarization measurement missions.

Introduction

- X-ray polarization measurements are a powerful diagnostic in high-energy astrophysics, offering direct insight into the magnetic-field structures, radiation mechanisms, and geometrical configurations of compact celestial sources such as black holes, neutron stars, and gamma-ray bursts.
- In practical space environments, detectors often operate under complex radiation backgrounds, where multiple high-energy particles may strike the pixel array simultaneously or in quick succession. This can lead to charge overlap, signal distortion, and degradation of energy resolution. Consequently, the front-end readout electronics must achieve fast response, short shaping time, and reliable event discrimination to ensure stable performance under high event rates. Conventional analog architectures are often limited in speed, dynamic performance, and pile-up rejection capability, making them insufficient for such demanding applications.
- To address these challenges, we present a high-speed analog front-end readout circuit for single pixel detectors intended for space X-ray polarization instruments.

Front-End Chip Design and Implementation

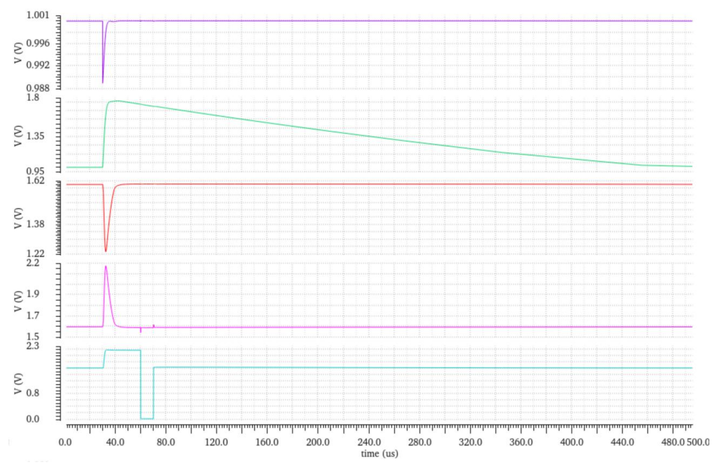
This section presents the design and implementation of the front-end readout chip for silicon pixel detectors, highlighting the architecture, key design considerations, and circuit-level implementation. The design aims to achieve a wide dynamic range, low noise, low power consumption, and compact integration, suitable for high-resolution particle detection applications. To meet these requirements, the front-end readout circuit comprises five primary functional modules: a charge-sensitive amplifier (CSA), a CR-RC shaper (SHAPER), an inverting amplifier stage (IAS), a peak-hold circuit (PHC), and an 4-to-1 analog multiplexer (MUX). All capacitors are realized using parasitic capacitances between metal interconnects, offering good matching and efficient area utilization. Pseudo-resistors implemented with MOS transistors operating in the subthreshold region provide high resistance values while maintaining low power consumption, small area, and strong process compatibility.



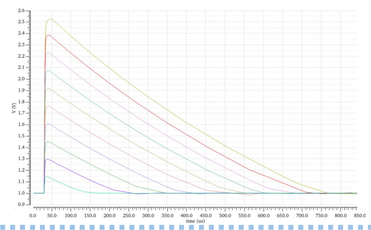
Simulation and Test Results

Simulation results of energy deposition

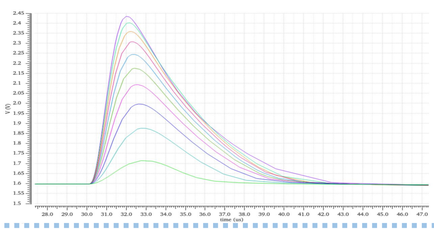
To evaluate the analog front-end readout chip, comprehensive simulations were performed over a 1–10 ke$^-$ input charge range, representing realistic particle-induced charge deposition. Output waveforms of the CSA, SHAPER, IAS, PHC, and the full readout chain were analyzed to characterize each stage's dynamic response.



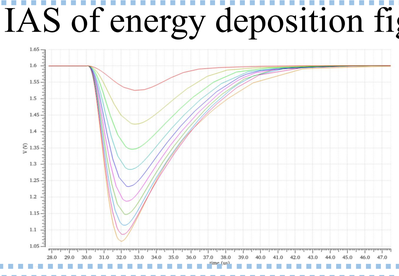
- CSA of energy deposition figure



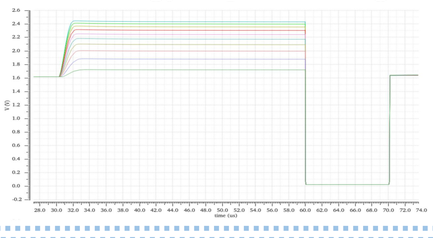
- SHAPER of energy deposition figure



- IAS of energy deposition figure



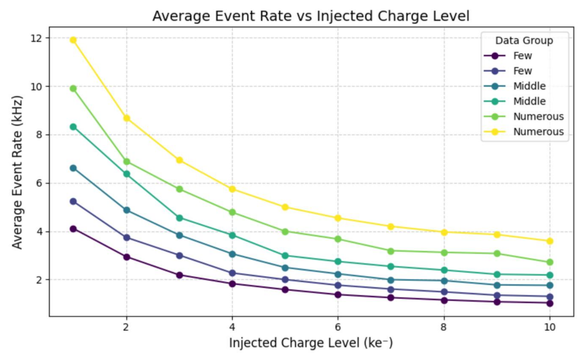
- PHC of energy deposition figure



Event rate test results

- To evaluate the chip's performance under high event rates, high-rate tests were conducted to assess signal integrity and event-handling, focusing on preventing saturation, distortion, and event loss, and determining the maximum instantaneous and average rates the chip can sustain.
- The theoretical upper limit of the instantaneous event rate is approximately 100 kHz.
- The average event rate must satisfy:

$$Y \lesssim \frac{1}{\tau} \qquad \tau(E, V_G) = C_f R_f(V_{SD}(E), V_G)$$



Conclusion

This work presents a low-noise, highly integrated analog front-end readout chip architecture, implemented in a 130 nm CMOS process. The proposed design employs a multi-stage signal chain with configurable signal paths, enabling high-precision conversion and shaping of weak charge signals. Both simulation and measurement results demonstrate excellent performance in energy response, shaping stability, and noise suppression, satisfying the front-end readout requirements of silicon pixel detectors operating under high event rate conditions.

Future research will further extend this architecture toward modular integration within pixel arrays, including the development of a unified bias and readout scheme at the array level. Moreover, systematic characterization of the timing response will be conducted to evaluate its potential for fast signal shaping and time-resolved detection applications.

Reference

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