

Investigations of the core column issue in ATLAS ITk pixel modules

Craig Buttar

On behalf of the ATLAS ITk Collaboration

HSTD14

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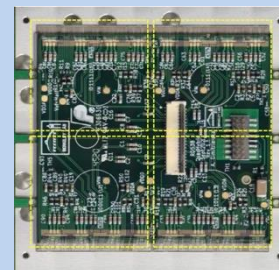
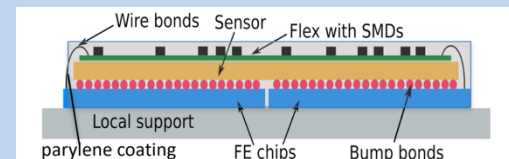
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Academia Sinica, Taipei

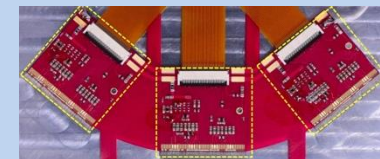
*the 14th International “Hiroshima” Symposium on the Development
and Application of Semiconductor Tracking Detectors+*



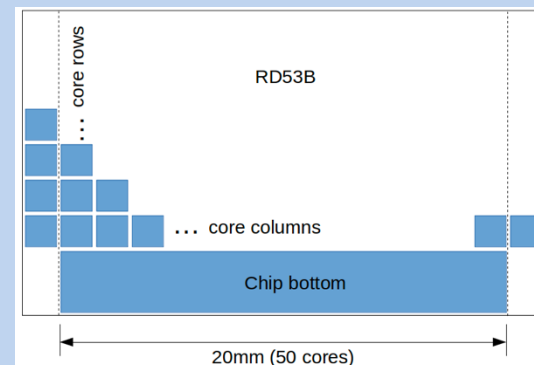
- FE-chip is ITkPixV2 developed by RD53 collaboration in 65nm CMOS technology
 - Production of 700 wafers is complete and 600/700 wafers have been probed ready for hybridization
 - Serial powering implemented using sLDO
 - CMS CROC chip also developed by RD53
- FE-chip and sensor connected using solder based bump-bonding to produce bare module
 - 3 hybridization vendors A,B,C
 - CMS also used vendors A & C
- Flexible pcb glued to the back of the sensor and wire-bonded to the FE-chip
 - Quad modules: 4 FE-chips bonded to 1 sensor
 - Triplet module: 1 FE-chip bonded to 1 sensor
 - Flexible PCB provides connections for power, DCS and data



Quad module



Triplet module

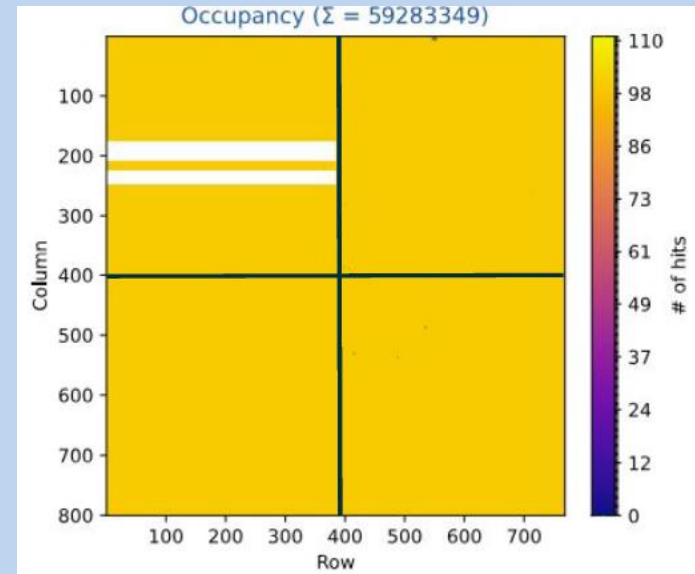


Chip is divided into cores of 8x8 pixels. A core column is 8 pixels wide and 384 pixels high (48 cores)

Data is readout via core columns

A core column corresponds to 2% of the active pixels

- triggered data readout from some cells inside the core column causes a deadlock of the readout processor, causing the whole chip to stop sending data (until reset)
 - Usually observed in basic digital and analog scans. In general, it can be easily seen.
- Chip operation can be recovered by disabling defective core columns
- Currently
 - 400/4927=8.1% of chips with ≥ 1 core column
 - 292/1233=24% of modules with ≥ 1 core column
 - This is most significant impact on the module yield
 - Rates of defective core columns are dominated by vendors B & C
- Issue is not seen during wafer probing
 - Would be seen at wafer level in digital and analog scans
 - > Look at electrical tests of assembled modules
- CMS experience
 - 1.0% chips with ≥ 1 core column
 - 2.8% modules with ≥ 1 core column
 - Also use vendors A & C
 - Rate for vendor A is low, same as for ATLAS, vendor C has lower rate than for ATLAS



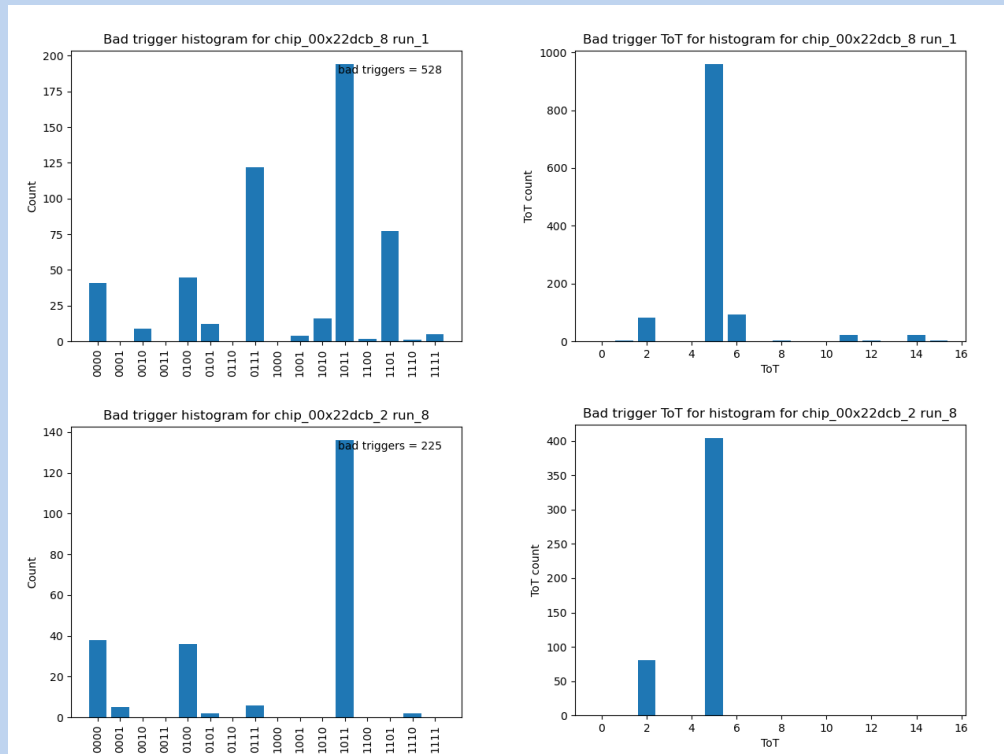
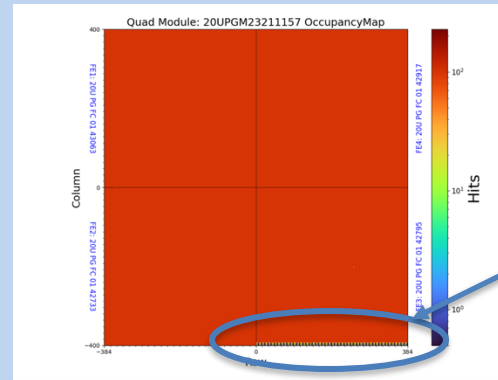
The occupancy scan can only be performed after core columns are disabled

	Number of chips with core columns	Total number of chips	Number of modules with core columns	Total number of modules
CMS CRO				
Duals	1	106	1	53
Quads	7	700	5	175

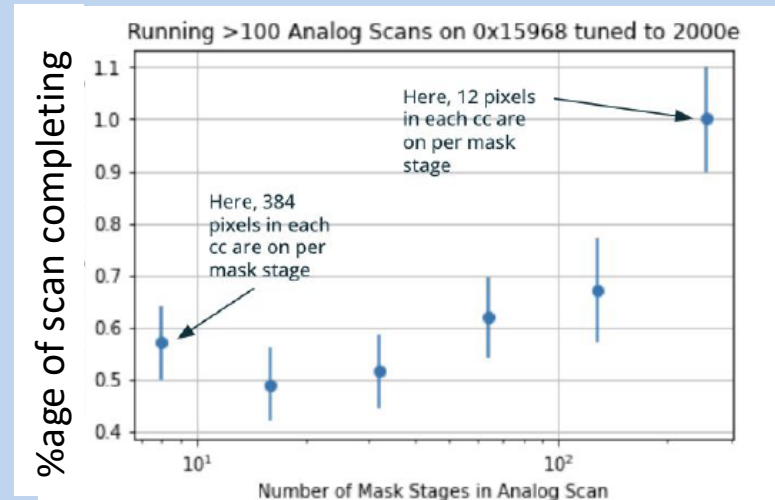
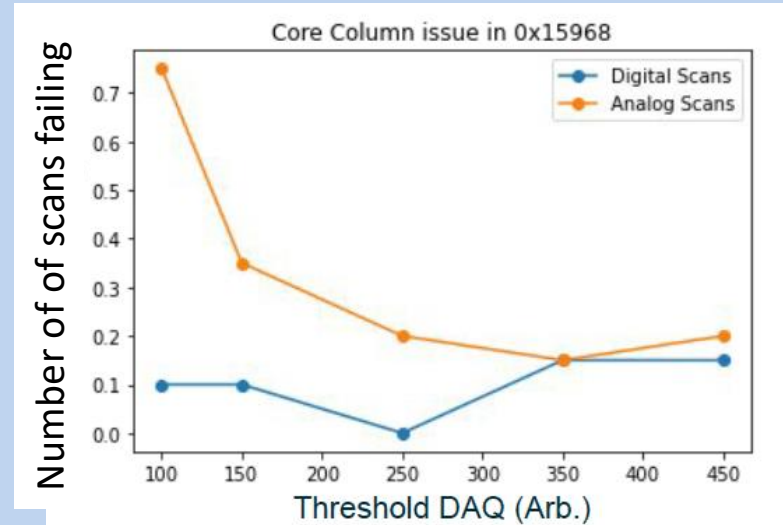
ELECTRICAL TESTING OF ASSEMBLED MODULES

An example of core column issue

- Normally core column locks the chip but look at special cases to try and understand underlying behaviour
- This chip exhibits defective core column behaviour but does not lock the chip
- Core column disabled
 - Chip 3 CC 1 (columns 1-8)
- Digital scan
 - Injecting directing to digital part of chip
 - ToT=5
 - Trigger bin=1000
- Look at number of out of time hits ie not in the specified trigger bin (1000) and their ToT
- Results were not repeatable over 8 runs
- Similar behaviour seen in other modules with bad core columns
- Cross-check with good chip, no bad triggers and ToT=5 for all pixels



- Core columns with issues can show up in later scans eg threshold scan
- Digital scan shows no core column issue but at low threshold, increasing number of core columns in analog scans
- Increasing number of core columns for increasing number of pixels/mask step
 - Typical value is 384 pixels/mask step



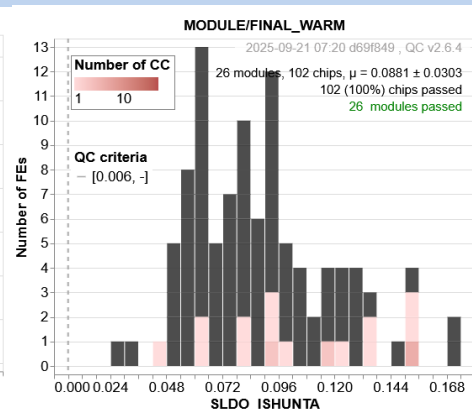
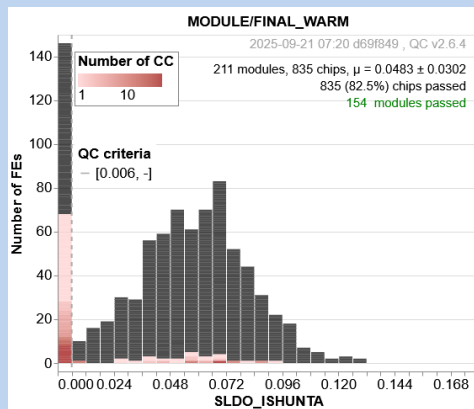
Pixel scan = #mask steps X #pixels/mask step

Correlation of core column issues and sLDO failure

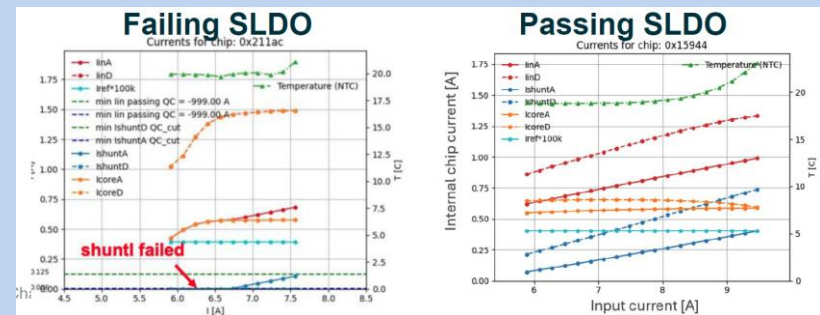
- Core column issues in vendor B modules are often accompanied by sLDO failure (typically shunt current is zero). This correlation is only observed for vendor C

Vendor B modules

Vendor C modules



Analog shunt current



- Wafer probing does not identify any core columns, but should be sensitive to them
 - Electrical testing shows a range of symptoms that are not repeatable in successive tests
 - Strong correlation between sLDO failures and core column issues for vendor B
- This suggests mechanical damage may be the issue

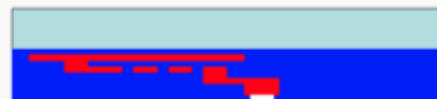
HYBRIDISATION

1



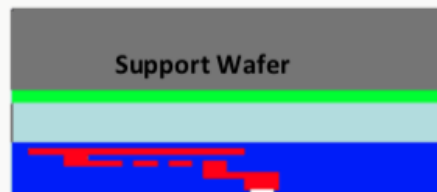
ROC Wafer

2



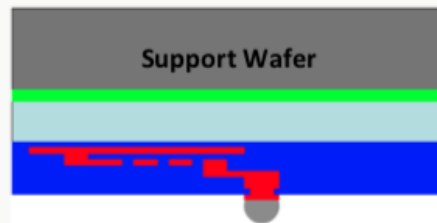
Wafer Thinning

3

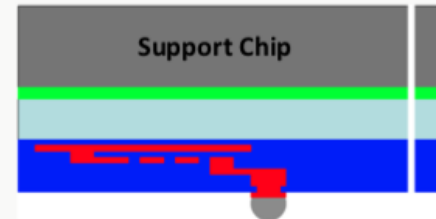


Temporary Wafer Bonding to support wafer

4

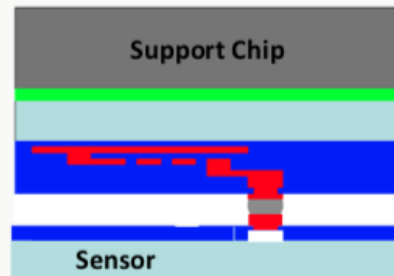


Contact formation (Micro-Bumping)



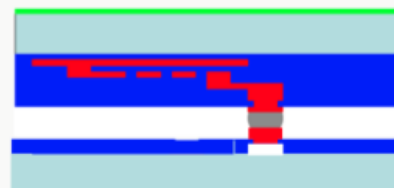
Dicing of Wafer Stack

5



Bump Bonding

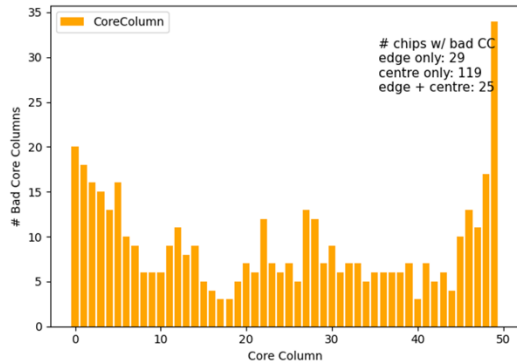
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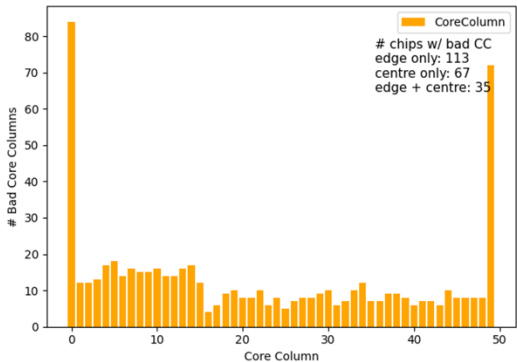
Support Chip Release

7

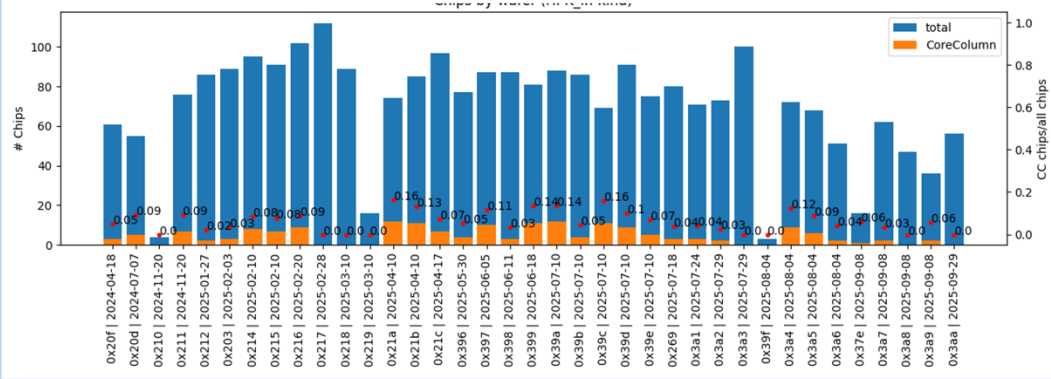
Core column position vendor B



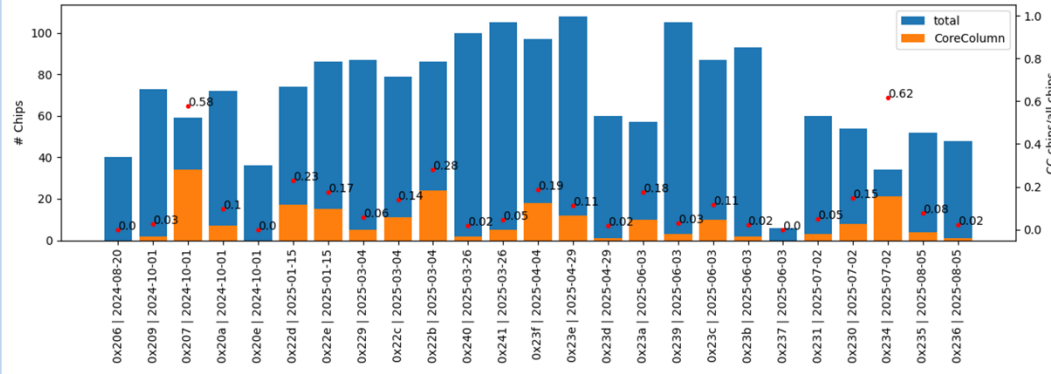
Core column position vendor C



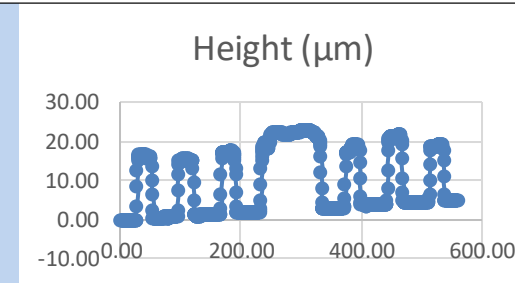
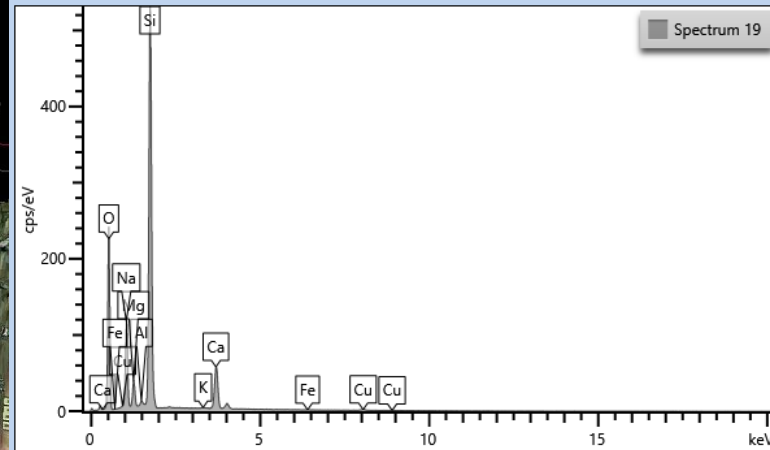
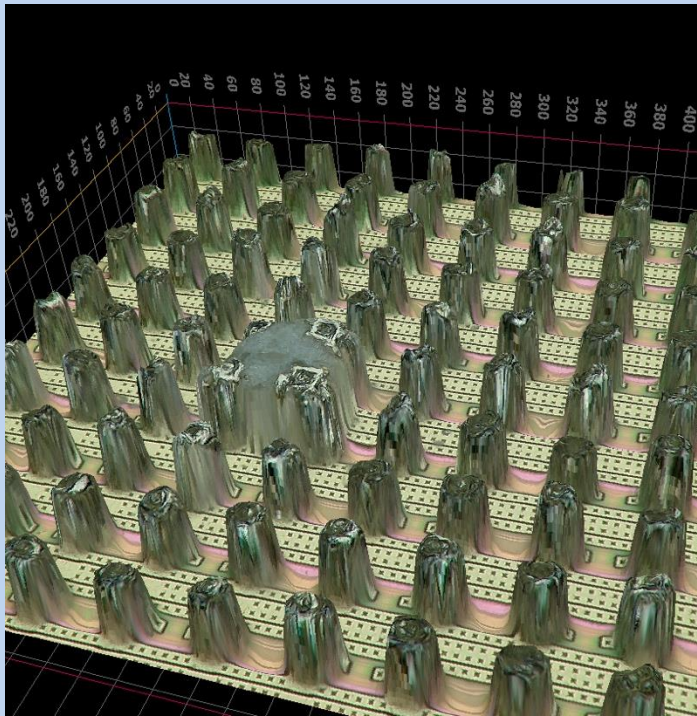
Number of chips defective core columns per wafer vendor B



Number of chips defective core columns per wafer vendor C

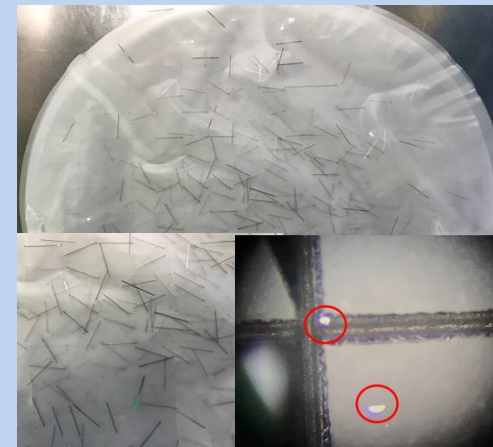
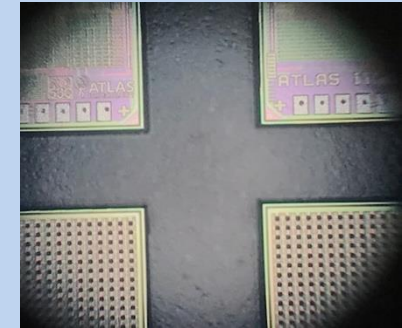
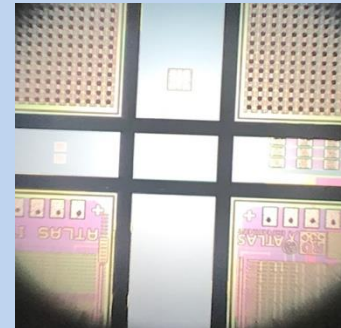


- Vendors show a different distribution of core columns across the pixel matrix
- Substantial variation of number of bad core columns with wafer at both vendors
- Vendor A has a very low number of bad core columns not discussed further

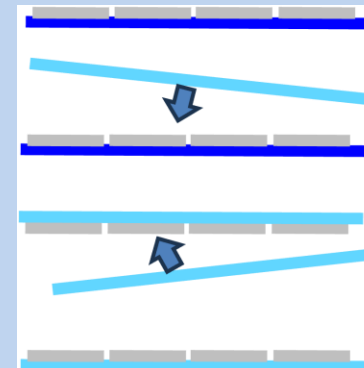


- Pull module apart and look at pixel matrix
- Large lump of silicon (EDX) embedded in the matrix and position of disabled core column
 - height corresponds to flip-chip height
- Other defects observed but not associated with disabled core columns and their height is lower than flip-chip height
- One other module pulled part and showed similar results

- Defective core columns appear to be caused mainly by debris across the surface. Aim to reduce debris on surface
- Current FE-wafer bump deposition vendor
 - Improved handling after dicing by replacing dicing tape
 - Rate of modules with defective core columns reduced from 39% → 20%
- Use the same FE-wafer bump deposition vendor and dicing vendor as vendor A
 - Rate of modules with defective core columns reduced from 39% → 20%
- Improvements have also significantly reduced the number of sLDO failures associated with core column issues
 - 72% → ~27%

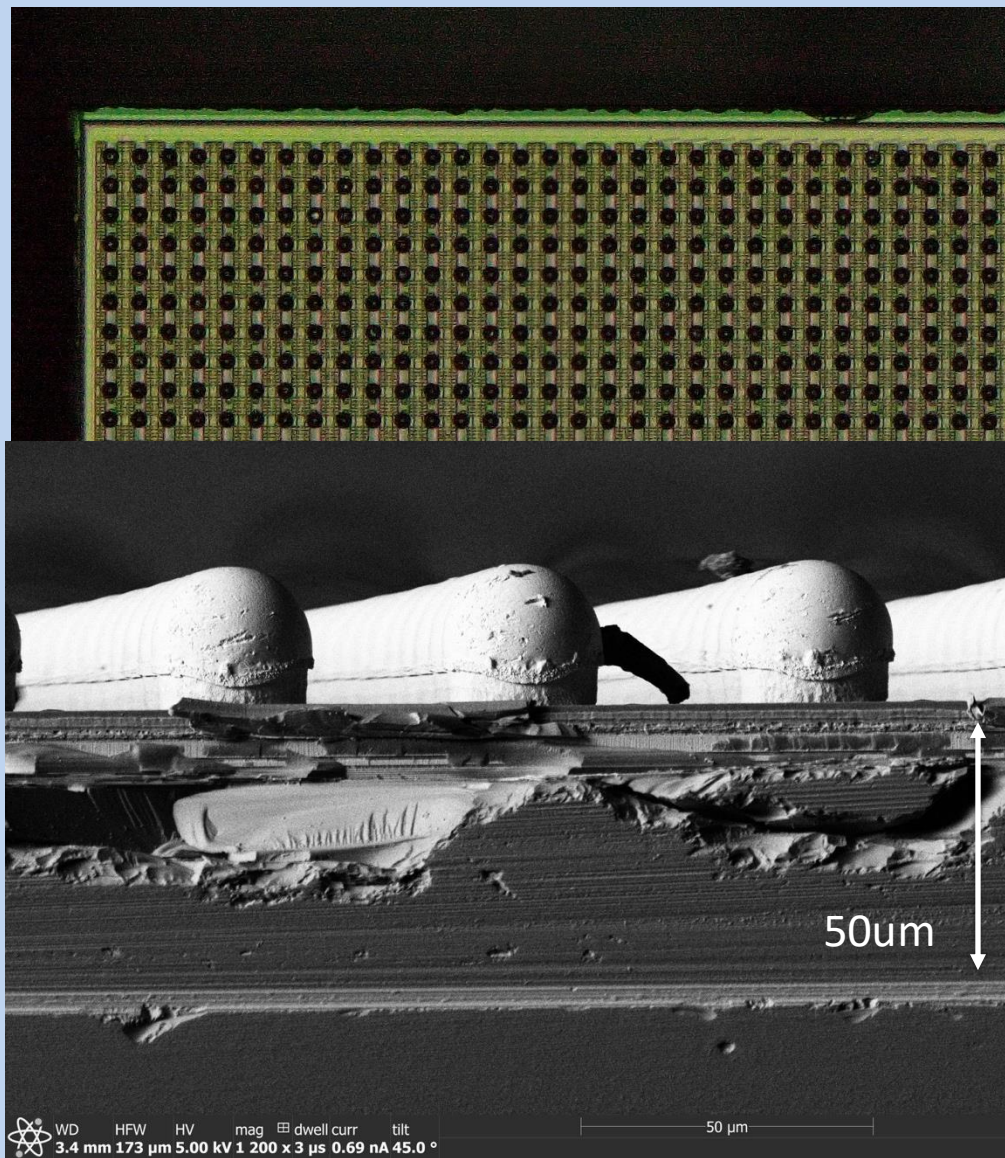


Double dicing removes test structures but leaves Si dust

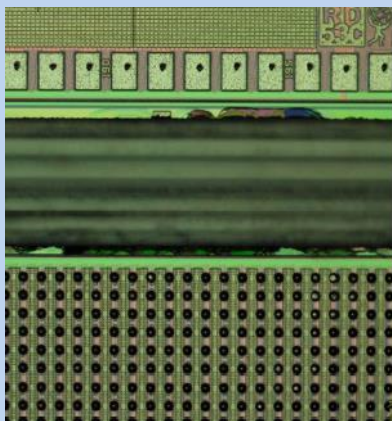


Replace dicing tape to remove shards and dust

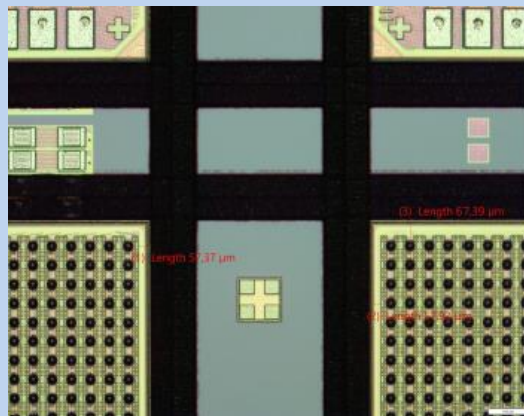
- Defective core columns appear to be caused mainly by edge chipping
- Chipping on edges shows significant damage near the surface of the chip
 - Attributed to low-k dielectrics used in 65nm CMOS process being difficult to saw
- Can result in damage up to the seal ring or into the matrix and debris on the matrix



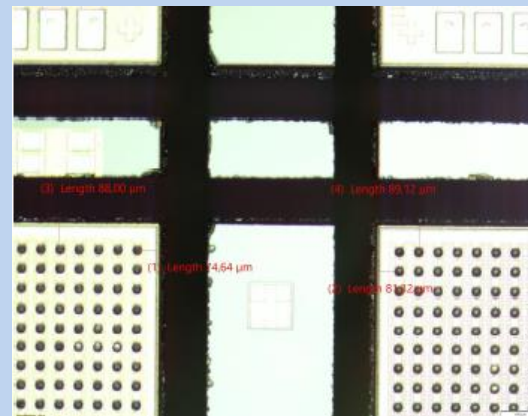
- Use laser pre-grooving to reduce damage at the edges when cutting low-k dielectric
- Initial studies show less chipping at edges
- Modules currently being assembled for electrical tests



Saw dicing



Laser pre-grooving



Laser pre-grooving
+ Saw dicing

Can modules with core column issues be used in the detector?

- Core columns have a significant impact on production
 - Current production yield is dominated by modules with defective core columns. This is evolving with time eg vendor B improvements should improve electrical yield of modules with core columns by reducing associated sLDO failure rate

Number of modules	Fraction with CC	Electrical Yield		
		With CC	Without CC	All modules
648	27%	43%	88%	76% inc CC 64% no CC

- Can CC modules be used in the detector?
 - Tracking performance studies show that a limited number of CC in a module can be tolerated (except for L0 barrel)
 - Modules with sLDO failures cannot be used
 - But** the causes of defective core columns are not yet fully understood. Need to understand if operational conditions (e.g. thermal cycling and radiation) cause changes in the distribution and behaviour of defective core columns that will impact electrical operation and data taking

Summary

- ATLAS has observed FE-chips behaving badly during module electrical QC that requires core columns to be disabled
- Core columns do not need to be disabled during wafer probing indicating there is no fundamental chip issue
- Electrical tests of assembled modules have defective core columns with a range of behaviours
- Data from the production database show different rates and distributions of the core columns for modules from the three hybridization vendors
- Investigations show different types of mechanical damage during hybridization can result in defective core columns
- Vendors are implementing new procedures and reducing the rate of defective core columns
- The use of modules with disabled core columns in the experiment requires an understanding of the stability of the core columns under operational conditions including thermal cycling and radiation, studies are under way.