Measurement of Threshold Voltages in PTP Structures and Estimation of P-stop Densities Across an ATLAS18 Silicon Strip Sensor Wafer Using TCAD Simulations

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Abstract - A total of 24,010 AC-coupled silicon strip sensors, consisting of n-type strips in p-type silicon and referred to as ATLAS18, are currently in production for installation in the upgraded ATLAS Inner Tracker (ITk).

In n-in-p strip sensors, a dense p-type region (e.g., p-stop implant) is essential for electrically isolating the n-type strips from a conductive inversion layer between the strips, caused by positive interface charges.

The punch-through protection (PTP) structure is implemented at one end of each strip to protect the AC-coupling capacitor in the event of large currents flowing into the strips.

During quality assurance (QA) testing, we occasionally observed a deviation in the threshold voltage (V_{PT}) of the PTP structure in the test chips located at a corner of the wafer perimeter, with a shift of four standard deviations or more below the mean.

To evaluate the variation of V_{PT} across a wafer, we selected two main sensors, each processed in a different furnace, where V_{PT} measurements in the QA test chips were still near the mean value. One sensor exhibited a flat distribution of V_{PT} measurements, while the other showed a non-uniform, parabolic distribution, with a shift of four standard deviations toward the wafer edge.

TCAD simulations were used to analyse V_{PT} as a function of p-stop density, confirming that the V_{PT} correlates well with the p-stop density. By setting the nominal p-stop density (4×10^{12} cm^{-2}) to correspond to the mean V_{PT} value, the p-stop density at the wafer edge, which is four standard deviations away from the mean, is estimated to be approximately half (2×10^{12} cm^{-2}). A p-stop density of 2×10^{12} cm^{-2} should still be sufficient to ensure isolation, even after irradiation, and in the presence of interface charges as high as 1×10^{12} cm^{-2}.

Introduction – A total of 24,010 AC-coupled silicon strip sensors are currently in production, consisting of n-type strips in p-type silicon, referred to as ATLAS18, for installation (17,888 sensors) in the outer layer of the upgraded ATLAS Inner Tracker (ITk) [1].

In n-in-p strip sensors, a dense p-type region (e.g., p-stop implant) is essential for electrically isolating the n-type strips from a conductive inversion layer in the surface of silicon between the strips, which is caused by positive interface charges.

A punch-through protection (PTP) structure, a narrow gap between the strip and the bias rail implants, is implemented at one end of each strip to protect the AC-coupling capacitor in the event of large currents flowing into the strip. The PTP structure creates a current flow channel between the strip and the bias rail implants despite the presence of the p-stop implant, in parallel with the bias resistor. A trace of bias resistor is designed to overlap the PTP region, functioning as a gate and ensuring a low PTP threshold voltage and fast turn-on [2].

During quality assurance (QA) testing, we occasionally observed[2] in the QA test chips that the threshold voltage (V_{PT}) of PTP structure deviated by approximately 4 times the standard deviations (sigma) below the mean, where V_{PT}(QA) for those within acceptance limits is ~15 V (mean) and ~0.8 V (sigma). The QA test chips are located at the corner of the perimeter of the 6-inch wafer.

To evaluate the V_{PT} variation across a wafer, we measured the strips in the main sensors. The main sensor is designed with approximately 1,280 strips, each having a typical strip pitch of 75 µm and containing either 2 or 4 segments per strip.

We used TCAD simulations to analyze the dependence of V_{PT} on p-stop density and other factors.

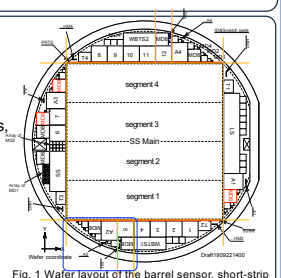

Fig. 1 Wafer layout of the barrel sensor, short-strip type (SS). Strips are arranged vertically, and consist of 4 segments. QA testchips are diced along the orange line, one set per wafer, indicated by a blue circle [1].

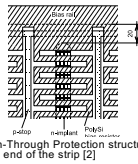

Fig. 2 Punch-Through Protection structure (PTP) at the end of the strip [2]

Variation of V_{PT} across a wafer – We selected two main sensors, each processed with a different furnace, and measured the V_{PT} of the strips to probe the variation across the wafer. In this setup, segments 1 (Seg 1) and 4 represent the PTP structure at the ends of the sensor, while segment 2 represents the middle.

VPA53553-W03492, processed with furnace B, showed flat V_{PT} distributions. VPA50932-W03132, processed with furnace A, showed non-uniform, parabolic V_{PT} distributions across the wafer, with V_{PT} approximately 4 standard deviations below the mean toward the edge in segment 2.

The measured V_{PT} of the QA test chips of these wafers (in the red circle) were still near the mean value, ~15 V.

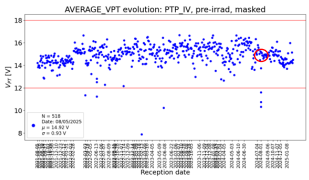

Fig. 3 Trend plot of V_{PT} over the course of production [5]. The acceptance limits are between 12 V and 18 V for the lower and upper bounds, respectively.

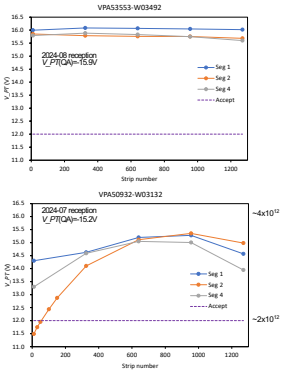

Fig. 4 V_{PT} measurements obtained by sampling strips across the wafer, with furnace B (top) and A (bottom).

TCAD model of the PTP structure – We used the TCAD 3D device simulator, HyDeLEOS VER. 8.5k [3]. The PTP structure is implemented in 2D geometry (Fig. 5) with the major parameters used in the simulations listed in Table 1.

Table 1. Major parameters of PTP structure in TCAD simulations

- Silicon bulk: p-type, 3 kΩcm, 320 µm
- n-strip (*Nsub1*: n^{++} implant)
- Bias rail (*Nsub2*: n^{++} implant)
- Bias voltages: 0 V to the bias rail, -400 V applied to the backplane
- Bias resistor:
  - Al (partially high resistivity, equivalent to PolySi)
  - 1.5 MΩ resistance (R_b)
  - The trace of the bias resistor functions as a gate to the PTP structure
- Oxide thickness (*tSio2*): 0.15 µm
- Oxide–silicon interface charge: 8x10^{10} cm^{-2}
- p-stop (*wPsub*: p^{+} implant): ~6 µm
  - nominal surface density: 4x10^{12} cm^{-2}
- PTP gap (*ggap*): ~7 µm each

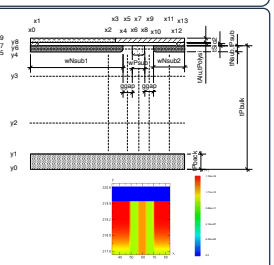

Fig. 5 PTP structure implemented in TCAD (top), and the graphical display of doping densities (bottom), both not to scale.

PTP structure resistance – The current flow between the bias rail (*Nsub2*) and the strip implant (*Nsub1*) was simulated by varying the strip implant potential (V_{strip}), while keeping the bias rail potential at 0 V and the backplane at 400 V.

The PTP resistance was defined as $R_{PT} = I_{strip} / V_{strip}$.

R_{PT} is shown as a function of V_{strip} (Fig. 6). The threshold voltage for PTP turn-on (V_{PT}) is defined as the strip potential at which R_{PT} is half of the bias resistance (1/2 R_b = 0.75 MΩ).

In the simulation, V_{strip} had a negative potential. When expressing V_{PT}, we take the absolute value.

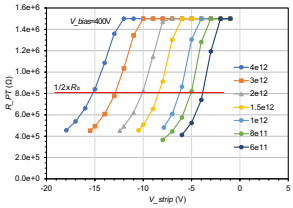

Fig. 6 PTP structure resistance (R_{PT}) as a function of strip potential V_{strip} , with variations in p-stop density.

The turn-on condition is visualized in the electron density. For a p-stop density of 4×10^{12}, at V_{strip} = -1 V, it is not visible, while at -16 V, a thin inversion layer becomes visible at the surface, connecting the strip and bias rail implants across the p-stop area (Fig. 7)

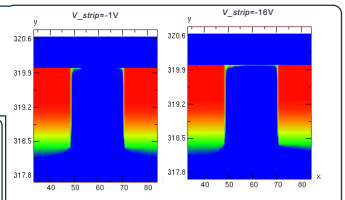

Fig. 7 Plot of the electron density in the PTP region at V_{strip} = -1V (left) and -16V (right), where the latter corresponds to R_{PT} being approximately ½ R_b.

Correlation between p-stop density and V_{PT} – From the plot (Fig. 6), V_{PT} is obtained for p-stop densities ranging from 4×10^{12} to 6×10^{11} cm^{-2} (Fig. 8). The p-stop density correlates exponentially with V_{PT}.

If the p-stop density 4×10^{12} cm^{-2} is scaled to V_{PT} ~ 16 V, V_{PT}~12 V corresponds to a p-stop density of approximately 2×10^{12} cm^{-2}. The corresponding p-stop density is shown on the second axis in Fig. 4. Typical correlation values are listed in Table 2.

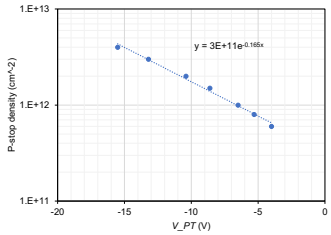

Fig. 8 Correlation between p-stop density and PTP threshold voltage (V_{PT}).

Table 2. Typical correlation between p-stop density and V_{PT}

V_{PT} (V)	p-stop density (cm^{-2})
16	~4×10^{12}
12	~2×10^{12}
6	~8×10^{11}

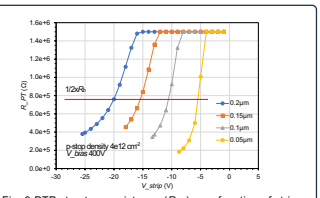

Fig. 9 PTP structure resistance (R_{PT}) as a function of strip potential V_{strip}, with variations in oxide thickness.

Oxide thickness – Oxide thickness beneath the bias resistor is another factor that affects V_{PT}, as the potential difference between the resistor and the p-stop functions as a gate. The dependence of R_{PT} on the oxide thickness was simulated (Fig. 9). V_{PT} shows a linear correlation with the oxide thickness (Fig. 10).

In the process, the variation in oxide thickness is estimated to be small, approximately 0.15 ± 0.004 µm, based on the variation in AC coupling capacitance (Fig. 11). The oxide thickness is not expected to be a major contributor to the variation in V_{PT} . Additionally, the p-stop density is independent of the oxide thickness.

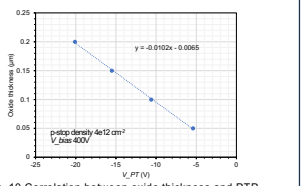

Fig. 10 Correlation between oxide thickness and PTP threshold voltage (V_{PT}).

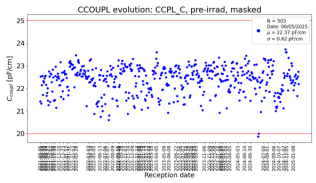

Fig. 11 Trend plot of AC coupling capacitance of strips (C_{coupl}) over the course of production [5].

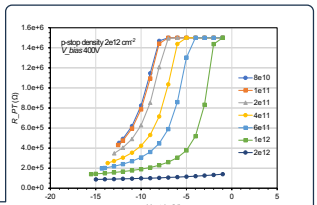

Fig. 12 PTP structure resistance (R_{PT}) as a function of strip potential V_{strip} , with variations in interface charge.

Radiation damage effect – Irradiation with γ rays, charged particles, and neutral particles induces radiation damage in the PTP structure, such as an increase in the interface charge at the oxide–silicon interface and the space charge in the silicon bulk.

The dependence of R_{PT} on the interface charge was simulated for a p-stop density of 2×10^{12} cm^{-2} (Fig. 12). V_{PT} shows linear correlation with the interface charge. Isolation in the PTP structure is lost when the interface charge exceeds 1×10^{12} cm^{-2}.

An increase in the space charge from 4×10^{12} cm^{-3} (non-irradiated) to 2.2×10^{13} cm^{-3} (after a fluence of 1×10^{15} neq/cm^{-2}) leads to an increase in V_{PT} by 3 V under a bias voltage of 400 V (Fig.13). This increase is due to a stronger electric field caused by the larger space charge. The difference is equivalent to a reduction in the interface charge of ~5×10^{11} cm^{-2}.

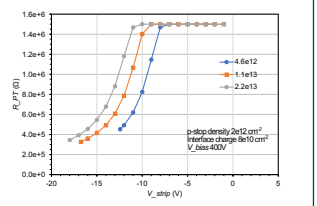

Fig. 13 PTP structure resistance (R_{PT}) as a function of strip potential V_{strip} , with variations in space charge.

Conclusion – We observed rare but occasional deviations in the threshold voltage (V_{PT}) of the punch-through protection (PTP) structure in test chips during quality assurance (QA) process of the ATLAS18 strip sensor production.

Of the two main sensors selected, each processed in a different furnace, one sensor exhibited a flat distribution across the wafer, while the other showed a non-uniform, parabolic distribution with a four-standard-deviation shift toward the wafer edge.

TCAD simulations confirm that V_{PT} correlates well with the p-stop density. By setting the nominal p-stop density (~4×10^{12} cm^{-2}) to correspond to the mean V_{PT} value (~16 V), the p-stop density at the wafer edge, four standard deviations away from the mean, is estimated to be approximately half (~2×10^{12} cm^{-2}).

The low value of 2×10^{12} cm^{-2} should still be sufficient to ensure strip isolation, even after radiation damage, and in the presence of oxide–silicon interface charges with densities as high as 1×10^{12} cm^{-2}.

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[2]A decrease in p-stop density was observed in the MOS capacitor test structure with the p-layer during production [4].