LF-MightyPix: A second HV-MAPS prototype for the LHCb Mighty Tracker

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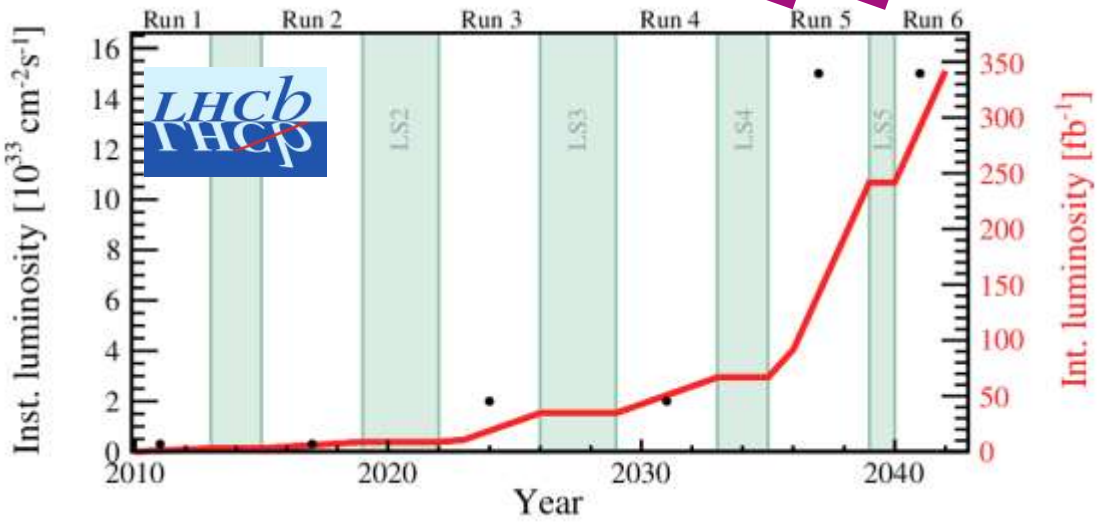
Introduction

- Upcoming experiments: Hight Luminosity
  - High hit-rate capability
  - High radiation hardness
  - **Large area, ~O(10m^2)**

→ Si pixel detectors are good candidates
  - High granularity
  - Radiation hardness has been studied extensively



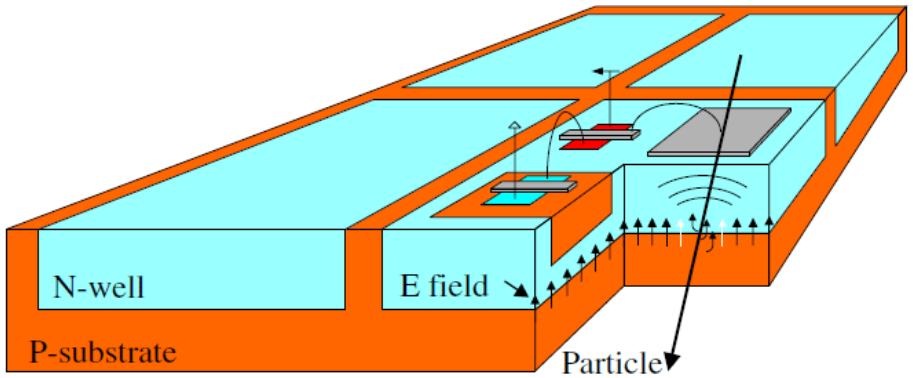
→ Monolithic Active Pixel Sensor (MAPS)
  - Simpler production process suitable for the large-scale production ☺
  - Discontinuation of CMOS process might impact the project ☹

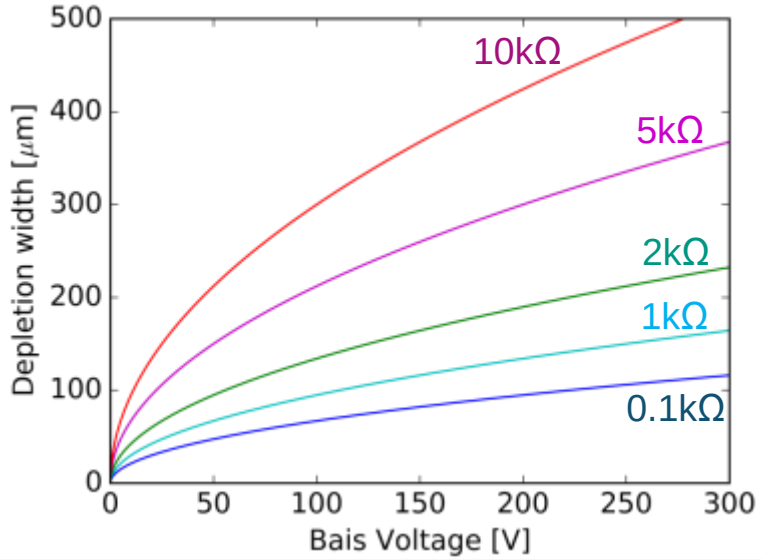
HV-MAPS

- High Voltage Monolithic Active Pixel Sensors (HV-MAPS) = MAPS + High Bias Voltage
  - MAPS: Sensor and readout in a single silicon chip
  - Readout electronics placed inside the n-well and isolated from sensor diode
    - High voltage (~100V) is possible to apply to the sensor diode and deplete sensor

$$\text{Depletion width d} \propto \sqrt{V_{bias} \cdot \rho_{material}}$$

→ Charge collection by drift (not diffusion)
→ Higher radiation hardness





Mighty Tracker in LHCb experiments

- LHCb is a forward-arm spectrometer

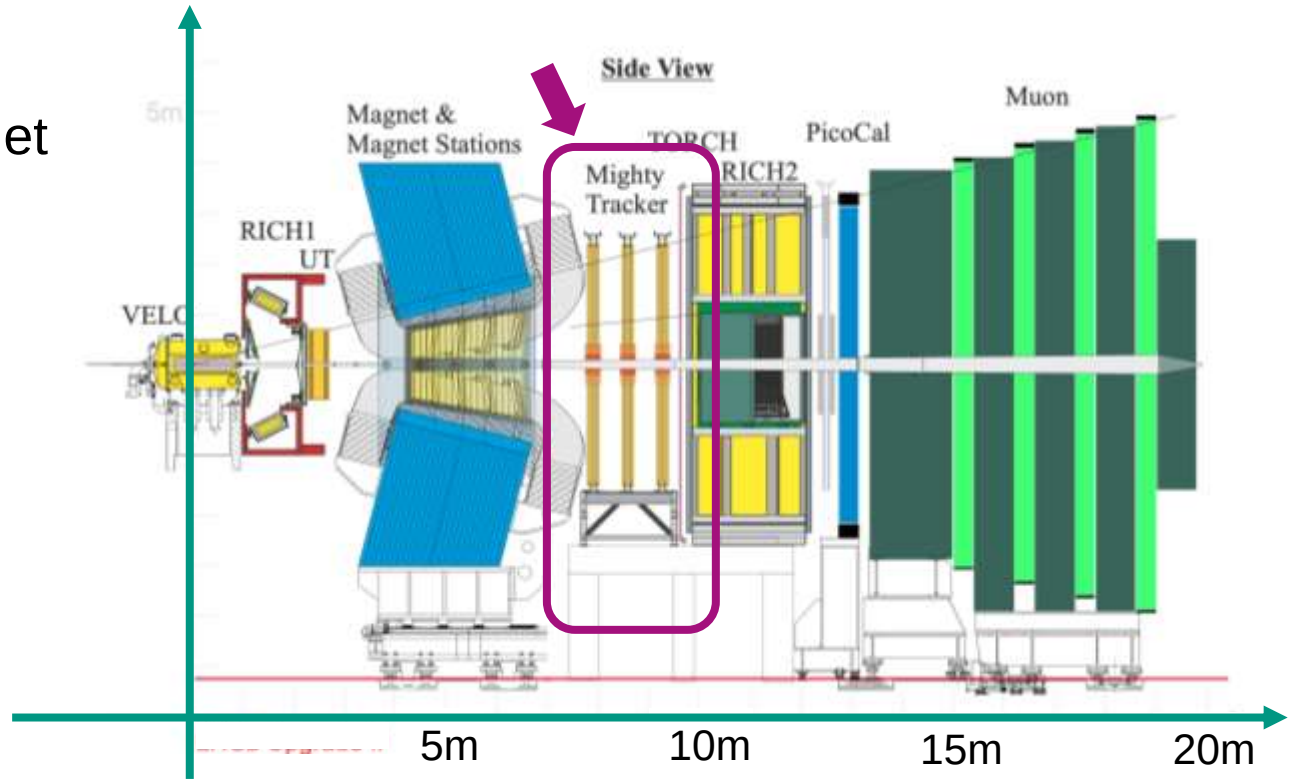
- Upgrade I (SciFi Tracker)
  - 3 tracking stations downstream of the magnet
    - Scintillating fibers

  → Now in operation

- Upgrade II (Mighty Tracker)
  - 3 tracking stations
    - Scintillating fibers
    - **HV-MAPS**

  → Higher hit-rate capability and radiation hardness required to survive in Run 5, 6

Upgrade II



MightyPix (HV-MAPS for Mighty Tracker)

Parameter	MP Specification
Pixel size (bending plane)	$\leqq 100\,\mu m$
Pixel size (non bending plane)	$\leqq 200\,\mu m$
Substrate thickness	$<200\,\mu m$
Pixel orientation	x
Max. Particle Rate	$17\ MHz/cm^2$
Max. Hit Rate	$34Mhit\ s^{-}1cm^{-2}$
Min. length of data word	32
Overall efficiency	>96%
Noise rate (End of life)	$\leq 400kHz/\,cm^2$
Transmission rate	4 links of 1.28Gbit/s each
NIEL	$3 \times 10^{14} n_{eq}/cm^2$
TID	40 MRad
Power Consumption	$\leq 150\ mW/\,cm^2$

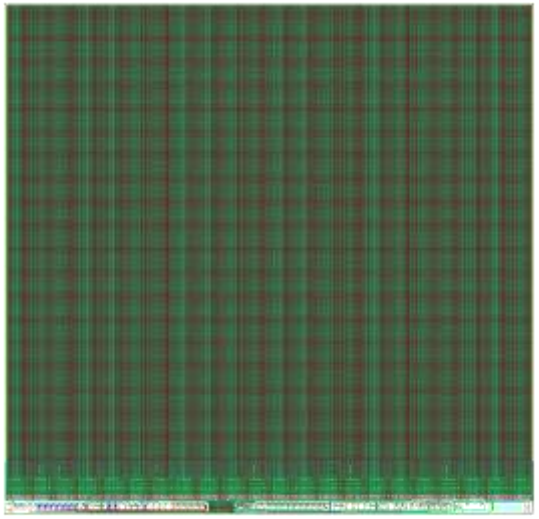
Specifications for the LHCb MightyPix sensor, S. Bachmann et al., LHCb-INT In preparation

- Data Output
  - 4 output links or multiplexing to 2 or 1 output
    - 2 data formats: 48bit/hit 32bit/hit
  - DC-Balancing by multiplicative scrambler
- Experiment Control System
  - Multidrop downlink, daisy chain uplink to occupy min. number of eLinks
  - Chip configuration and tuning
  - Monitoring features (ADC, Status registers)
  - I2C interface for debugging
- Timing and Fast Control
  - 5 needed commands
- PLL, BX-CLK phase shifter
- Serial Powering Regulators

MightyPix Development

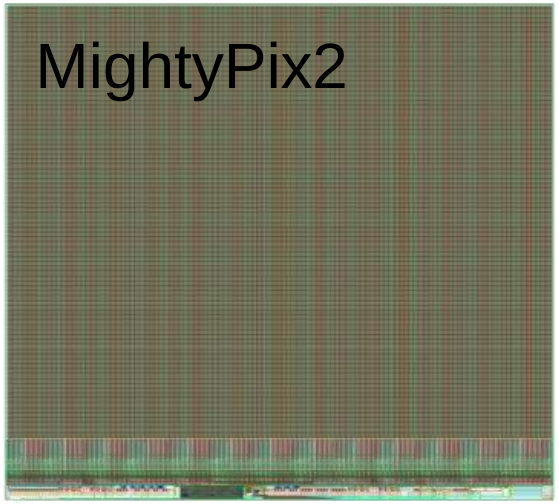
MightyPix1

5 mm x 20 mm
180nm CMOS process
Basic LHCb specific digital functions (2022-2023)



P2Pix

20 mm x 20 mm
180nm CMOS process
Mightypix identical analog matrix (2024-2025)



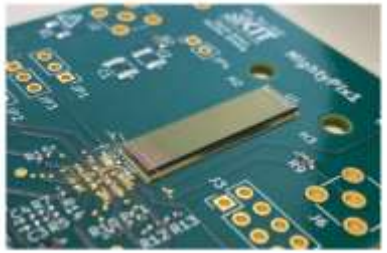
20 mm x 16 mm
180nm CMOS process
(Almost) Full LHCb specific functions (2025-2026)

20 mm x 20 mm
180nm CMOS process
Final chip

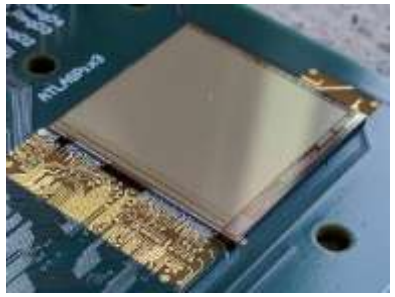
HV-MAPS in alternative CMOS Process

- Further advantages of HV-MAPS: Several foundries can fabricate chips
  - Commercially available CMOS process
  - No change in CMOS process except resistivity of wafers for larger signal charge.

➡ Many types of HV-MAPS has been developed using different foundry, feature size, possible options to full fill each projects' requirements

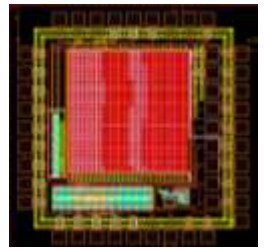


180nm CMOS process



180nm CMOS process

SiGe 130nm BiCMOS process



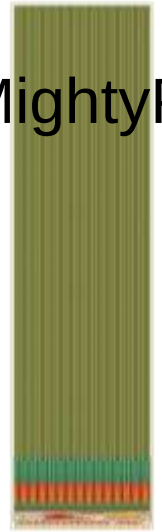
55nm CMOS process

- A prototype using another CMOS process as a backup
- LHCb specific digital function in silicon

➡ HV-MAPS using 150nm CMOS

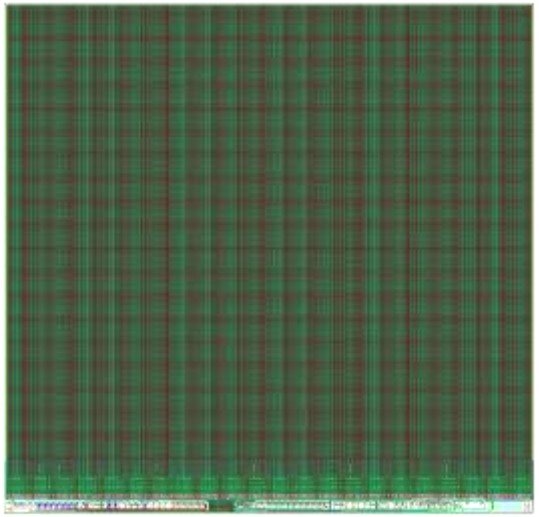
MightyPix Development

MightyPix1



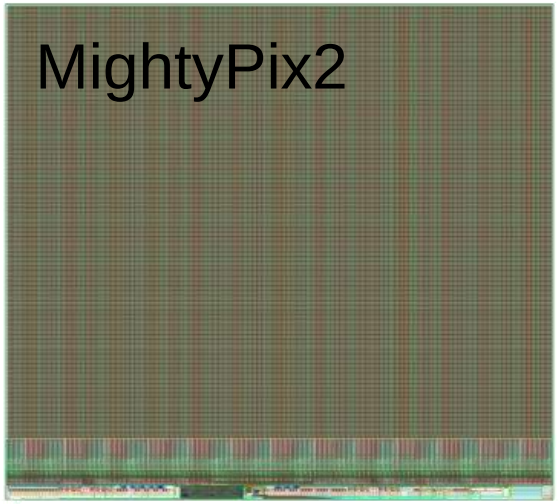
5 mm x 20 mm
180nm CMOS process
Basic LHCb specific digital functions
(2021-2022)

P2Pix



20 mm x 20 mm
180nm CMOS process
Mightypix2 identical analog matrix
(2024-2025)

MightyPix2

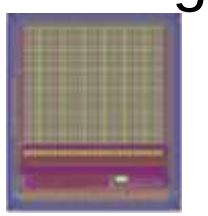


20 mm x 16 mm
180nm CMOS process
(Almost) Full LHCb specific functions (2024-2025)

MightyPix3

20 mm x 20 mm
180nm CMOS process
Final chip

LF-MightyPix



3 mm x 4 mm
150nm CMOS process
Improved LHCb specific digital functions
(2024-2025)

LF-MightyPix

Parameter	MP Specification
Pixel size (bending plane)	100 µm ✓
Pixel size (non bending plane)	≦ 200 µm ✓
Substrate thickness	**280 µm**
Pixel orientation	x
Max. Particle Rate	17 MHz/cm²
Max. Hit Rate	**30M hits/s/cm²**
Min. length of data word	**48**
Overall efficiency	>96%
Noise rate (End of life)	≤ 400kHz/ cm²
Transmission rate	**1** links of 1.28Gbit/s each
NIEL	$3 \times 10^{14} n_{eq}/cm^2$
TID	40 MRad
Power Consumption	≤ 150 mW/ cm²

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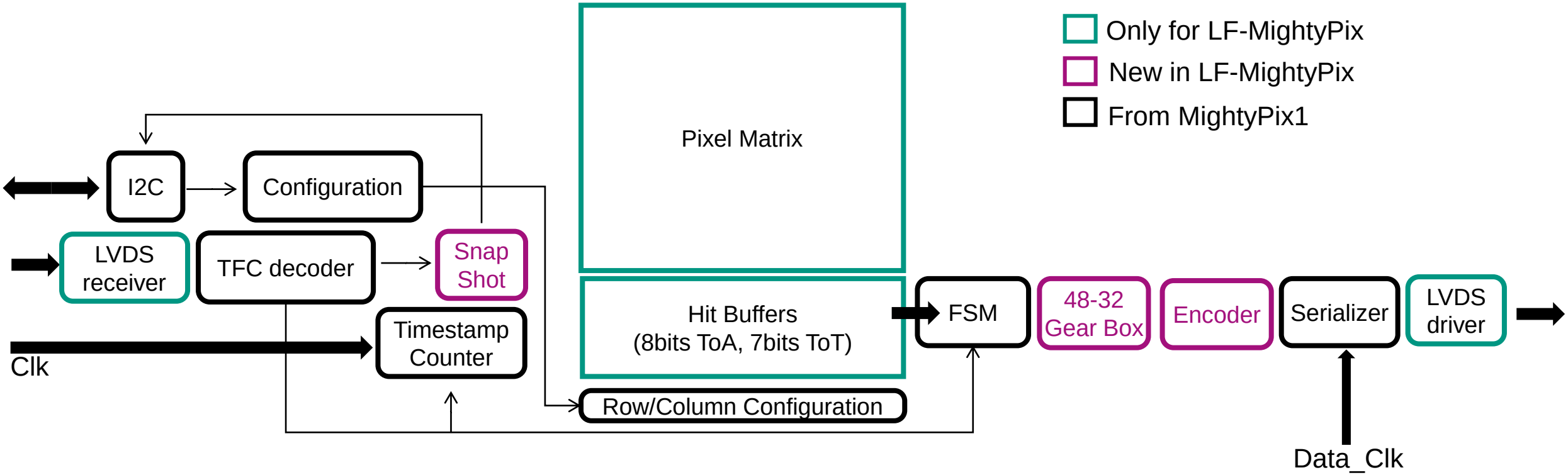
  - DC-Balancing by multiplicative scrambler
- Experiment Control System
  - Multidrop downlink, daisy chain uplink to occupy min. number of eLinks
  - Chip configuration and tuning
  - Monitoring features (ADC, Status registers)
  - **I2C interface for debugging**
- **Timing and Fast Control**
  - 5 **(4 + 0.5) needed commands**
- Clock and Reset
- Serial Powering Regulators

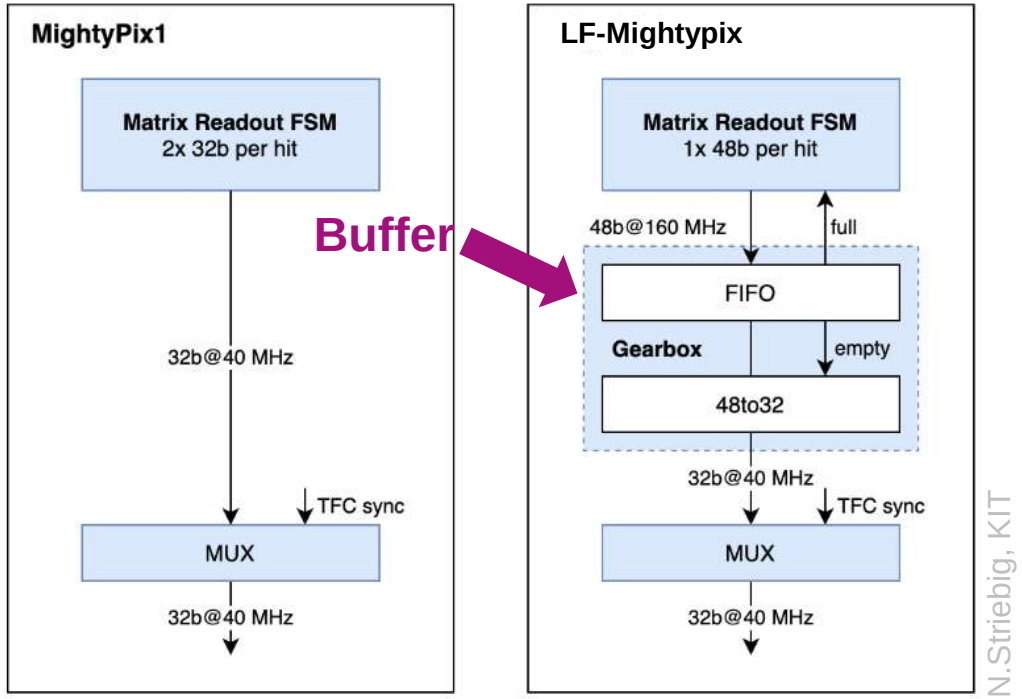
Block Diagram of LF-MightyPix



In-pixel readout, Hit buffer: customized for 150nm CMOS process
TFC, Data Links: implemented in 150nm CMOS process before implementing in large chip

New Features in LF-MightyPix

- 1.28Gbp data link: 32bits/packet
  - MightyPix1: 64bits/hit, ~17MHz/cm^2
  - LF-MightyPix : 48bits/hit, **~30 MHz/cm^2**



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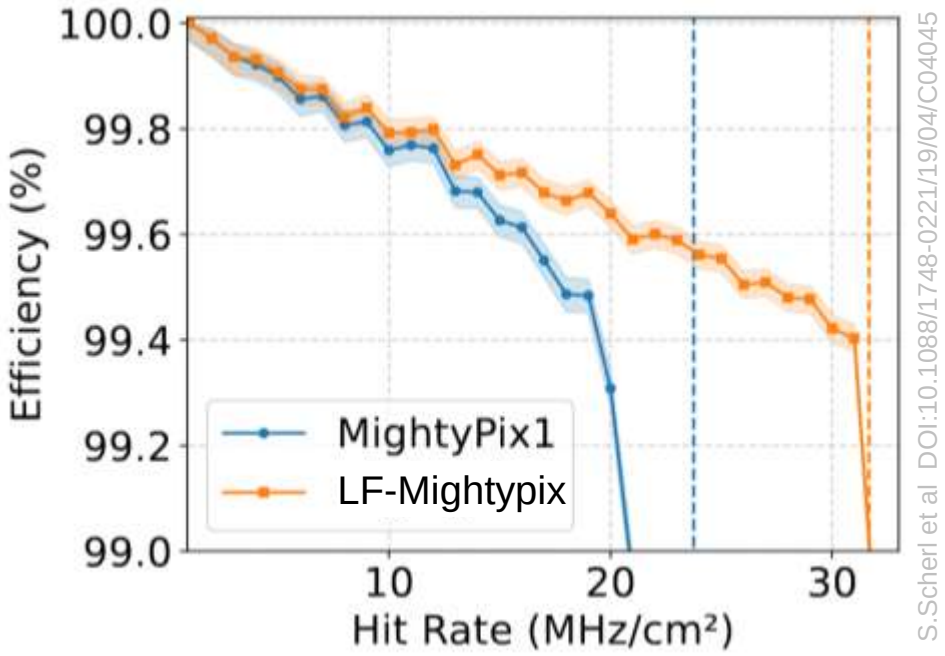
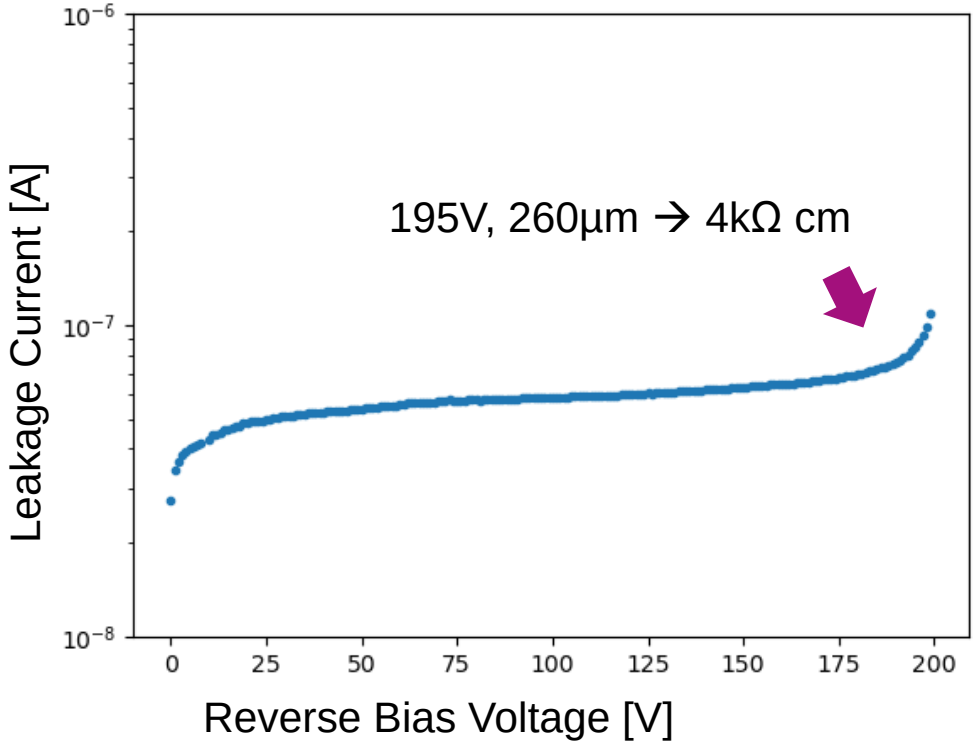
Simulated Readout Efficiency



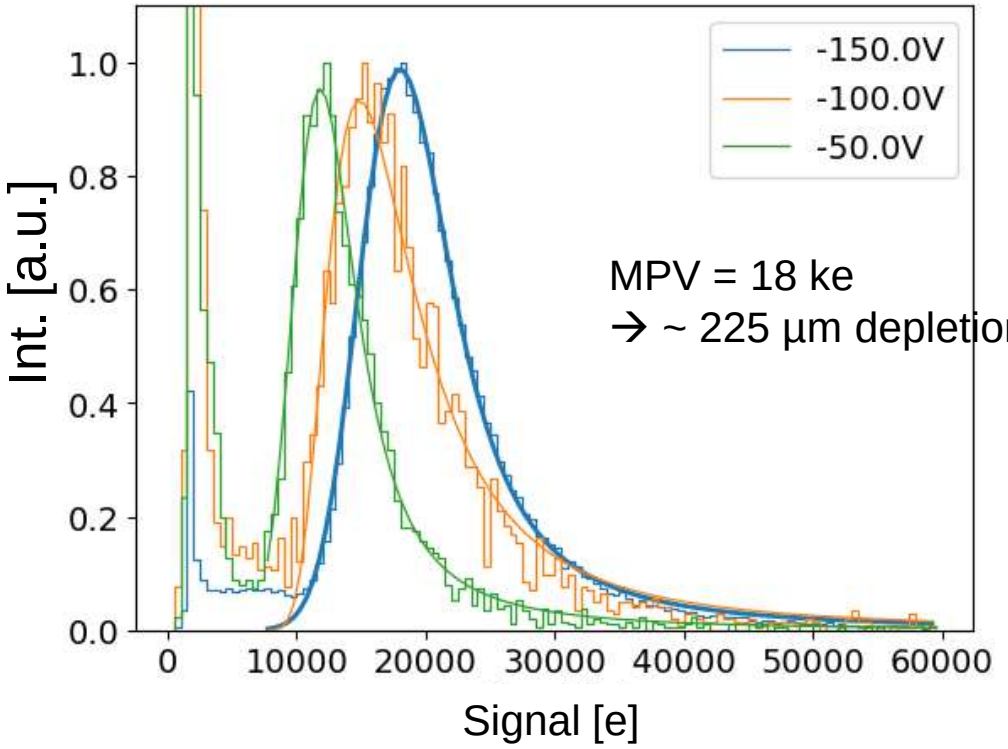
S.Scherl et al DOI:10.1088/1748-0221/19/04/C04045

Sensor of LF-MightyPix

IV-Curve



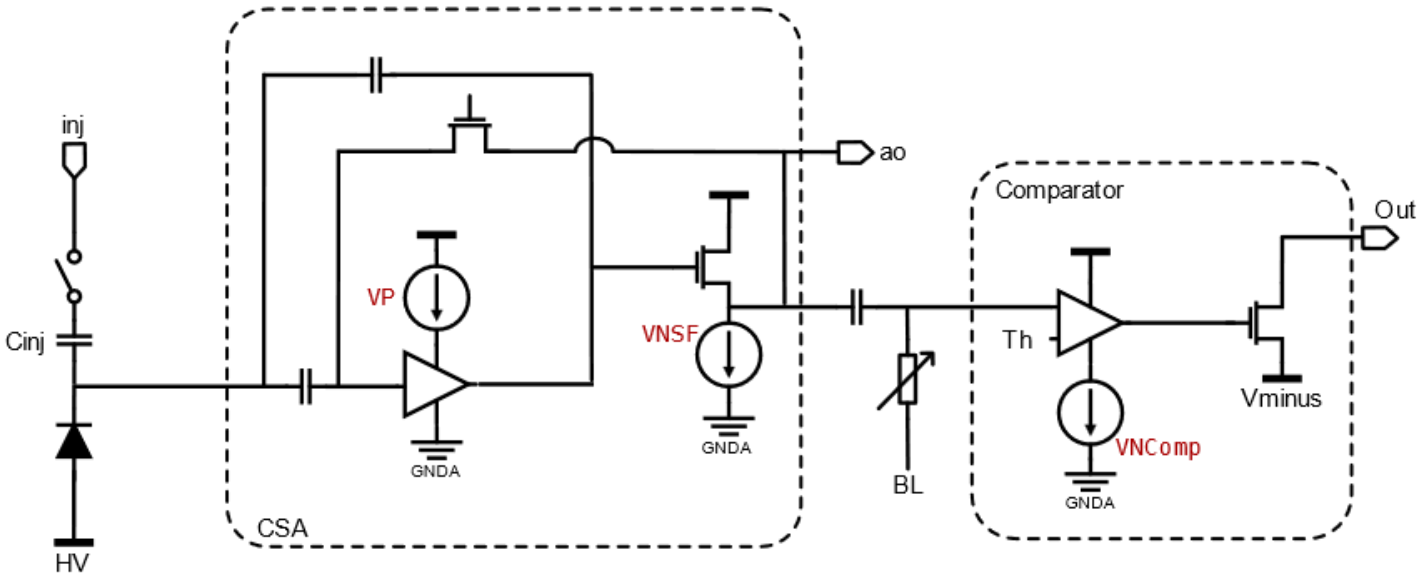
^{90}Sr Spectrum

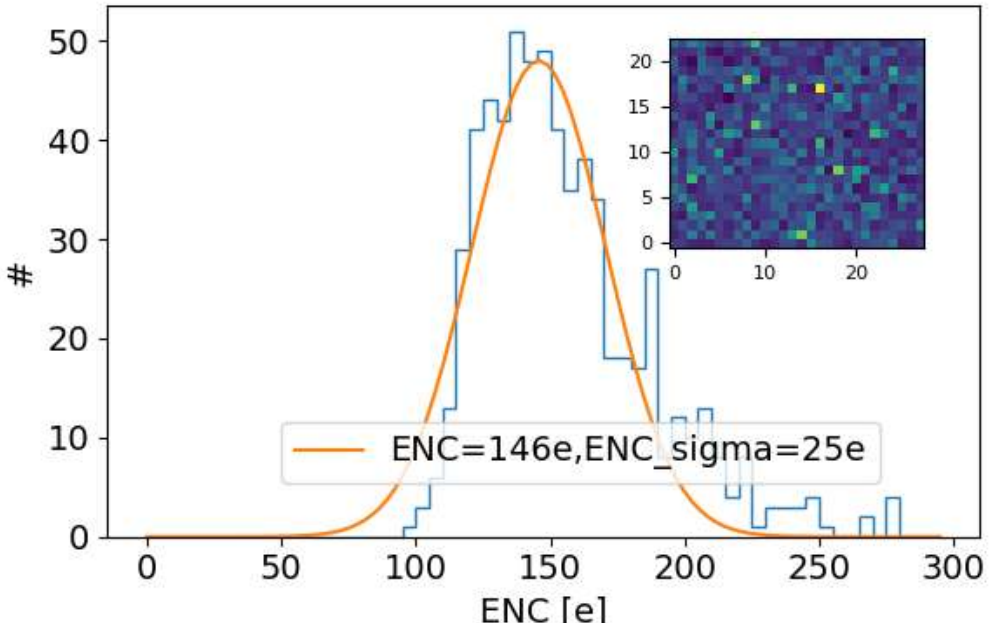


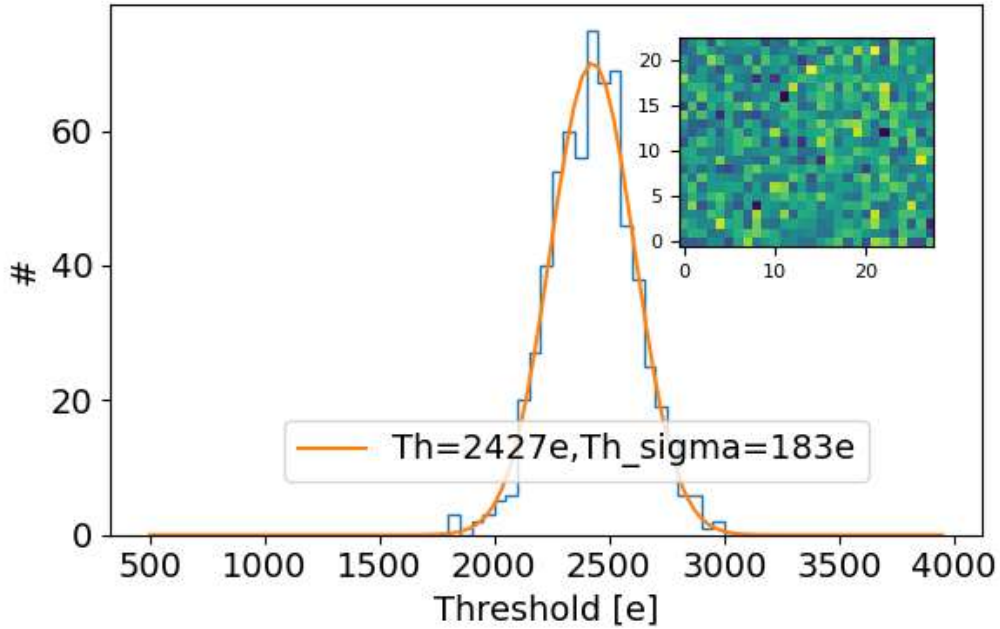
Charge collection from sensor of > 200 µm thickness

In-Pixel Readout of LF-MightyPix

- Designed and optimized for the150nm CMOS process
- CSA + Comparator w/ 4bits fine Tuning DAC
  - ENC 146e
  - Thresholds are in a tunable range

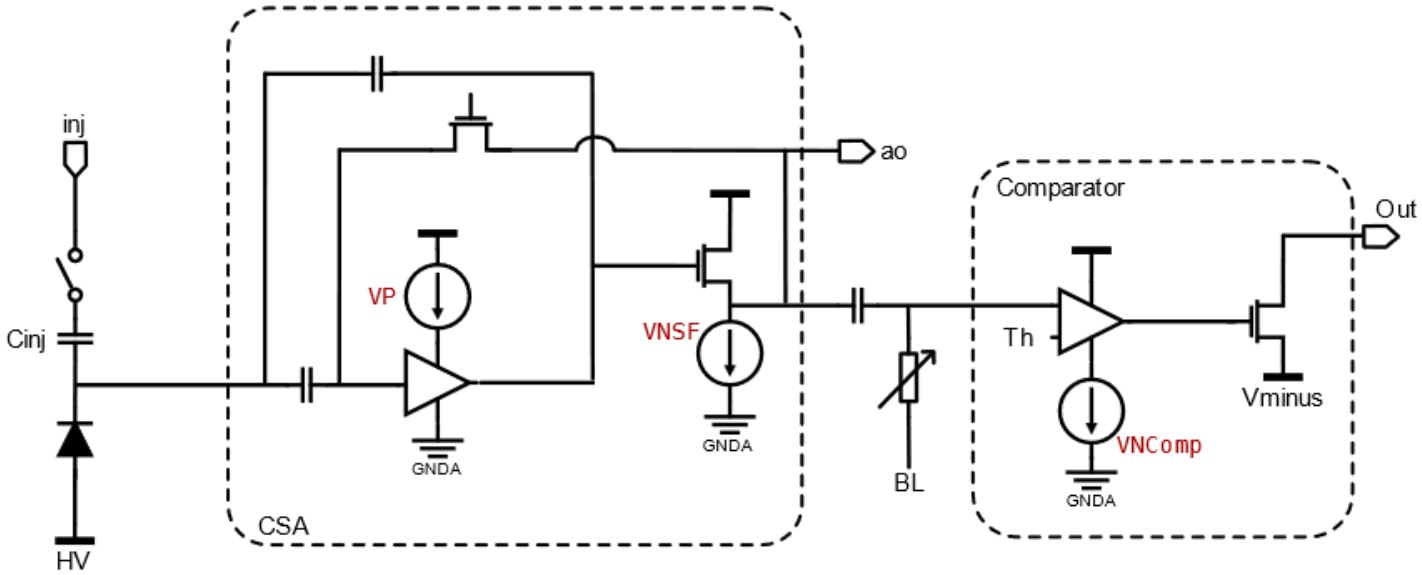


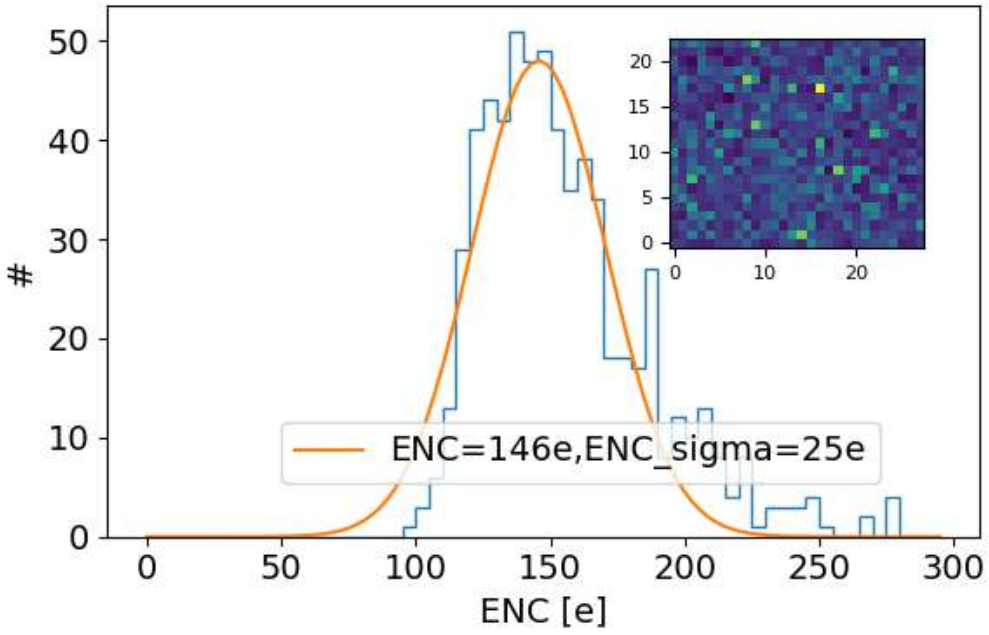


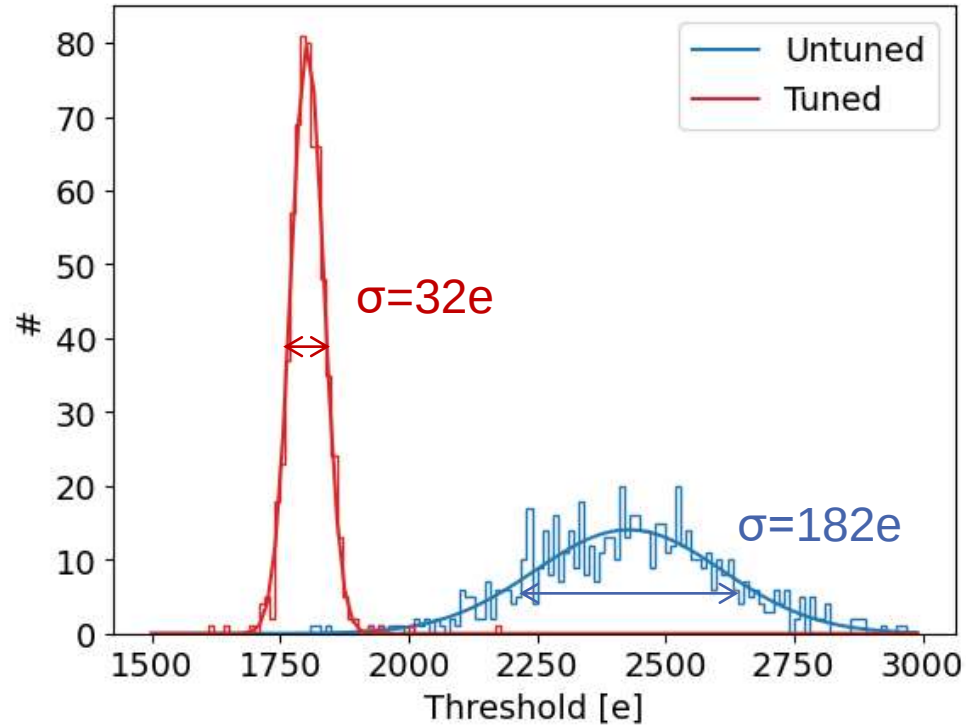


In-Pixel Readout of LF-MightyPix

- Designed and optimized for the150nm CMOS process
- CSA + Comparator w/ 4bits fine Tuning DAC
  - ENC 150e
  - Threshold distribution is in a tunable range

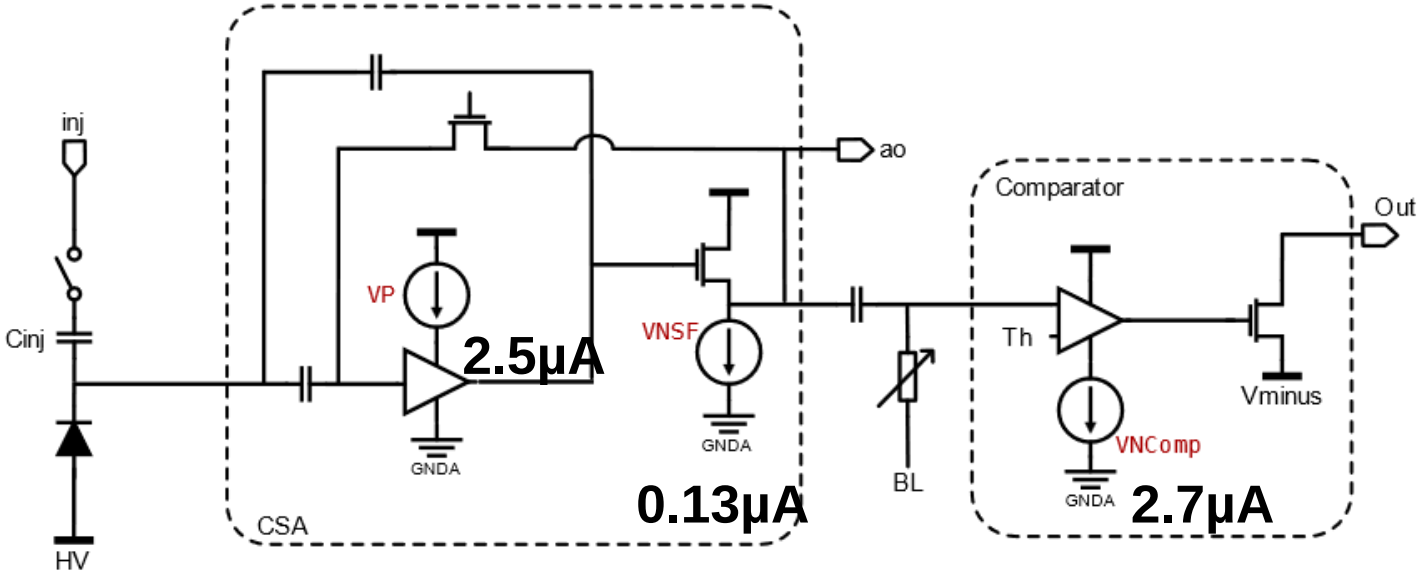






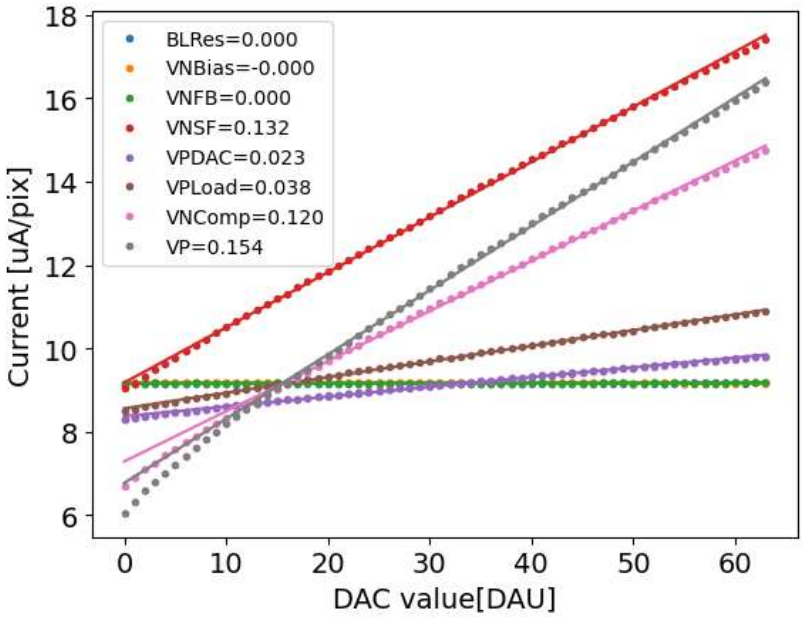
In-Pixel Readout of LF-MightyPix

- CSA + Comparator w/ 3bits fine tuning
- Ddesigned and optimized for the150nm CMOS process
- Pixel currents are supplied via the current mirrors controlled by DACs.
  - The slope of VDDA current indicate the power consumption of each block per 1DAU



➡ 5.92 µA/pix (*cf.* Designed Value = 6µA/pix)

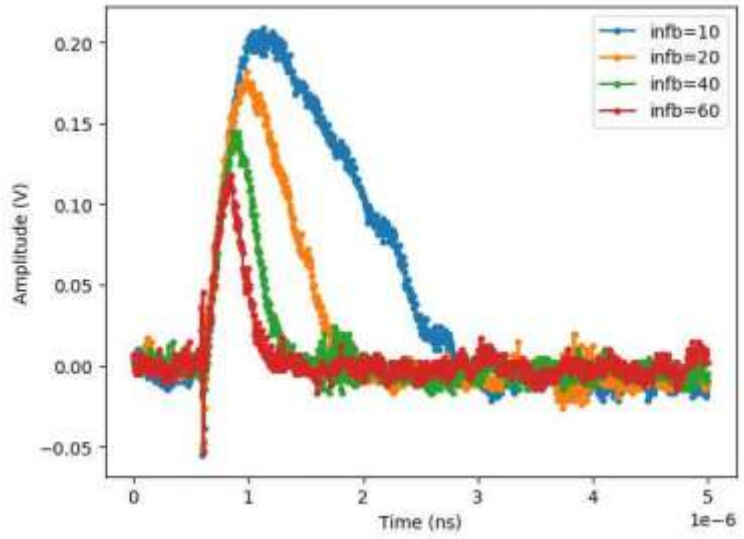
Current Consumption of the Pixels



LF-MightyPix to MightyPix2

- MightyPix1
  - 1.28Gbps data link
- LF-MightyPix
  - 48bits/hit data link with Gear Box
  - TFC
  - Feasibility as a backup process
- **Full reticle chip (P2Pix) from another project**
  - **Pixel Matrix**
  - **Serial Powering**
- MightyPix2 (new features)
  - 4 to 2, 4 to 1 data link Multiplexer
  - 32bits/hit mode
  - DC balanced ECS and TFC decoder
  - SEU hardened digital logics
  - Clock and Resets

Analog output of P2Pix



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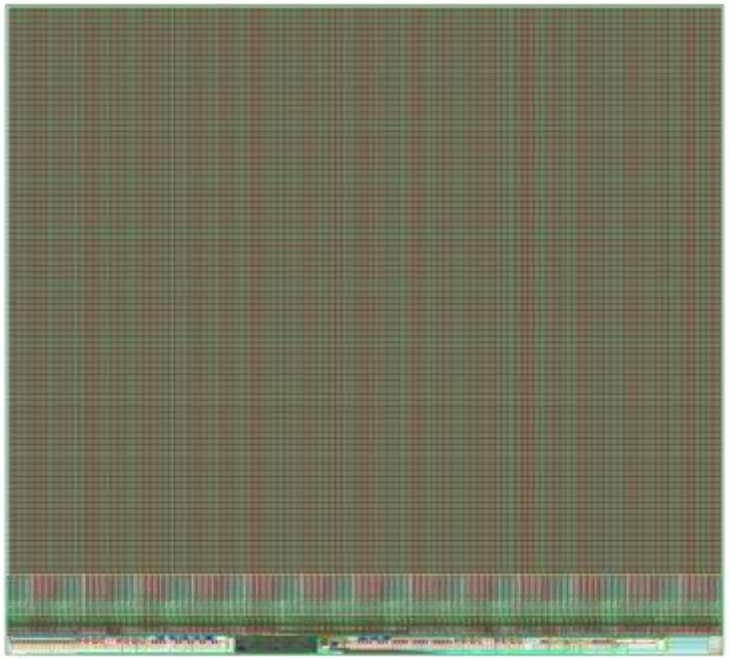
Further tests are on-going

LF-MightyPix to MightyPix2

- Mightypix1
  - 1.28Gbps data link
- LF-Mightypix
  - 48bits/hit data link with Gear Box
  - TFC
- P2Pix
  - Pixel Matrix
  - Serial Powering
- New features
  - 4 to 2, 4 to 1 data link Multiplexer
  - 32bits/hit mode
  - ECS(slow control) and TFC 6b8b decoder
  - SEU hardened digital logics

MightyPix2



Submission: Oct 2025 !

Summary

- LHCb-Control/DAQ compatible HV-MAPS, LF-MightyPix, has been produced using 150nm CMOS process in addition to MightyPix1 (180nm CMOS process, 400Ω/cm^2)
- The test results of sensors and pixel matrix shows feasibility of the 150nm process.
- Experiences in porting Sensor/Readout design ensured a backup plan for long-term projects
- Using results of MightyPix1, LF-MightyPix and chips from other projects, MightyPix 2 has been designed and submitted