# MAPS-based LHCb Upstream Pixel Tracker: challenges and development

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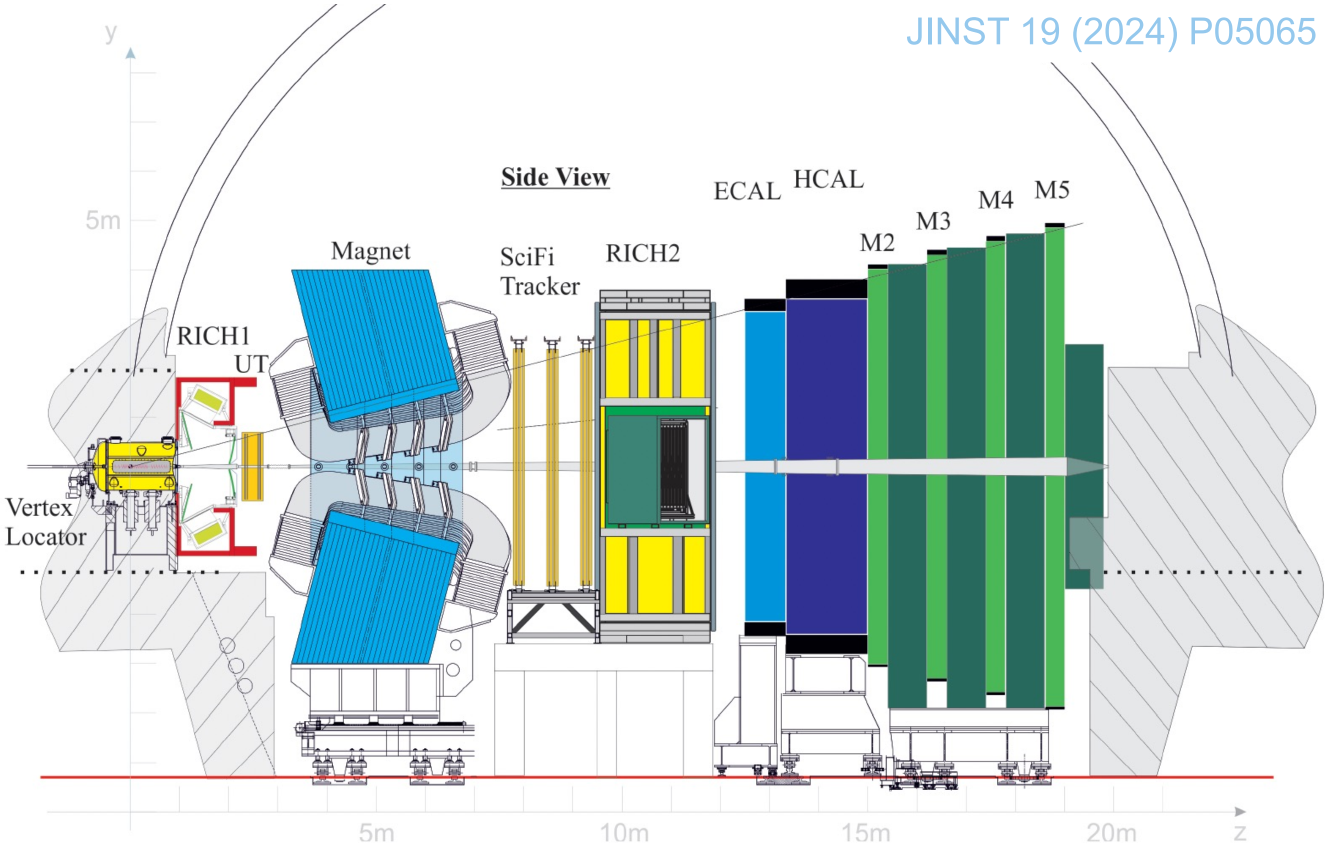
The 14th "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD14)

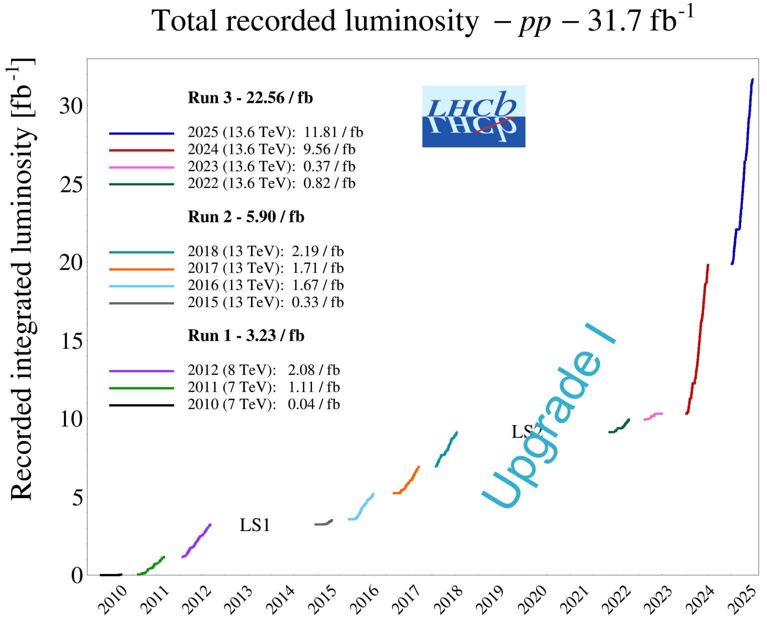
Taipei, 17th Nov 2025

# LHCb detector … upgraded!

- Single-arm spectrometer at LHC dedicated for heavy flavour physics

JINST 19 (2024) P05065

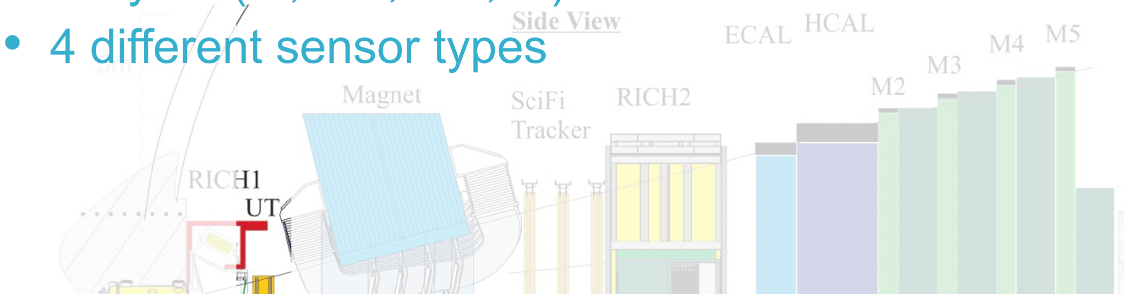


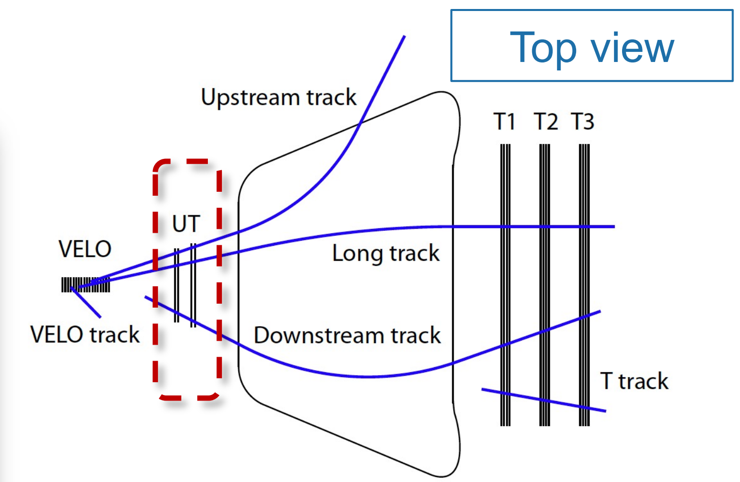



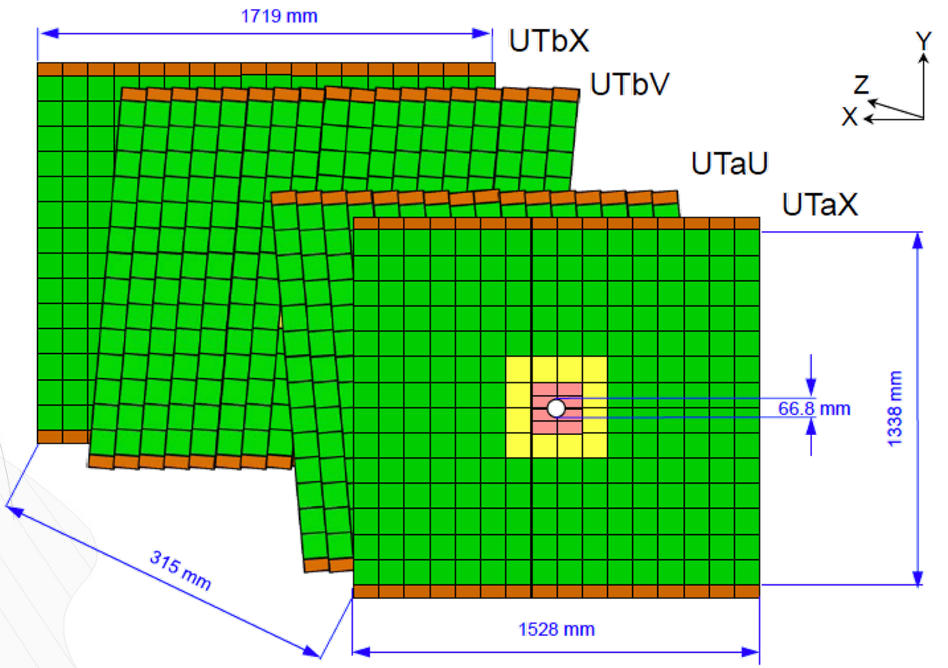

$4.0 \times 10^{32} cm^{-2} s^{-1}$
$\rightarrow 2.0 \times 10^{33} cm^{-2} s^{-1}$

# Upstream Tracker

- Key component in tracking
  - Reducing ghost rate, speeding up tracking, crucial for long-lived particles like $K_S, \Lambda$
- Silicon strip detectors
  - 4 layers $(0°, +5°, -5°, 0°)$
  - 4 different sensor types

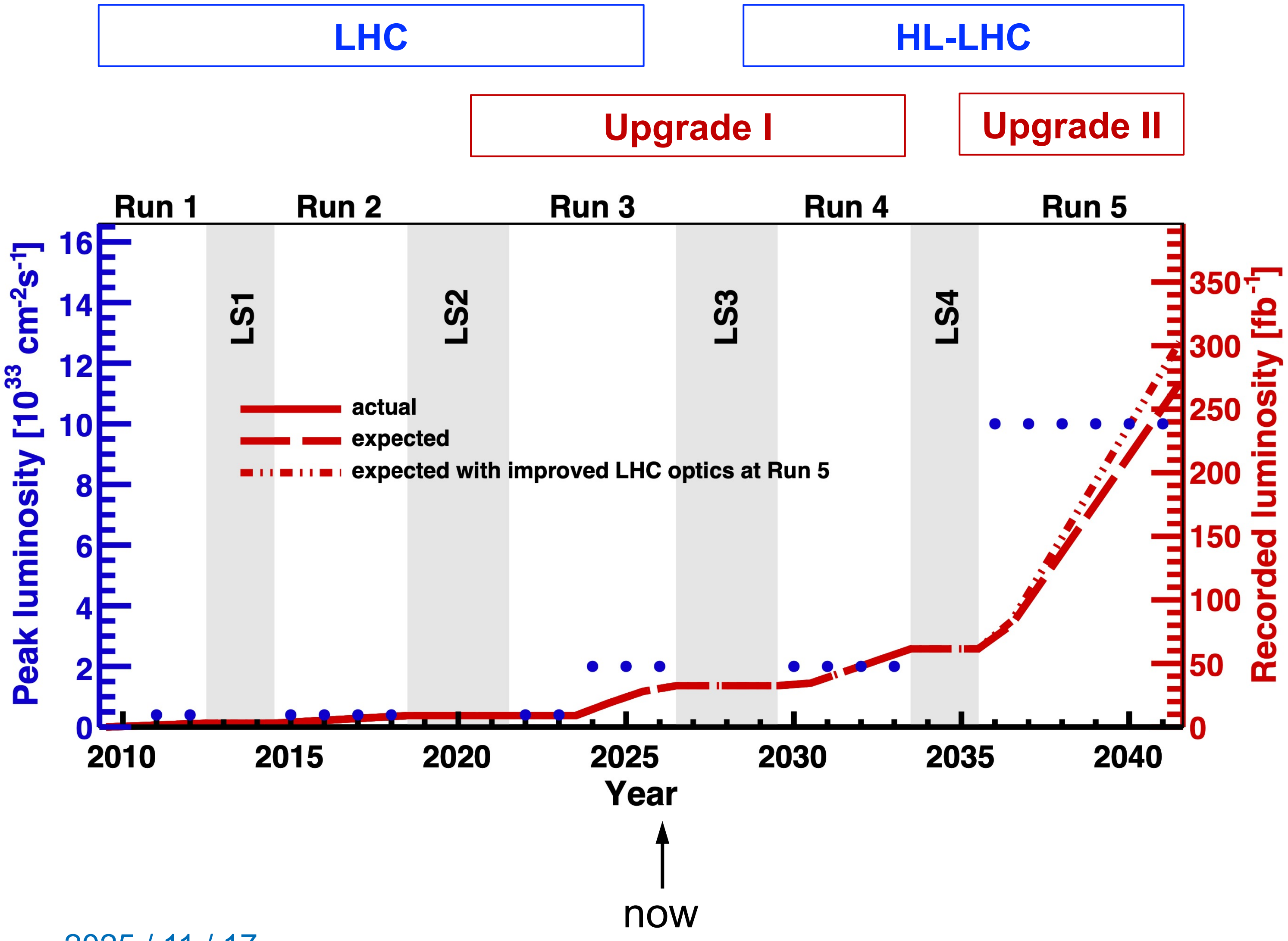



| Sensor | Type | Pitch, μm | Length, mm | Strips | Sensor # |
|---|---|---|---|---|---|
| A | p-in-n | 187.5 | 98 | 512 | 888 |
| B | n-in-p | 93.5 | 98 | 1024 | 48 |
| C | n-in-p | 93.5 | 49 | 1024 | 16 |
| D | n-in-p | 93.5 | 49 | 1024 | 16 |

# Upgrade II



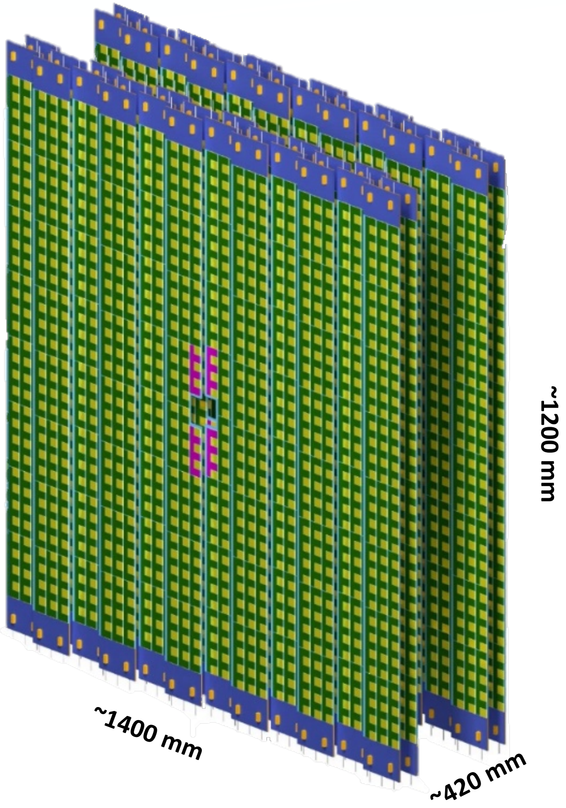

- Upgrade II to fully exploit flavour physics potential in HL-LHC
- Target luminosity:
  - $1.0 \sim 1.5 \times 10^{34} \mathrm{cm}^{-2}\mathrm{s}^{-1}$
  - $300 \sim 350\ \mathrm{fb}^{-1}$
- High-lumi operation challenges:
  - Pile-up: $\mu \sim 1 \rightarrow 5$ (UI) $\rightarrow 40$ (UII),
  - High multiplicity (→ occupancy)
  - Severe radiation damage
  - High data rates (200 Tb/s)

*Expression of interest*
*CERN-LHCC-2017-003*
*Physics case*
*CERN-LHCC-2018-027*
*Framework TDR*
*CERN-LHCC-2021-012*
*Scoping Document*
*CERN-LHCC-2024-010*

# Upstream Pixel detector

- Challenges for UT due to higher luminosity
  - Increased track density → higher granularity
  - Higher bandwidth
  - Increased radiation level:

    NIEL up to $1 \times 10^{15}\ n_{eq}/cm^2$ (without safety factor!)
- A MAPS based pixel detector proposed
  - Sensor options: HVCMOS / small electrode CMOS




6.8 $m^2$ active area in ‘middle-scenario’

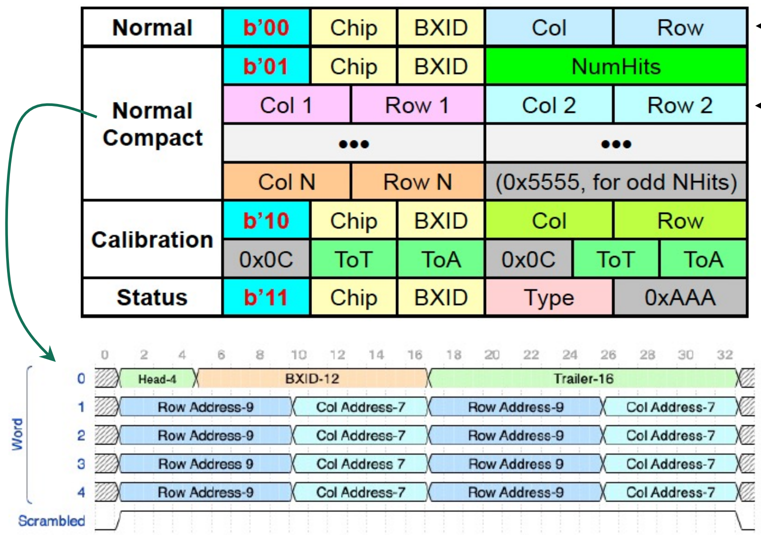
Collaborations of 12 groups from China, France, Mongolia and US

# UP Challenges for sensors

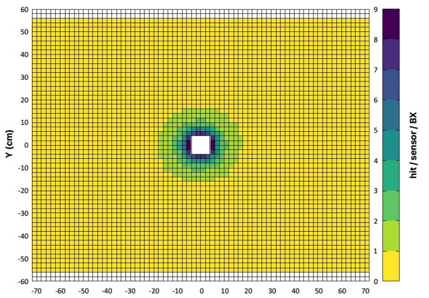
| Parameters | Specification |
|---|---|
| Sensor size | $\sim 2\times2\ \mathrm{cm}^2$ |
| Pixel size, rectangular<br>Pixel size, square | $\leq 50\times200\ \mu\mathrm{m}^2$<br>$\leq 85\times85\ \mu\mathrm{m}^2$ |
| Substrate thickness | $< 200\ \mu\mathrm{m}$ |
| Max particle rate | $\sim 4\ \mathrm{hits/cm^2/BX}$ |
| Max hit rate | $74\ \mathrm{MHz/cm^2}$ |
| In-time efficiency | $> 99\%$ within 25 ns |
| TID | $\sim 200$ MRad * |
| NIEL | $3\times10^{15} n_{\mathrm{eq}}/\mathrm{cm}^2$ * |
| Power consumption | $\leq 200\ \mathrm{mW/cm^2}$ |

* Safety factor of 3 assumed

- High data rate, radiation tolerance & good timing for moderate power
- Functionalities required for system
  - Daisy-chaining 4 chips
  - SLDO to allow serial powering
- Exact values subject to minor modification as simulation improves



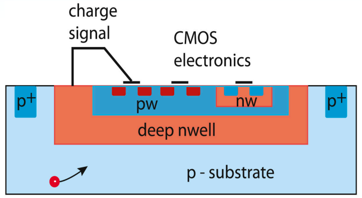

Proposal for data format



# Sensor R&D with 55nm HVCMOS

- HVCMOS: a promising technology candidate
- Prototypes developed using advanced 55nm process

*NIM A1069 (2024) 169905*
*JINST 20 (2025) C10011*



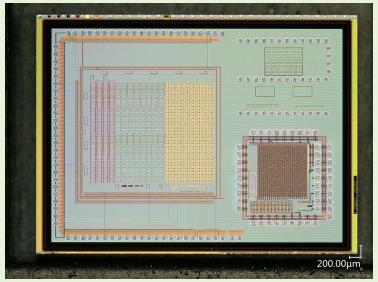

COFFEE

CMOS SENSOR IN FIFTY-FIVE NM PROCESS

**COFFEE 2**

**First HVCMOS 55nm prototype chip**

- Breakdown at -70V
- Responsive to laser, X-ray and beta-ray sources




*Hui Zhang's talk @ HSTD14*

Validation of process modification

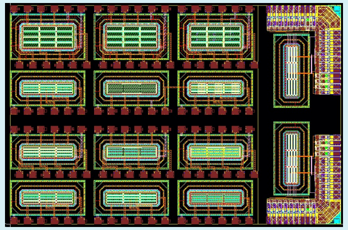
Quarter-size chip submission

## Submission timeline

… | 2022 | 2023 | 2024 | 2025 | 2026 | …

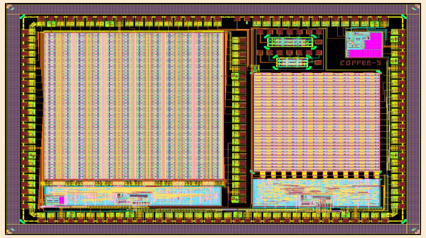
**COFFEE1**

- Prototype in LL process
- Validation of deep N-well structure



**COFFEE3**

- Two pixel arrays with data-driven readout
- Designed for good timing resolution and moderate power consumption



*Yang Zhou's talk @ HSTD14*

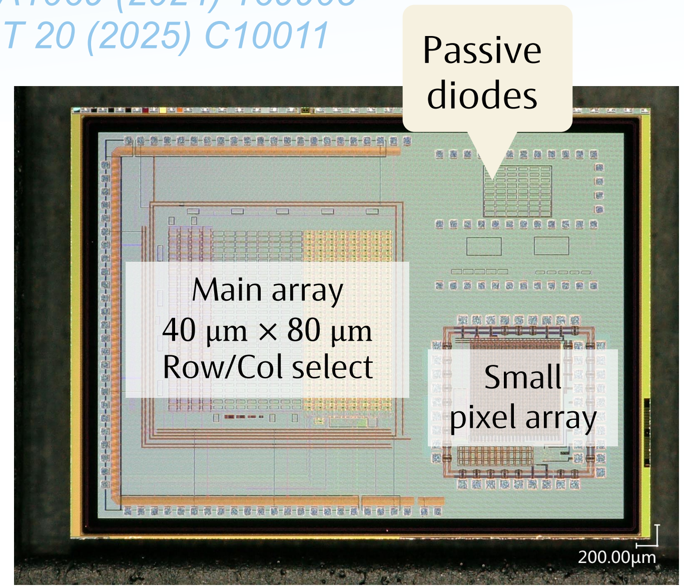
Large prototype planned ~end 2027

*Synergy with future electron-positron collider: Xiaojie Jiang's poster @ HSTD14*

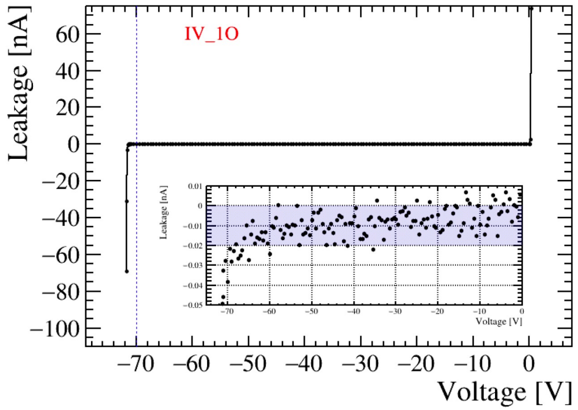
# COFFEE2

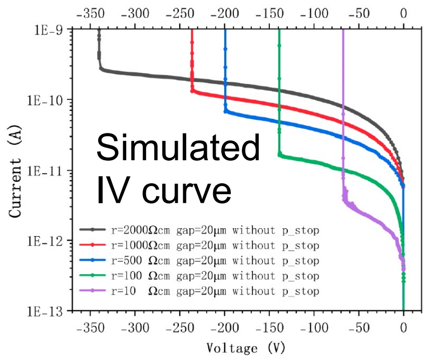
NIM A1069 (2024) 169905
JINST 20 (2025) C10011

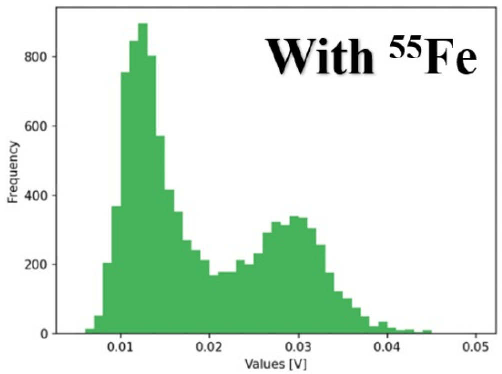
- First HVCMOS prototype in 55nm process
  - $4\ \mathrm{mm} \times 3\ \mathrm{mm}$
  - Triple-well process
  - Regular wafer of a few $\Omega \cdot \mathrm{cm}$
  - Passive arrays + Two pixel arrays with in-pixel amplifier and more digital design
- IV shows breakdown at ~ -70V
  - Simulation shows should improve with substrate resistivity

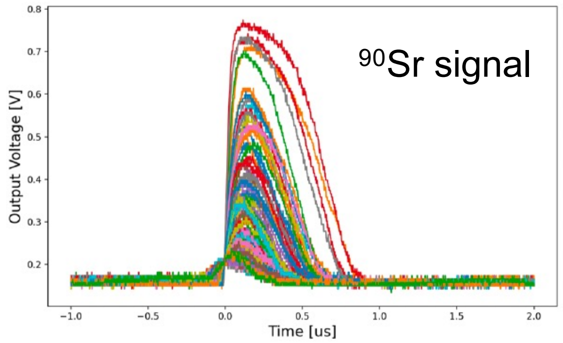



- Responses to laser, radioactive sources



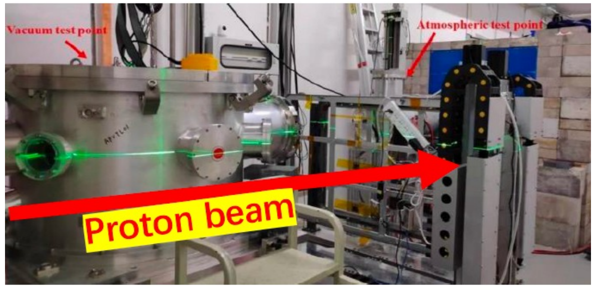



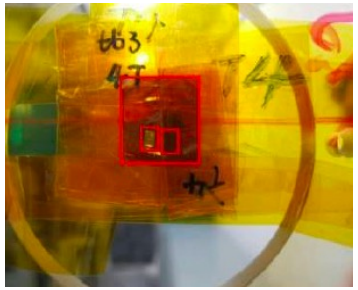



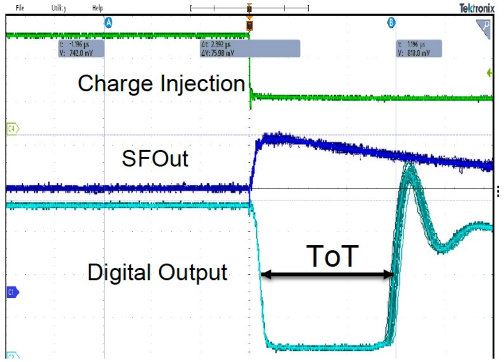
# COFFEE2

- Irradiated to a few $10^{14}$ $n_{eq}/cm^2$
  - Chip still functioning
- In-pixel circuit working
  - Digital circuit using PMOS shows crosstalk with sensor, as expected for triple-well process
  - Can be mitigated by adding a deep p-well isolation PMOS and deep n-well

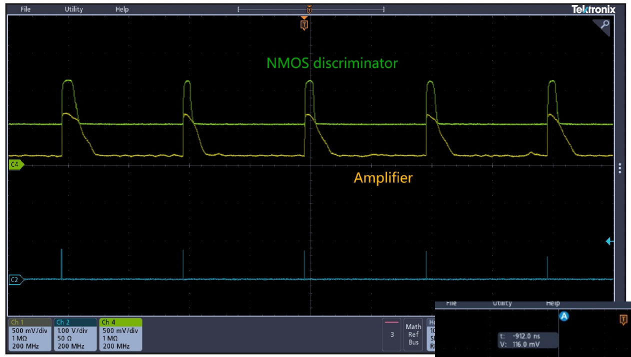


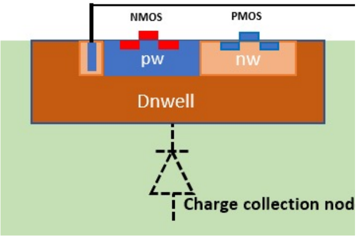
Irradiation tests using 80 MeV proton beam @ Chinese Spallation Neutron Source

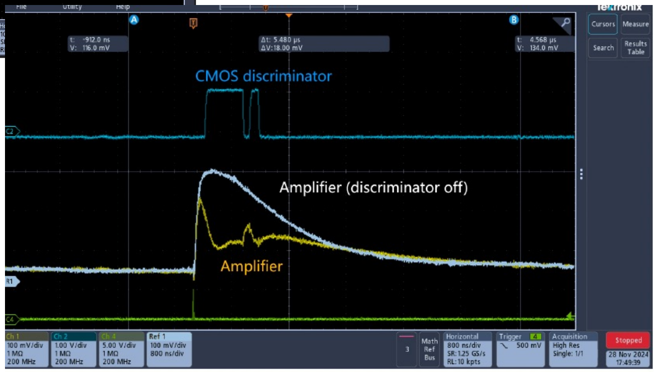



*Hui Zhang's talk*




NMOS discriminator and CMOS discriminator output



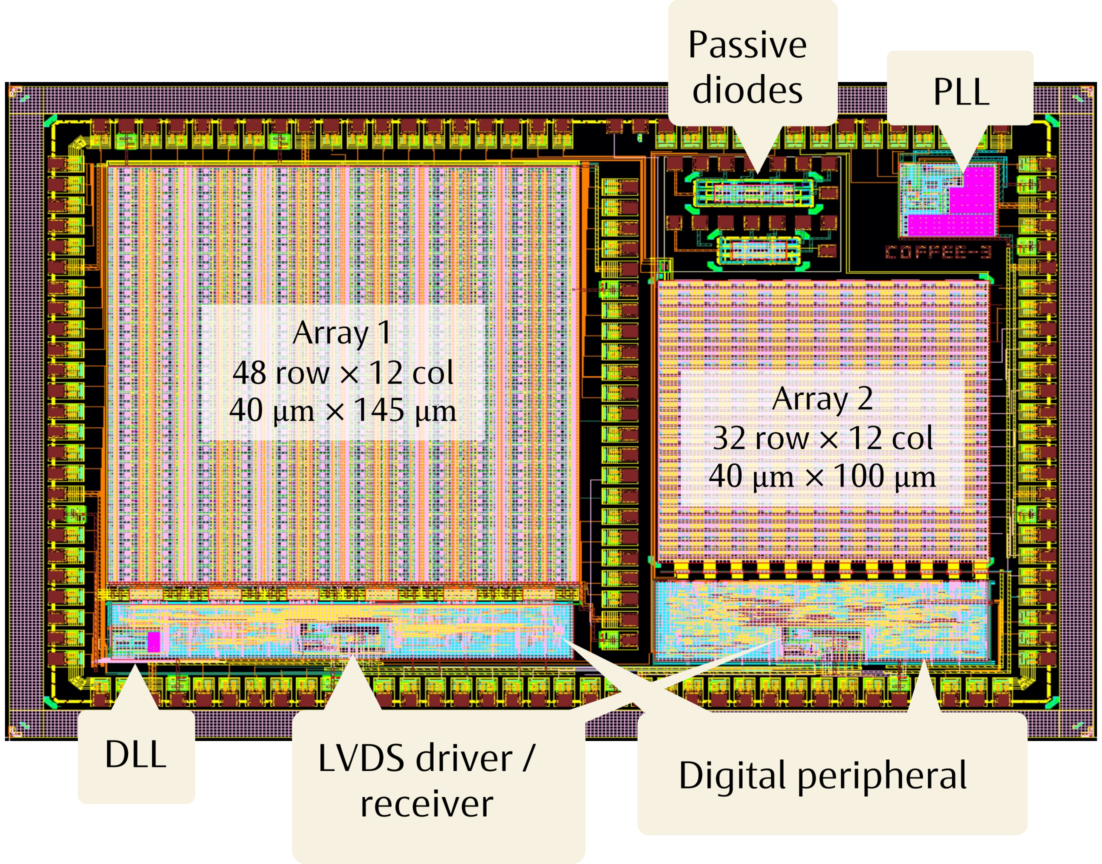
# COFFEE3 sensor

- A prototype with key designs implemented to tackle high data rate at Upgrade II
  - 4mm x 3mm, submitted in Jan 2025, received in May 2025
  - Two novel readout architectures in two pixel arrays
  - Standalone function modules to integrate into full-size chip

*Yang Zhou's talk*

Architecture 1:

CMOS in-pixel digital design fully exploiting 55nm advantage



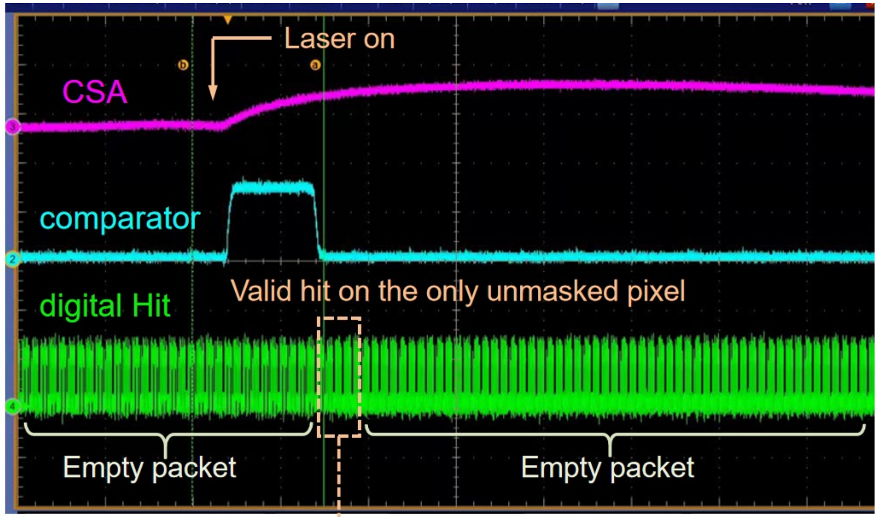

Architecture 2:

NMOS-only in-pixel digital design: lower power consumption in pixel; no process modification needed

# First COFFEE3 results

- Preliminary tests show that both readout array function well
- Standalone modules meet design goal: PLL, LVDS, DLL

*Yang Zhou's talk*

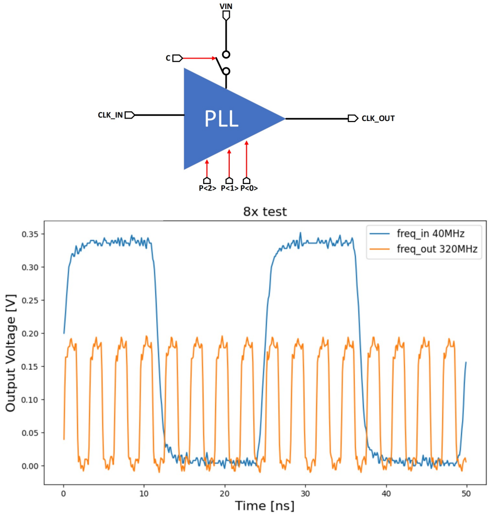



| 4 bit | 4 bit | 8 bit | 8 bit | 6 bit | 2 bit | 7 bit | 3 bit |
|---|---|---|---|---|---|---|---|
| header | CHIP_TS | LE_coarse | TE_coarse | LE_fine | TE_fine | Addr_Row | Add_Col |
| 0 1 1 0 | 0 1 0 1 | 0 0 0 1 0 1 1 0 | 0 1 1 0 1 0 1 1 | 1 1 0 0 0 0 | 0 0 | 0 0 0 0 0 0 1 | 0 0 0 |

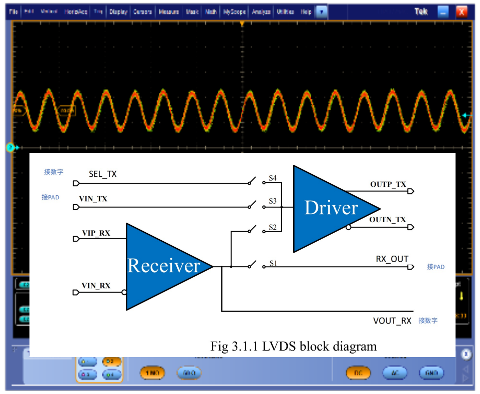
A valid transmission packet corresponding to a hit

Correct row & column address

Laser signal on a single pixel corrected read




Phase Lock Loop works up to 640MHz




LVDS tranceiver works at 640MHz


DLL delays main clock to achieve finer timing

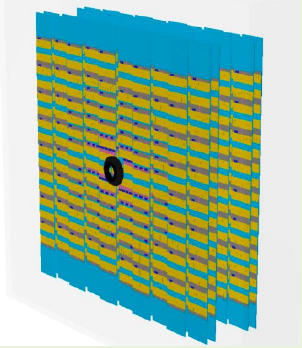
# Future plans for sensor R&D

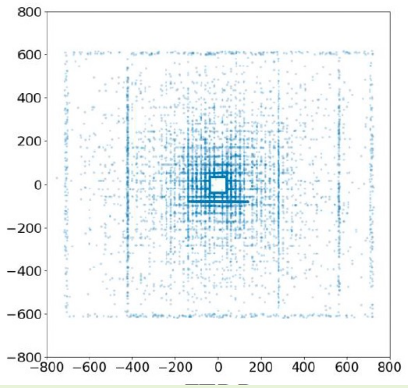
- Finalization of the specifications
- Full characterization of available chips
  - Especially on the radiation tolerance to the level of UP operation
  - Validation of the key performance
- Modification of process for better performance
  - Using high-resistivity wafers for higher $V_{bd}$ and full depletion
  - Adding deep p-well isolation to allow use of CMOS in full swing
- Aiming at a full-size full-function chip submission by end 2027

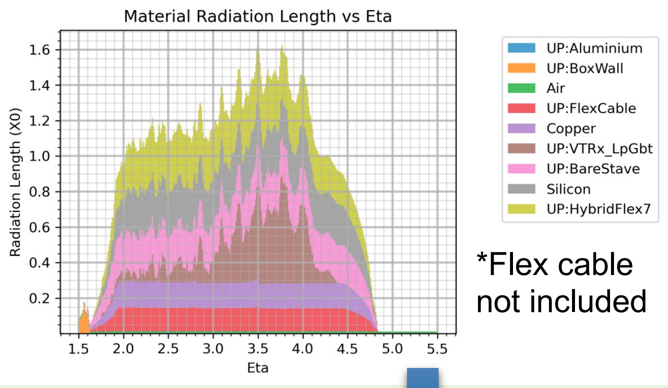
# Simulation and performance study

- New UP design implemented in LHCb official framework followed by tremendous work on tracking algorithm and detector optimisation

FTDR design





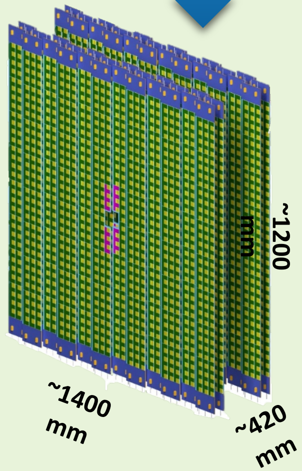


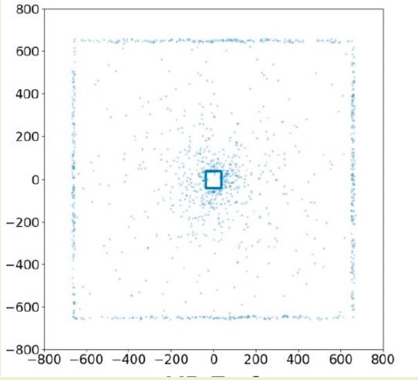

*Flex cable not included

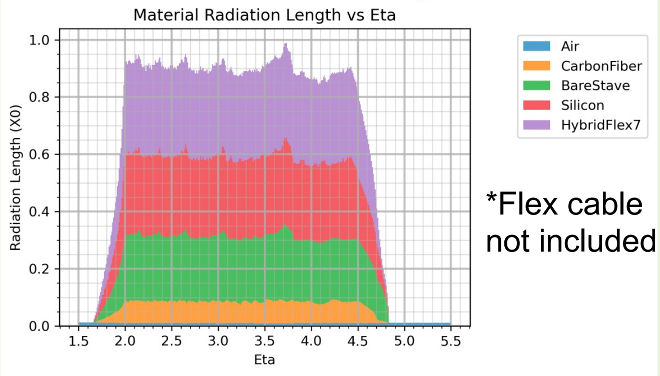
Less dead area

Less material

Gapless module design

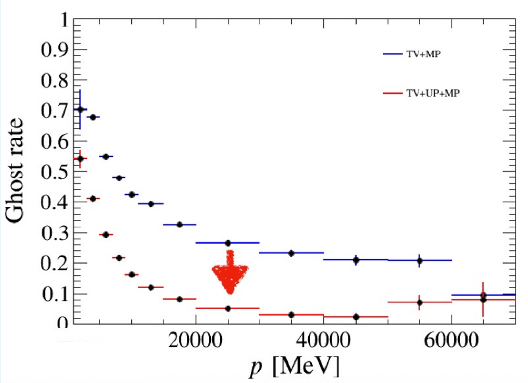


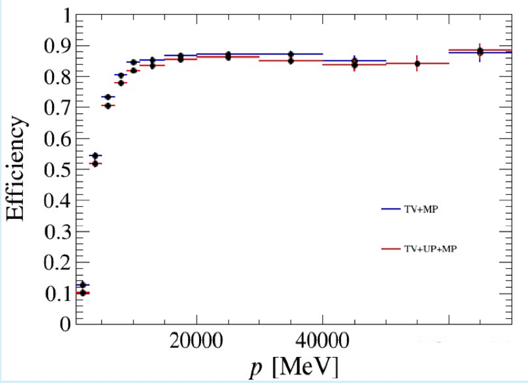






*Flex cable not included

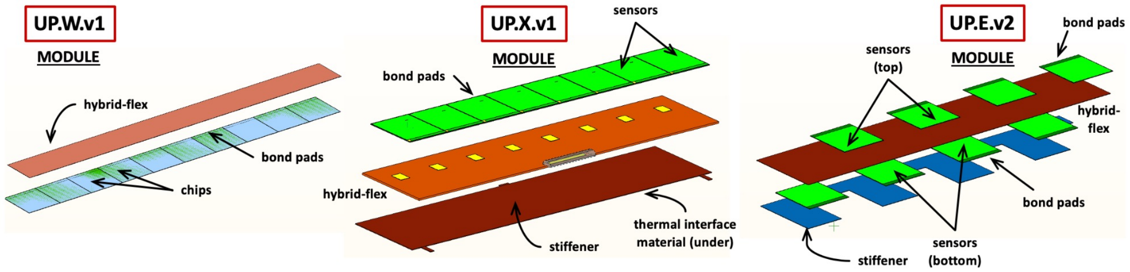
Adding UP in tracking indeed improves GR and efficiency!



# Concept design and prototyping

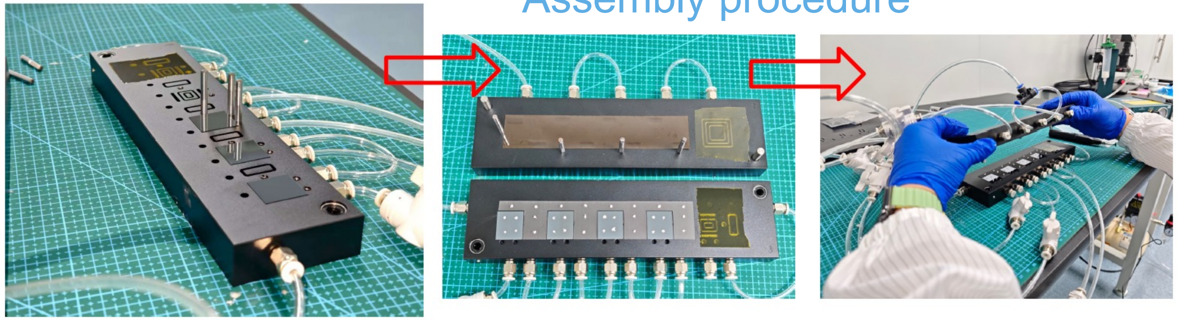
- Various design concepts for modules & staves
- First modules developed with dummy silicon sensors and dedicated tools

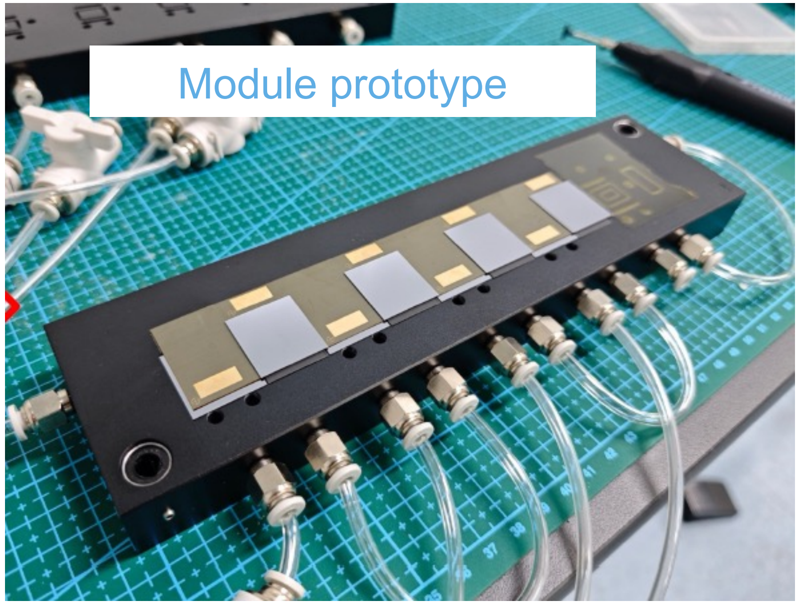



1st dummy sensor

1st dummy hybrid

Assembly procedure

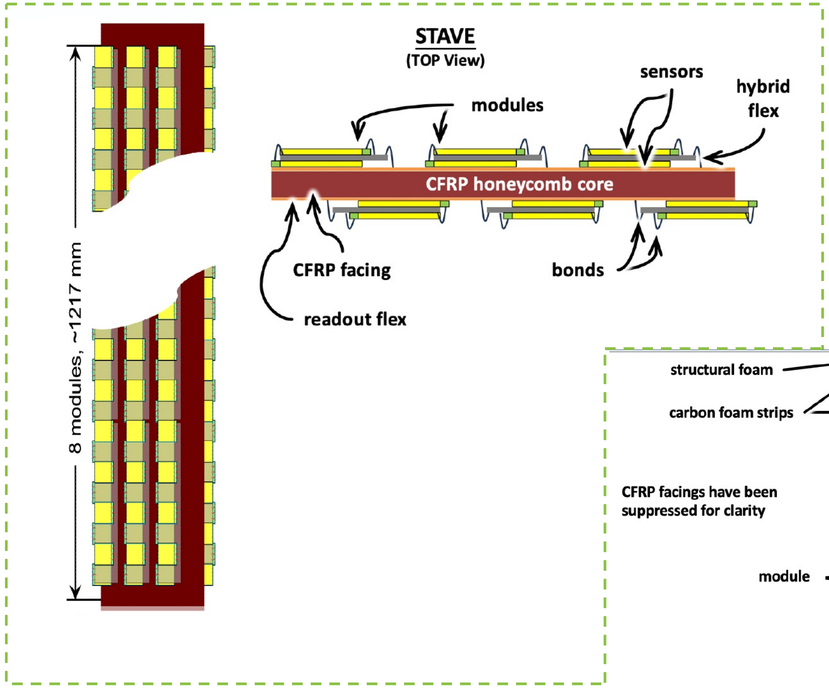


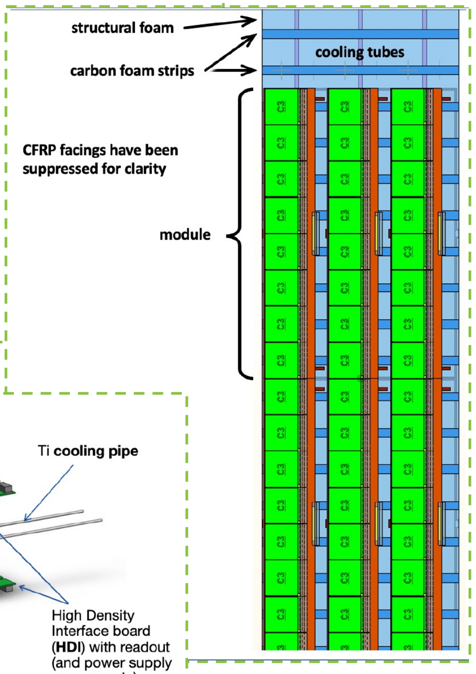


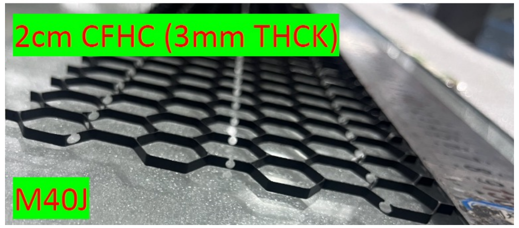
Module prototype

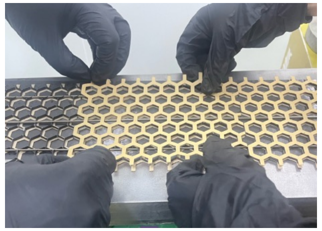
# Concept design and prototyping

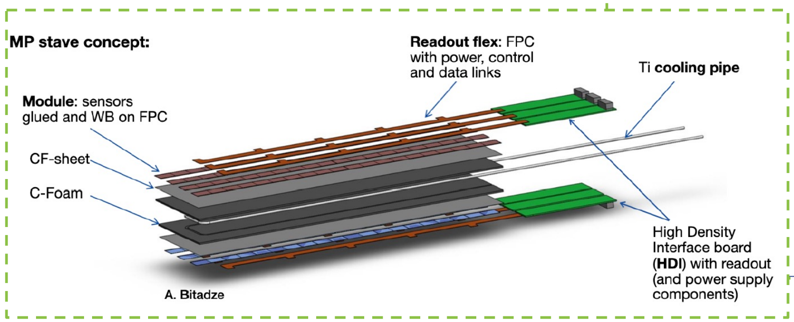
- Various design concepts for modules & staves
- First modules developed with dummy silicon sensors and dedicated tools
- Carbon fibre based bare stave produced with titanium cooling tube

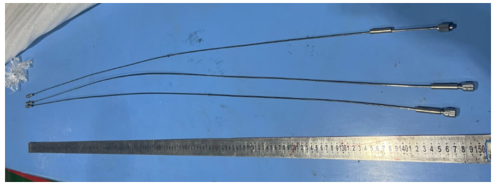


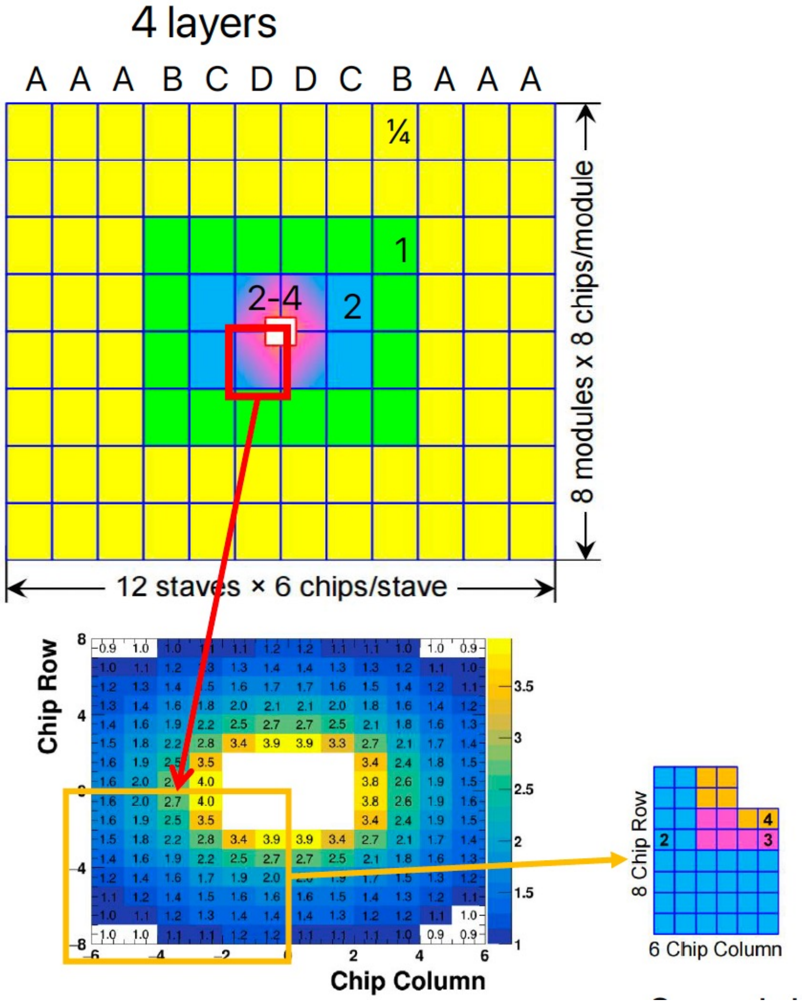





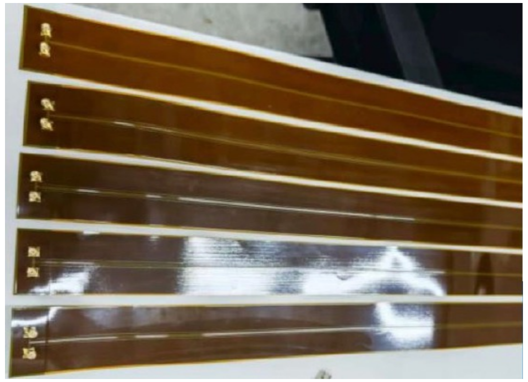



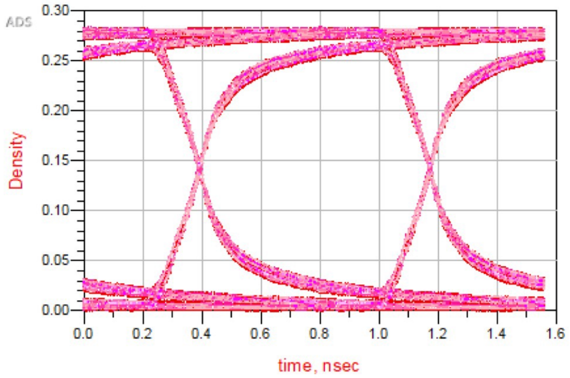
# Readout and electronics




Number of e-links needed per chip

- Common electronics as defined by LHCb
  - lpGBT, VTRx+…
  - TELL400, SOL400
- Still a lot to be studied and finalized
  - Optical conversion at end-of-stave: material budget for flex cables?
  - Serial powering vs. parallel powering?

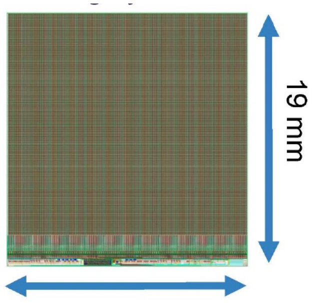




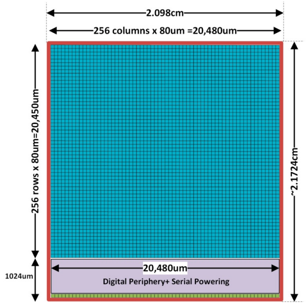

Flex cable prototypes ~70cm long

# Synergy with Mighty Tracker

- Inner part of Mighty Tracker also based on MAPS
- HVCMOS sensors under development
  - Specification sufficient to cover large area of UP except for the innermost region near beampipe
  - All sensor options form backup for each other

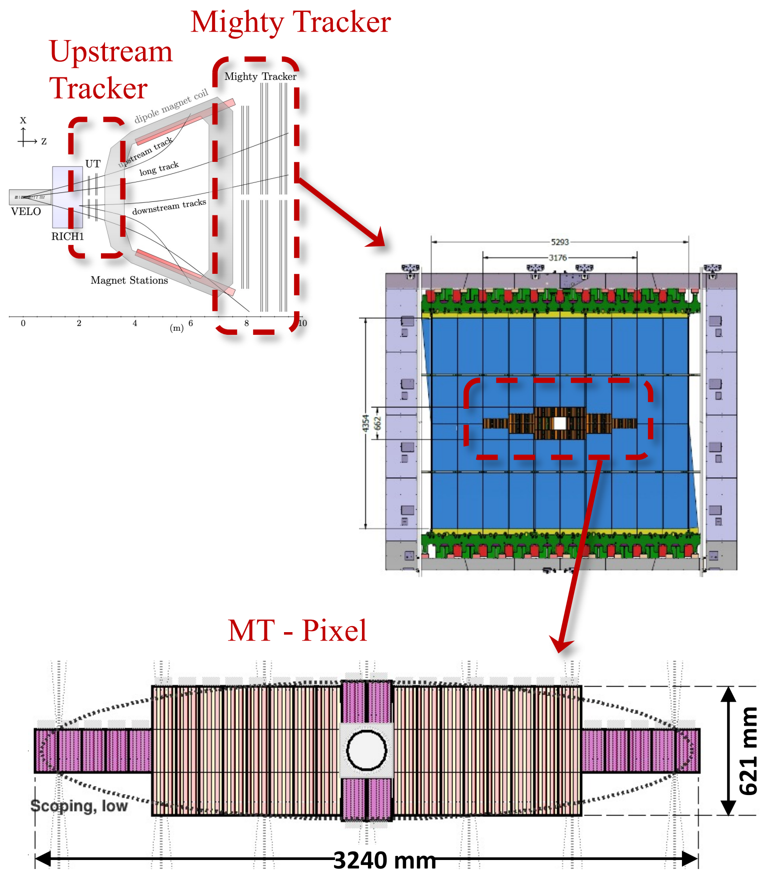



MightyPix
in AMS 180nm




RadPix
in LFoundry 150nm

- Joint tasks formed between UP and MT to define common components and share experiences & resources




*Tianqi Gao's talk*

# Summary

- MAPS-based Upstream Pixel tracker proposed for LHCb Upgrade II, and R&D active in the last couple of years
  - New sensor prototypes designed and produced
  - Detector concept design is optimized with support of simulation
  - Prototype of module and mechanical components started even without the final chip
  - Synergy being explored with Mighty Tracker
- Upgrade II tracker TDR is expected next year
  - A lot of development work ongoing
  - Your interest and participation welcome