Design and development of MAPS-based CEPC Inner Tracker

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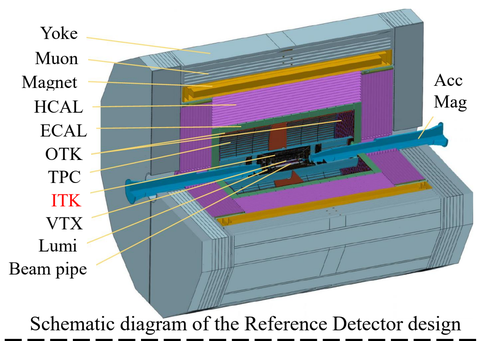
1. Abstract

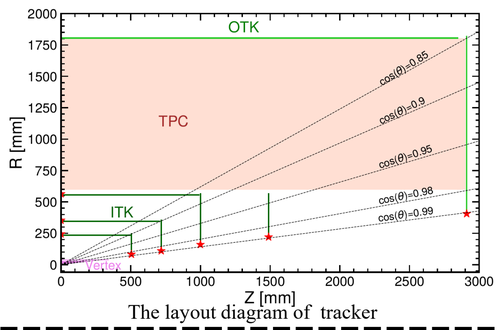
The Circular Electron Positron Collider (CEPC) is a next-generation electron positron collider for precision studies of Higgs, flavor physics and beyond. A key component of its tracking system is the Inner Tracker (ITK) using High Voltage Complementary Metal-Oxide-Semiconductor (HV-CMOS) sensor technology. We will introduce the design of the CEPC ITK, which consists of three barrel layers and four pairs of endcap disks, covering a total active area of about 20 m^2. The HV-CMOS sensor fabricated with advanced 55 nm process is used to achieve a few-micrometer spatial resolution and a few-nanosecond timing resolution, with a moderate power consumption. The design of modules is shared between barrel and endcap to facilitate production. The whole system is designed for minimal material budget, with ~0.7% X0 per layer in the barrel part. The design has been implemented in CEPC software framework for performance study and future optimization.

2. Introduction

- The tracking system is composed of the Vertex Detector (VTX) and the Inner Silicon Tracker (ITK), the Time Projection Chamber (TPC) and the Outer Silicon Tracker (OTK), as shown below. More details about the CEPC tracking system can be found in its Technical Design Report of Reference Detector (Ref-TDR) at arXiv:2510.05260
- The HV-CMOS ITK is a key subsystem. Its baseline design consists of three barrel layers and four endcap layers positioned between the VTX and the TPC
- The overall track momentum resolution requirement: ~0.1% for momenta below 100 GeV/c



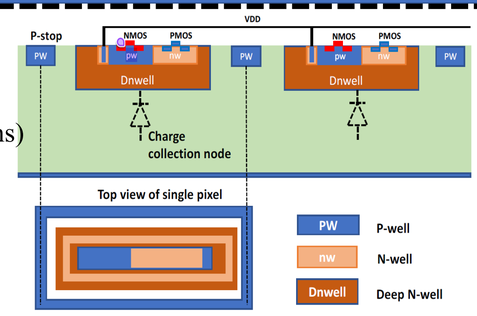
Schematic diagram of the Reference Detector design



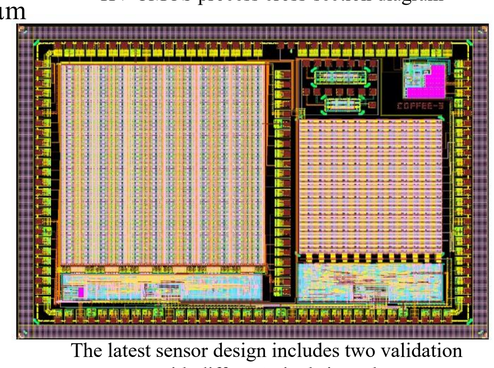
The layout diagram of tracker

3. Sensor for ITK

- The cost effective monolithic HV-CMOS sensor:
  - Large collection electrode
  - Large depletion, radiation hard
  - Sufficient timing resolution for accurate bunch tagging (23 ns)
  - Low material (~0.16% X0)
- The 55 nm process HV-CMOS sensor key specifications:
  - Sensor size: 2 cm × 2 cm (active area: 1.74 cm × 1.92 cm)
  - Sensor thickness: 150 μm
  - Array size: 512 × 128
  - Pixel size: 34 μm × 150 μm, spatial resolution: 8 μm × 40 μm
  - Time resolution: 3 - 5 ns
  - Power consumption: 200 mW/cm^2
- Two small prototypes (COFFEE2 and COFFEE3) have been designed and produced, for validation of the process and the readout architectures, respectively. A full-size fully functioning sensor chip is planed for submitted by end of 2027
- More details can be found in:
  - NIM A1069(2024) 169905
  - JINST 20 (2025) C10011



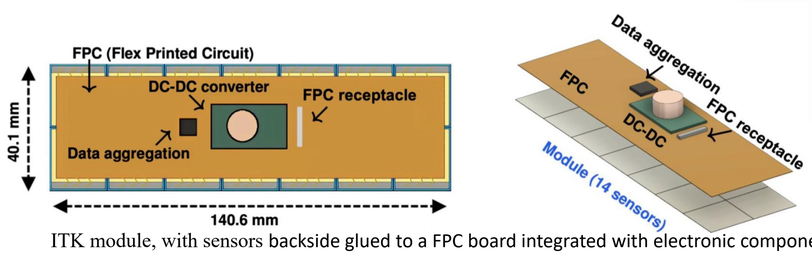
HV-CMOS process cross-section diagram



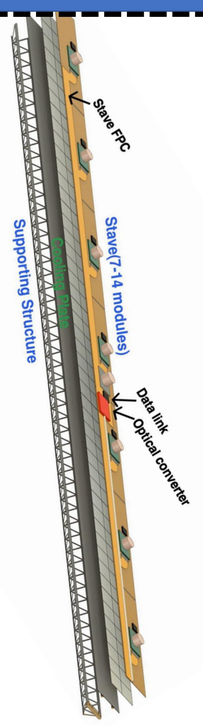
The latest sensor design includes two validation areas with different pixel size schemes

4. The Design of ITK Module and Stave

- The standard module:
  - 14 sensors (2 rows × 7 columns)
  - Module dimensions: 140.6 mm × 40.1 mm
  - Sensors electrically connected to Flexible Printed Circuit (FPC) via wire bonds
  - FPC carries power, data, clock and chip commands signal
  - Direct Current-Direct Current (DC-DC) converter and data aggregation chip



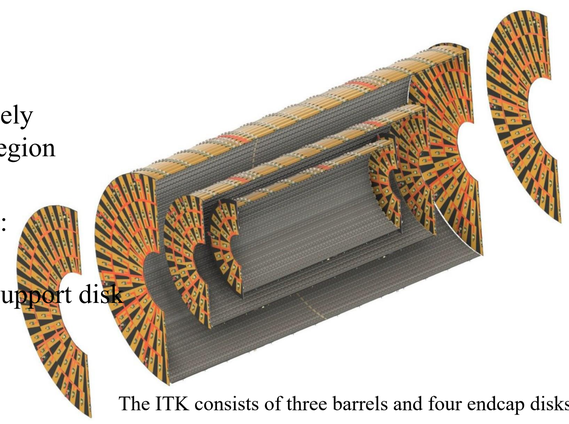
ITK module, with sensors backside glued to a FPC board integrated with electronic components



- Stave:
  - 7, 10 or 14 modules, with lengths of 986.6 mm, 1,409.6 mm, and 1,973.2 mm
  - One or two long FPCs per stave
  - FPC Center Components: a data link chip, an optical converter and DC-DC per FPC
  - A carbon fiber plate with embedded polyimide cooling tubes
  - A carbon fiber truss frame provides mechanical support
  - A graphite foil layer and two carbon fleece layer

5.The Design of ITK Barrel and Endcap

- The ITK layout was optimized through analytic calculations and simulations
  - Details in poster: Tracker optimization for the Fourth Detector Concept of CEPC, Jiang et al., CEPC Workshop 2023
- Staves constitute the three ITK barrels:
  - Barrel radii: 235.0 mm, 345.0 mm, and 555.6 mm
  - 44, 64, and 102 staves for the three barrels, respectively
  - Mounted in a staggered structure to minimize dead region
  - Integrate 33264 sensor chips
- Four ITK endcap disks (ITKE1, ITKE2, ITKE3, ITKE4):
  - 3 types of modules: 8, 12, and 14 sensors
  - Modules in both sides of a carbon fiber honeycomb support disk
  - 81.5 mm < r < 242.5 mm (ITKE1),
    110.5 mm < r <352.3 mm (ITKE2),
    163 mm < r < 564 mm (ITKE3),
    223 mm< r < 564 mm (ITKE4)
  - 13760 sensors
- The ITK detector geometry is implemented in CEPCSW for simulation



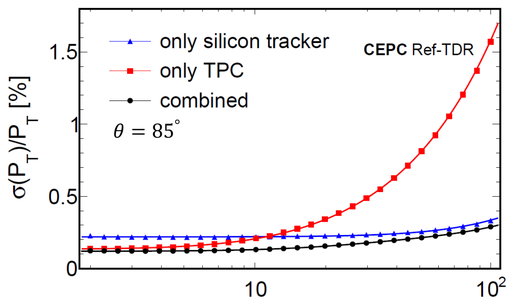
The ITK consists of three barrels and four endcap disks

6. Performance

- The tracker momenta resolution:
  - The total momenta resolution mainly determined by intrinsic spatial resolution and multiple scattering. At a given polar angle θ in the barrel, we have:

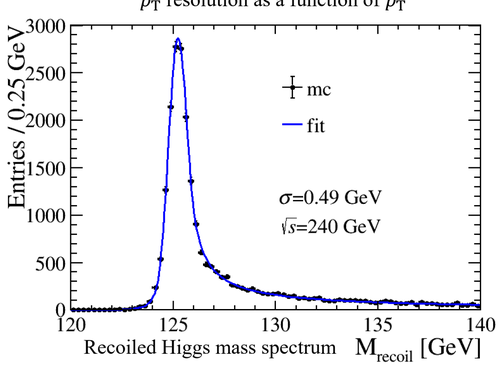
$$\frac{\sigma_{P_T}}{p_T} = aP_T \oplus \frac{b}{\beta\sqrt{\sin\theta}}$$

  - where a = 2.1 × 10^{-5}, b = 2.2 × 10^{-3}
  - At high momenta, the silicon tracker significantly improves the momentum resolution, and the combined momenta resolution is about 0.1% from the simulation

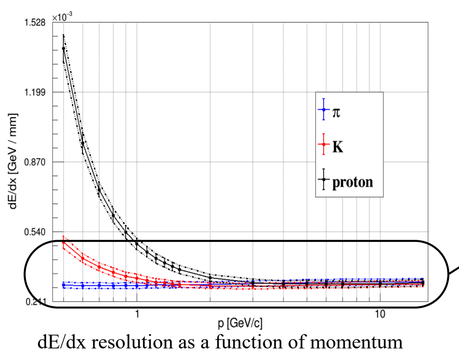


p_T resolution as a function of p_T

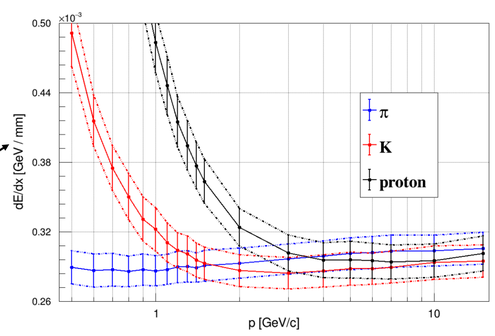
- Performance of recoiled Higgs reconstruction in CEPCSW:
  - Physics progress: e^+e^- → ZH (μμγγ) with √s = 240 GeV
  - Consider the energy spread effect
  - The Higgs mass resolution: 0.39%



- PID capacity of non-baseline ITK endcap in CEPCSW:
  - 4 double-layers ITKE, 200 μm silicon sensor
  - PID resolution extraction from a Crystal Ball fit to the dE/dx distribution
  - PID capability for charged hadrons separation below 2 GeV

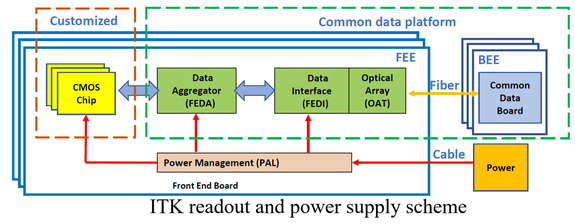


dE/dx resolution as a function of momentum



7. Hit Rate Study

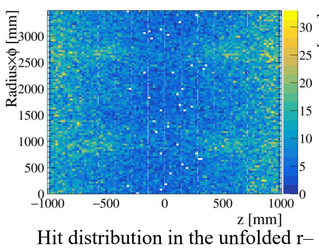
- Data transmission rate:
  - Module 86.67 Mbps ×14 → FEDA 1.39 Gbps → FEDI 11.09 Gbps
- A full simulation was performed to evaluate the beam-induced background hit rate under various operating modes, ensuring the safety of the readout system:



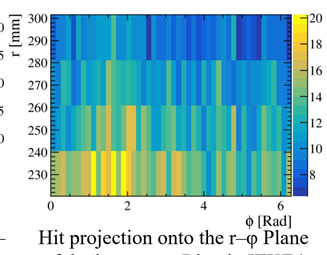
ITK readout and power supply scheme

Estimated average and maximum hit rates of the ITK (safety factor 2 applied) [10^3 Hz/cm^2]

$\mathcal{L}$ (10^{34} $cm^{-2}s^{-1}$)	Low Lumi. Z 26		Higgs 8.3		High Lumi. Z 192	
	Average	Max	Average	Max	Average	Max
ITKB1	2.0	3.9	1.2	2.0	6.2	11.7
ITKB2	2.0	6.6	1.1	2.6	5.9	19.8
ITKB3	1.5	3.4	0.8	1.5	4.5	10.1
ITKE1	6.9	31.6	4.7	23.4	20.7	94.6
ITKE2	8.0	49.0	4.1	19.6	23.9	146.8
ITKE3	4.6	34.5	2.2	14.9	13.7	103.4
ITKE4	5.1	17.1	2.5	7.4	15.2	51.2



Hit distribution in the unfolded r–z plane of ITKB3 (Higgs Mode)



Hit projection onto the r–φ Plane of the innermost Ring in ITKE4 (Higgs Mode))

8. Summary and Future Plan

- The Inner Tracker R&D has been included in the Ref-TDR
- Scaling up HV-CMOS sensor production and completing the development of integrated modules and systems
- Detailed testing of the latest sensor version, which features a data-driven readout with in pixel Coarse-Fine TDCs
- Advancing prototype detectors, with the goal of transitioning to an engineering-ready system within the next few years
- Continuous innovations in sensor technology, readout electronics, mechanical design, and the development of the cooling system to ensure that the ITK meets the high demanding requirements of CEPC physics