Characterization and Simulation for CASSIA: A CMOS Pixel Sensor with Internal Amplification

J. Lunde[1], E. K. Anderson[1], P. Bartulović[2], J. Baudot[3], I. Berdalović[2], A. Dorokhov[3], S. Haberl[1], M. Jugović[2], A. Kotsokechagia[1], H. Pernegger[1], B. Požar[2], H. Shamas[3], and T. Suligoj[2]

[1]CERN, Geneva, Switzerland
[2]University of Zagreb, Faculty of Electrical Engineering and Computing, Zagreb, Croatia
[2]IPHC, University of Strasbourg, Faculty of Physics and Engineering, Strasbourg, France

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Future high-energy physics experiments require trackers with improved timing and spatial resolution, combined with a low material budget. The CASSIA (CMOS Active Sensor with Internal Amplification) project addresses these requirements by developing a monolithic pixel detector with internal amplification through the implementation of gain layers in an industrial 180nm CMOS imaging process.

The first prototype, CASSIA1, includes four 3×3 pixel matrices and 24 single-pixel structures without on-chip readout, enabling systematic studies of how geometrical parameters and variations in gain layer and electrode implantation profiles affect characteristics like sensor gain, breakdown voltage and dark count rate. The sensor can successfully be operated in LGAD mode as well as SPAD mode, allowing to target different HEP applications of the same sensor design.

CASSIA1 has been extensively characterized at regulated temperature in a climate chamber, and laser pulse measurements have been conducted to study the photo response. Sensor measurements and TCAD simulations are in good agreement and both are used to improve the design of the second prototype, CASSIA2. CASSIA2 will feature larger matrices with digital readout and analog readout, as well as multiple smaller test structures.

First results from CASSIA1 will be shown, which demonstrate the excellent performance of the first prototype sensor in terms of dark count rate, pulse amplitude, and operational range for LGAD mode and SPAD mode depending on sensor geometry and implantation profiles. The design of CASSIA2 will be introduced in the presentation, which aims at full fill factor while maintaining low dark count rate and integrating both analog and digital readout.