CASSIA = CMOS Active SenSor with Internal Amplification

A CMOS sensor with internal gain

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HSTD-14

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DRD3

Outline

- Introduction - What is CASSIA?
  - CASSIA1 design variants
- Simulation and measurements
  - TCAD IV simulations
  - First measurements
  - Pulsed laser measurement series
  - New measurements at Bonn and KEK
- CASSIA2
- Summary

The CASSIA project

- Aims to implement a pixel implant structure with **internal gain** in a **CMOS imaging process**
- To be used in MAPS for **tracking, timing or time-tagging**
- **Internal gain for:**
  - Much higher signal-to-noise in thin monolithic sensors (simplification of circuits)
  - Substantial improvement of time resolution for tracking sensors
  - Aim at limited gain in linear amplification range to keep noise rate low enough for HEP trackers

The CASSIA project

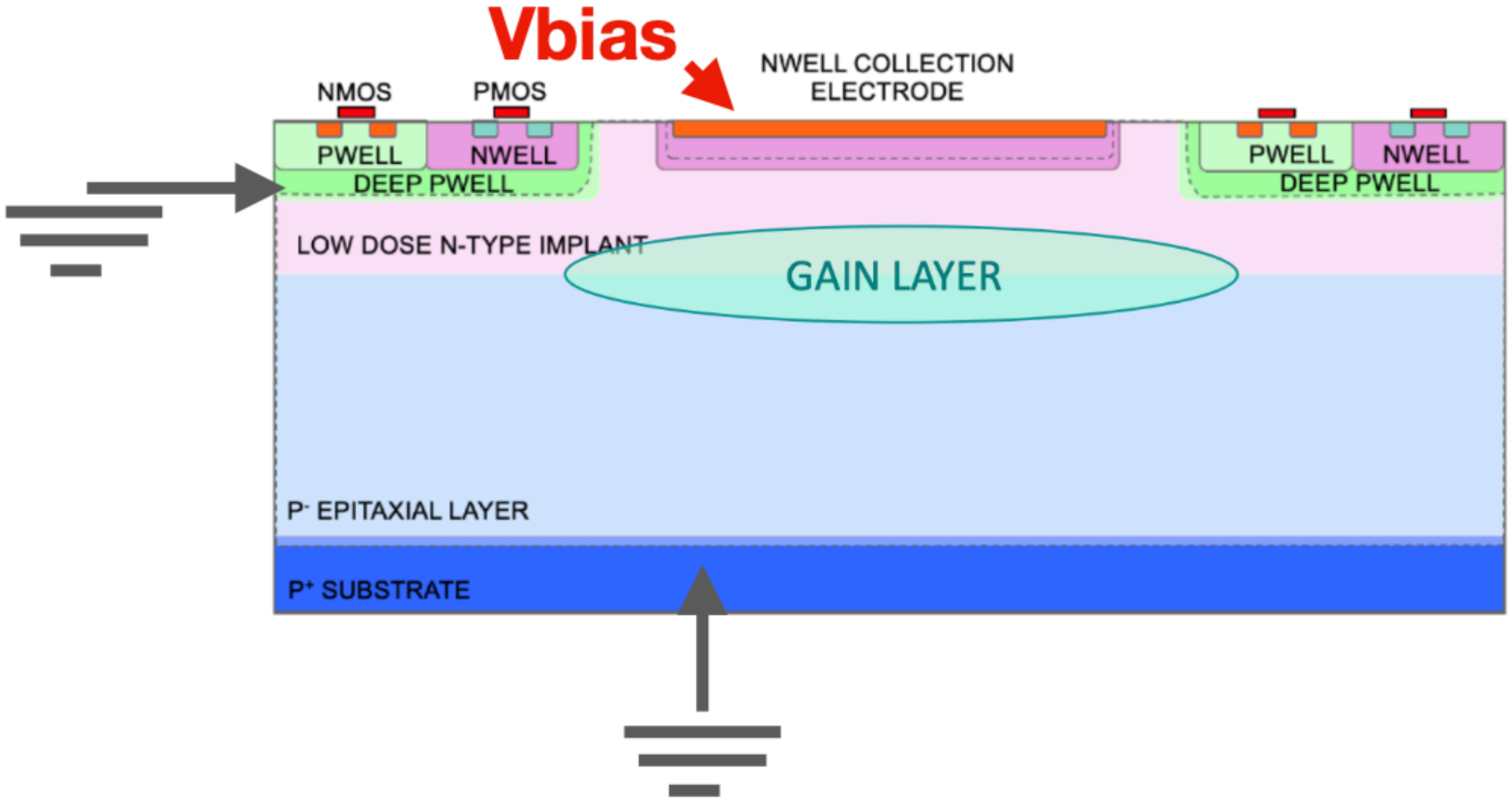
- **Done in Tower Jazz 180nm CIS imaging process,** on which many HEP sensors are based and we have substantial experience for tuning implant profiles

- A **transfer of results to finer-pitch processes** (e.g. 65nm) is envisaged for a future stage after initial developments in 180nm

CASSIA Sensor Design Variants

CASSIA1 design jointly by CERN and University Zagreb/FER

- Main focus : demonstrate that internal gain can be achieved in 180nm CIS with existing doping profiles
- Voltages necessary to achieve gain are within process capabilities
- Implemented low-gain avalanche (LGAD)/SPAD-type sensor in Tower 180nm CIS imaging process
  - Top biased electrode, substrate and PW on GND
  - Pixel pitch 80μm
- EPI and Cz substrate - focus on EPI in this talk



General design of the CASSIA sensors

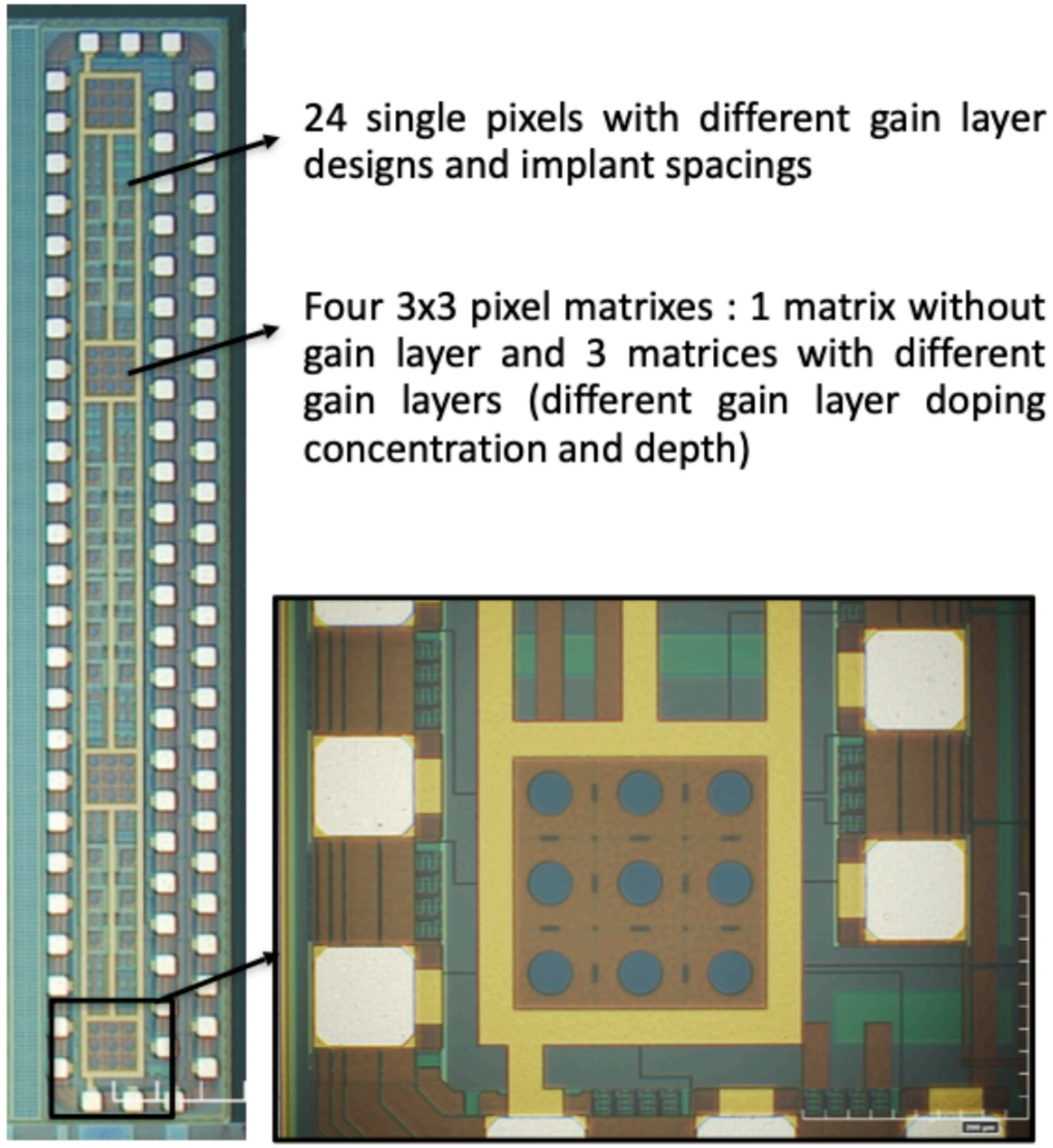
CASSIA Sensor Design Variants

Electrode and gain layer configurations:

A. No gain layer (reference)
B. NW electrode + p-type GL depth 1
C. NW electrode + p-type GL depth 2
D. Shallow electrode + p-type GL depth 2
E. Deep electrode + p-type GL depth 2

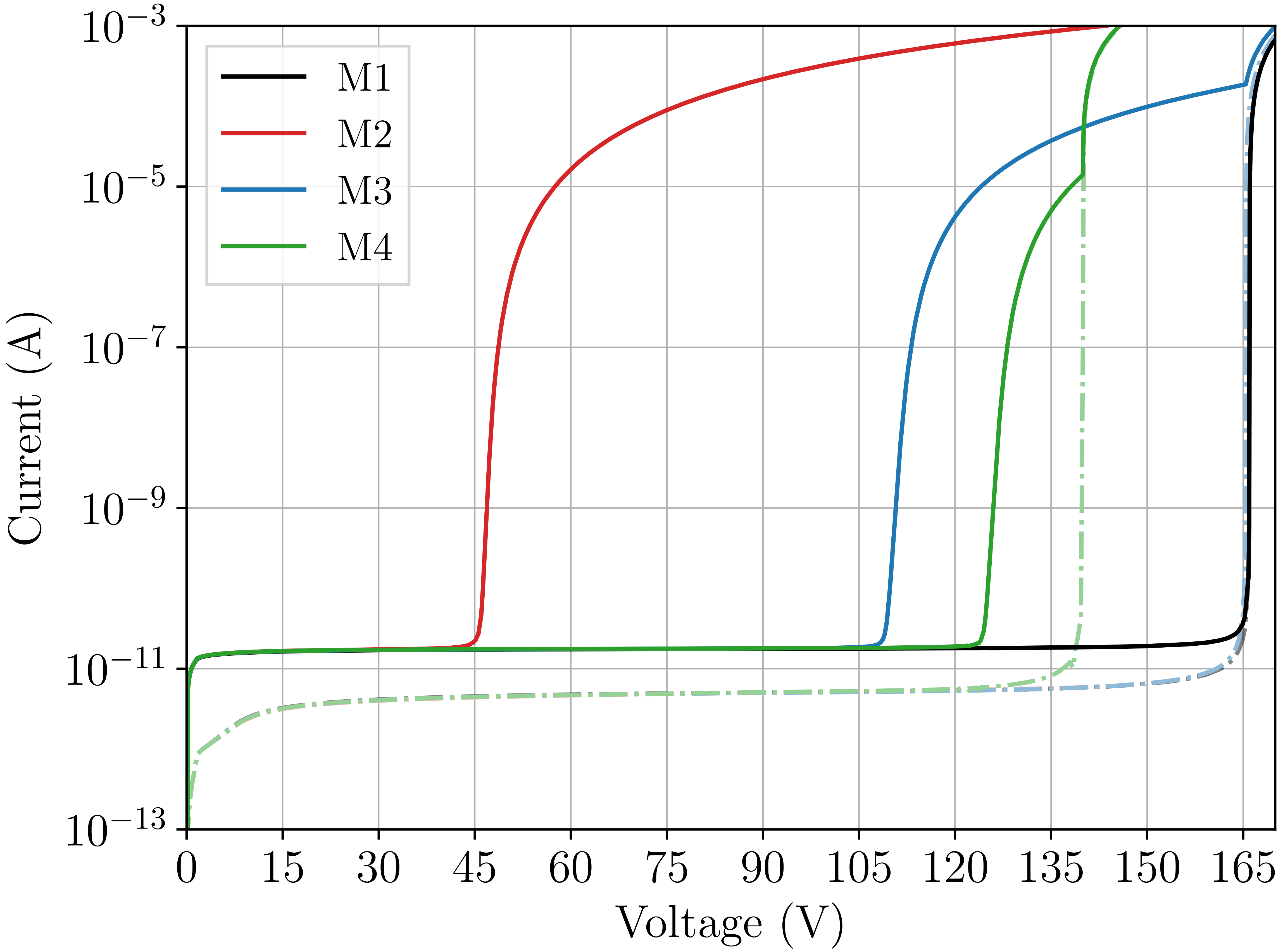
What we look for:

- Clear LGAD and SPAD region
- Low dark count rate
- High fill factor
- Breakdown to substrate (not PW)



TCAD simulations

- TCAD in 2D cylindrical
- Use Okuto-Crowell model for charge multiplication
- Bias electrode, substrate/PW on GND
- Solid line: Current through electrode
- Dashed line: Current through electronics p-well
- **All matrices with gain break down to substrate**



M1 : No gain layer. Break down to p-well at ~165V

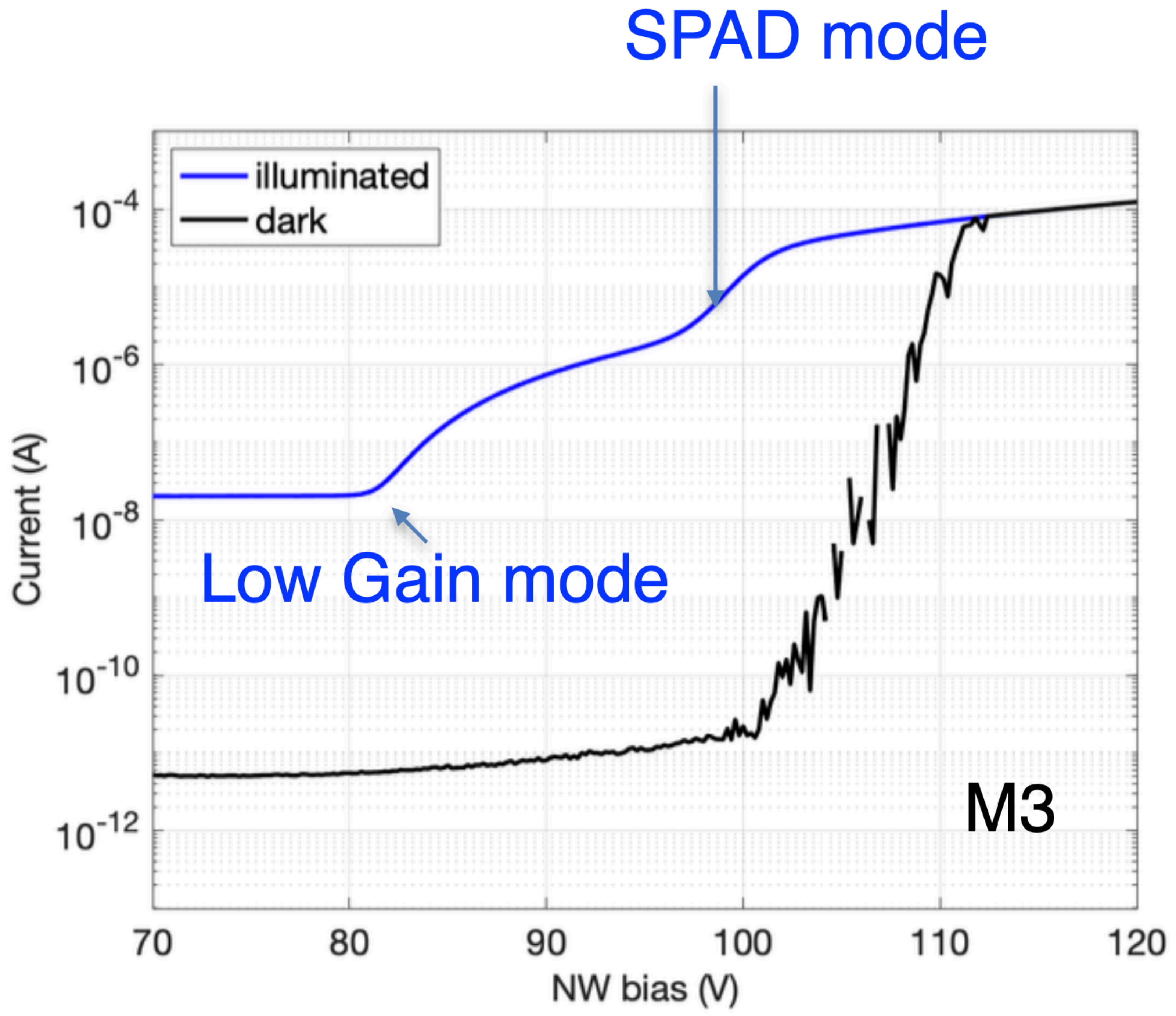
M2 : NW electrode + p-type GL depth 1. GL radius = 20µm

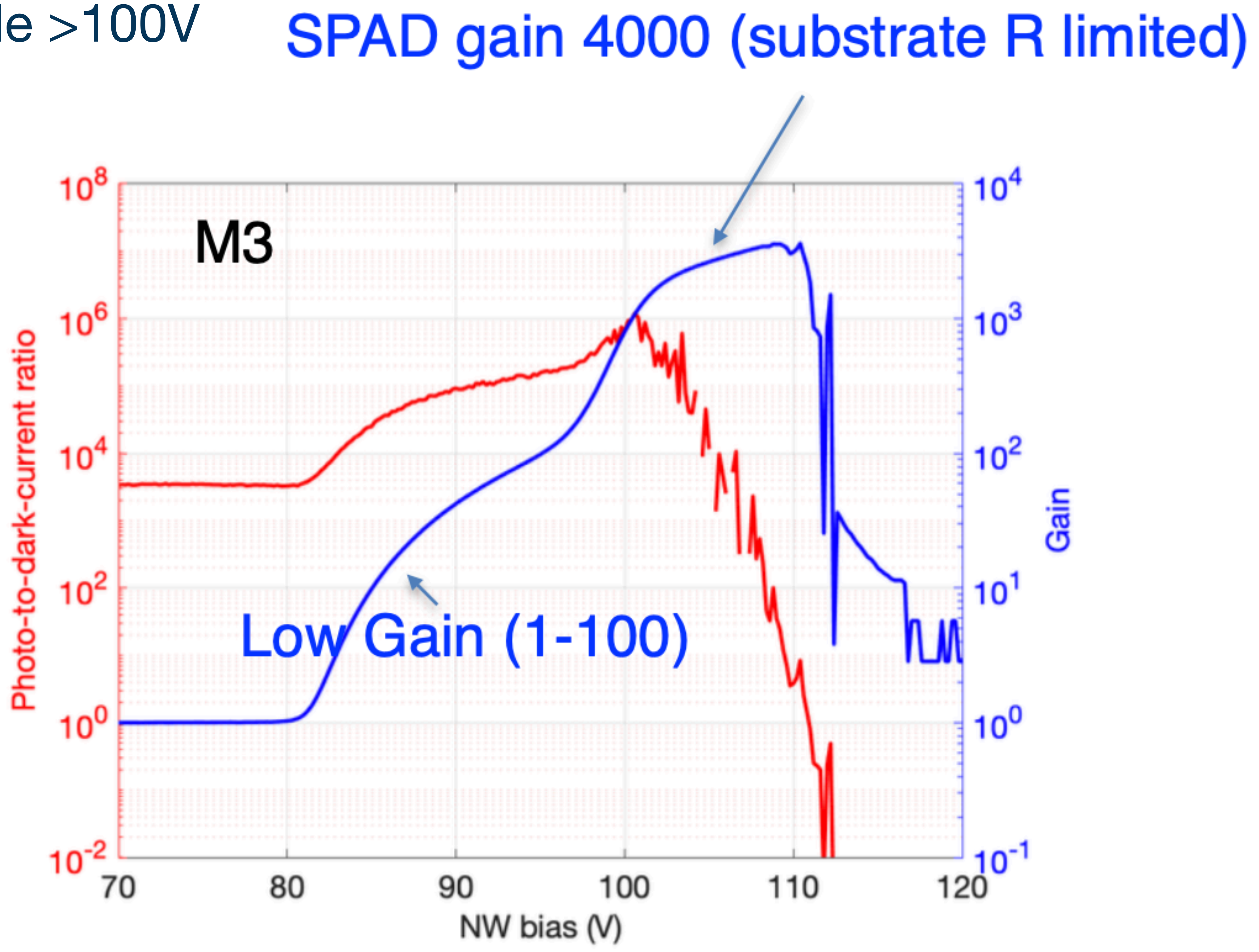
M3 : NW electrode + p-type GL depth 2. GL radius = 12µm

M4 : Shallow electrode + p-type GL depth 2. GL radius = 12µm

IV curves and gain: Dark and illuminated with visible light

- IV in dark and illuminated with visible light
- Design variation: NW electrode + p-type GL depth 2
- **Very well controlled gain modes** : LGAD mode 82V to 98V , SPAD mode >100V

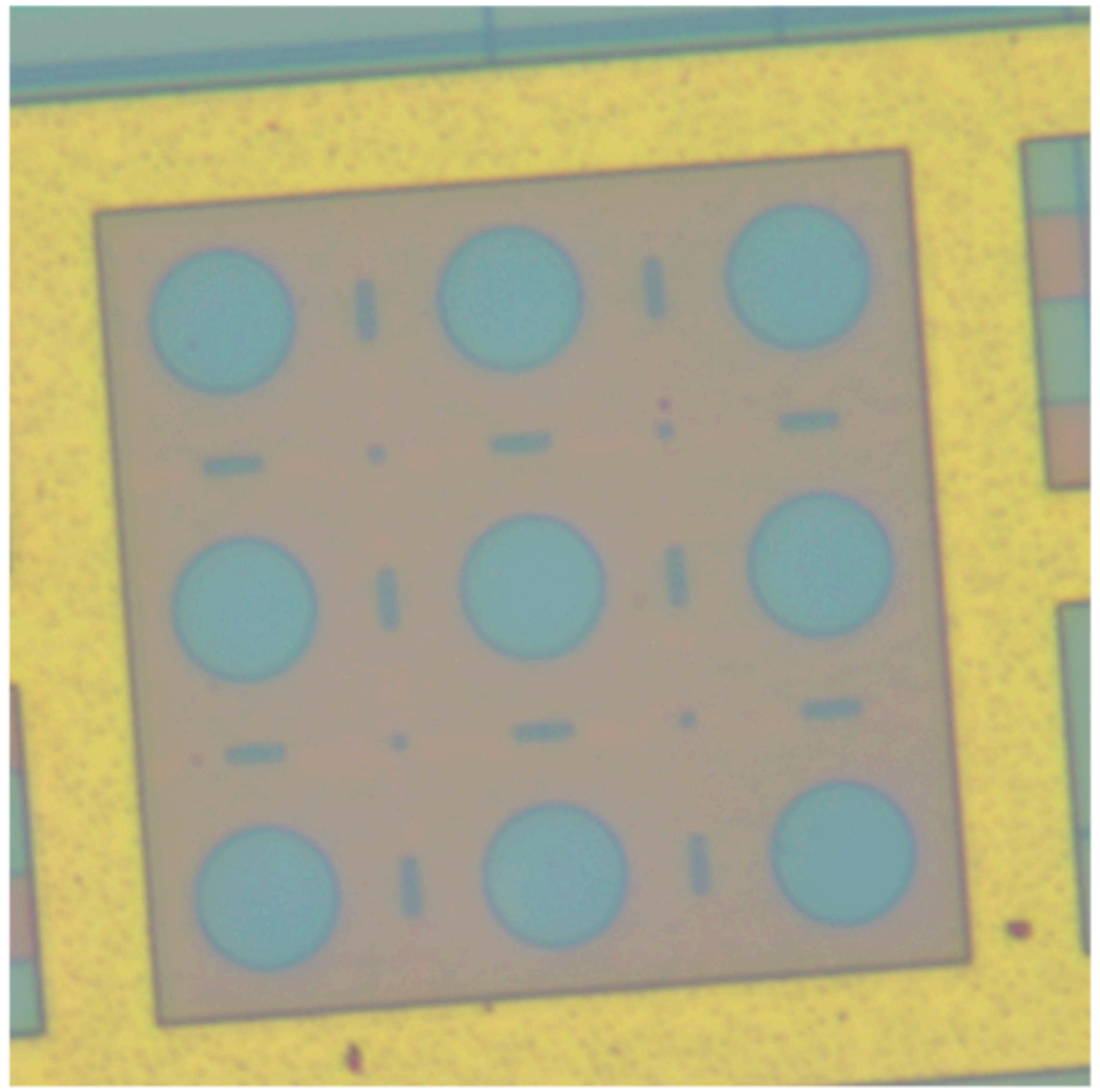




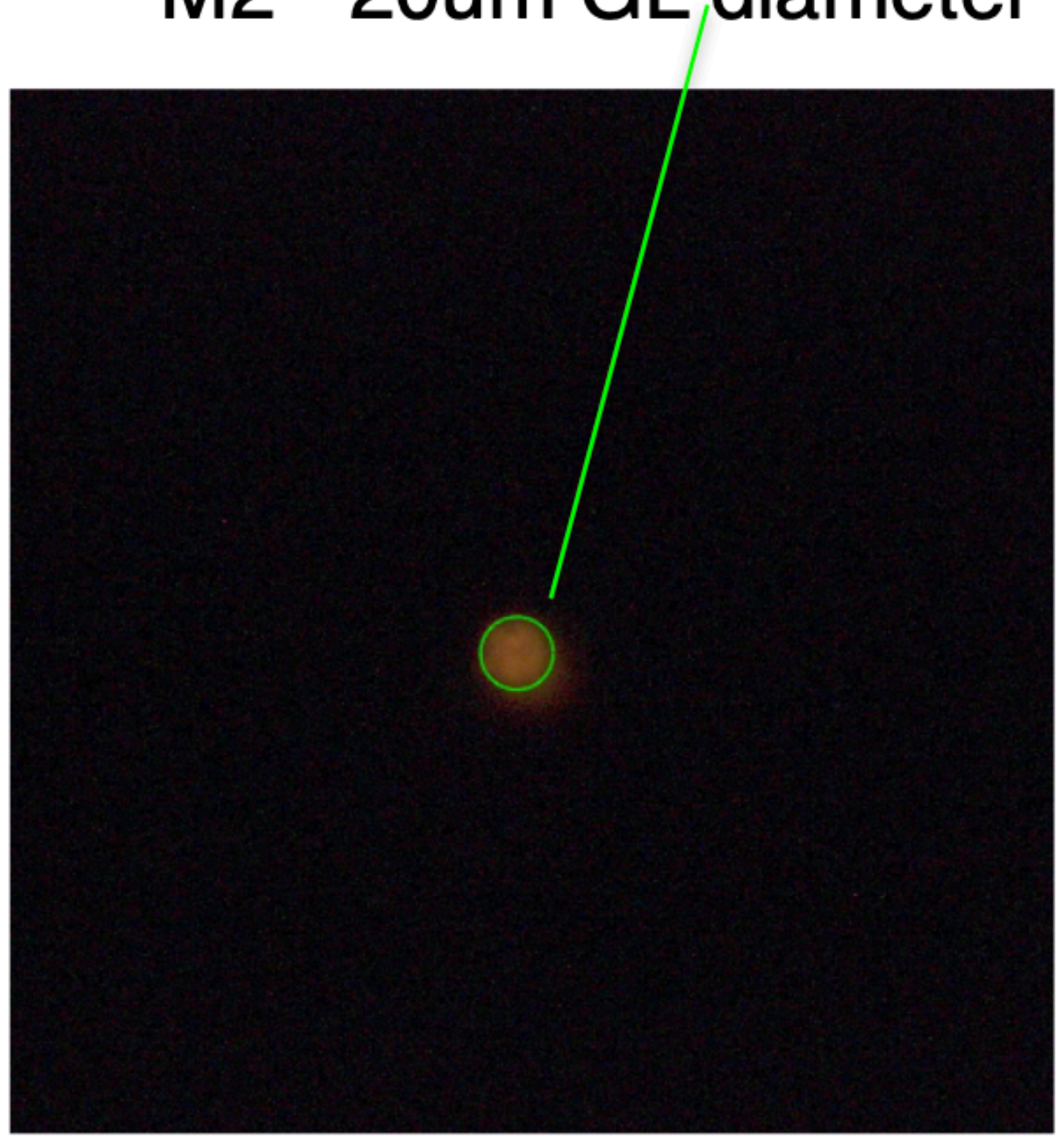
Light emission measurements

Break down in GL area or edge?

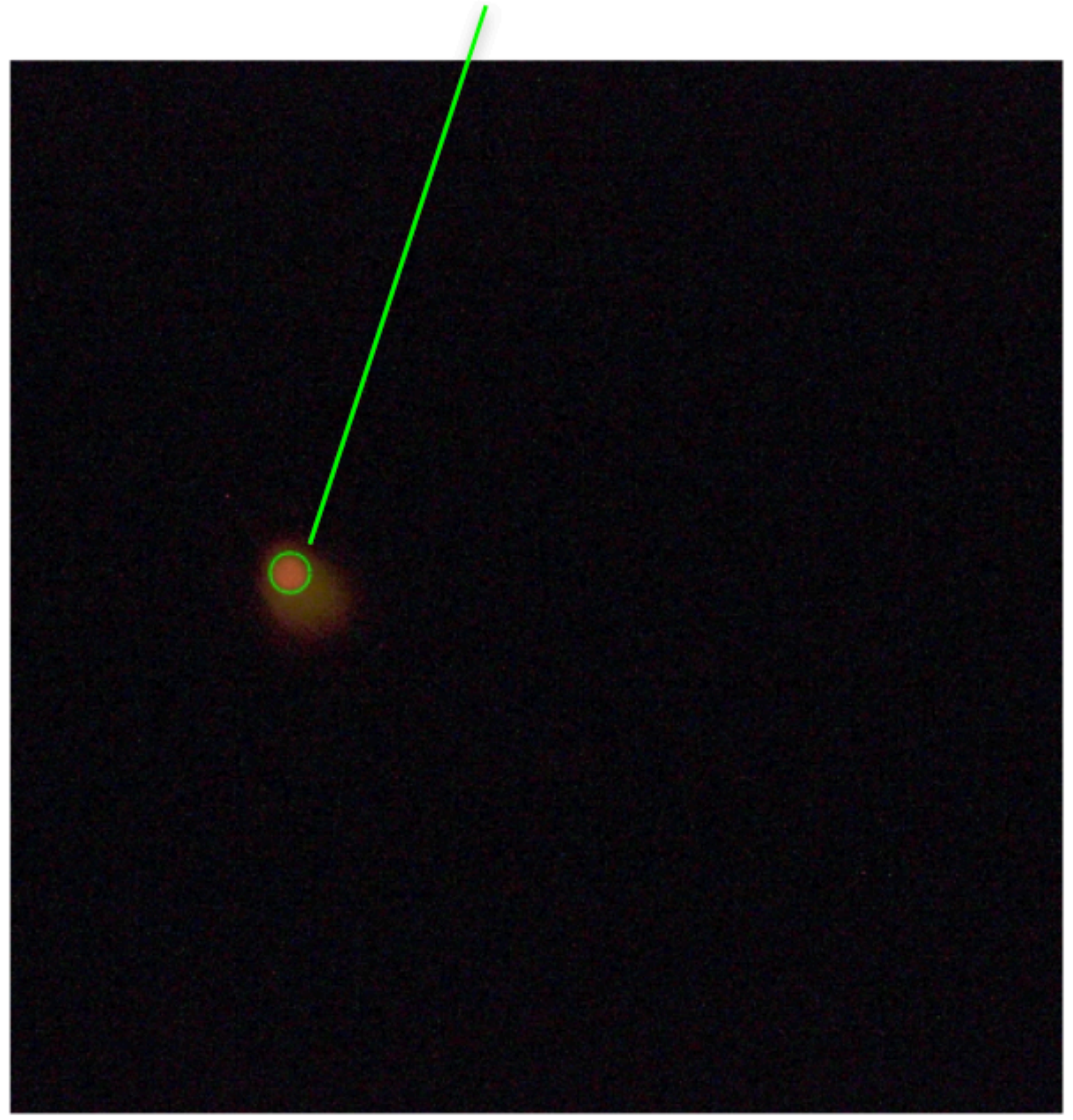
- Bias electrode above 100V (SPAD region) and record light emission
  - Light emitted uniformly across GL and spot size matches GL diameter



M2 - 20um GL diameter

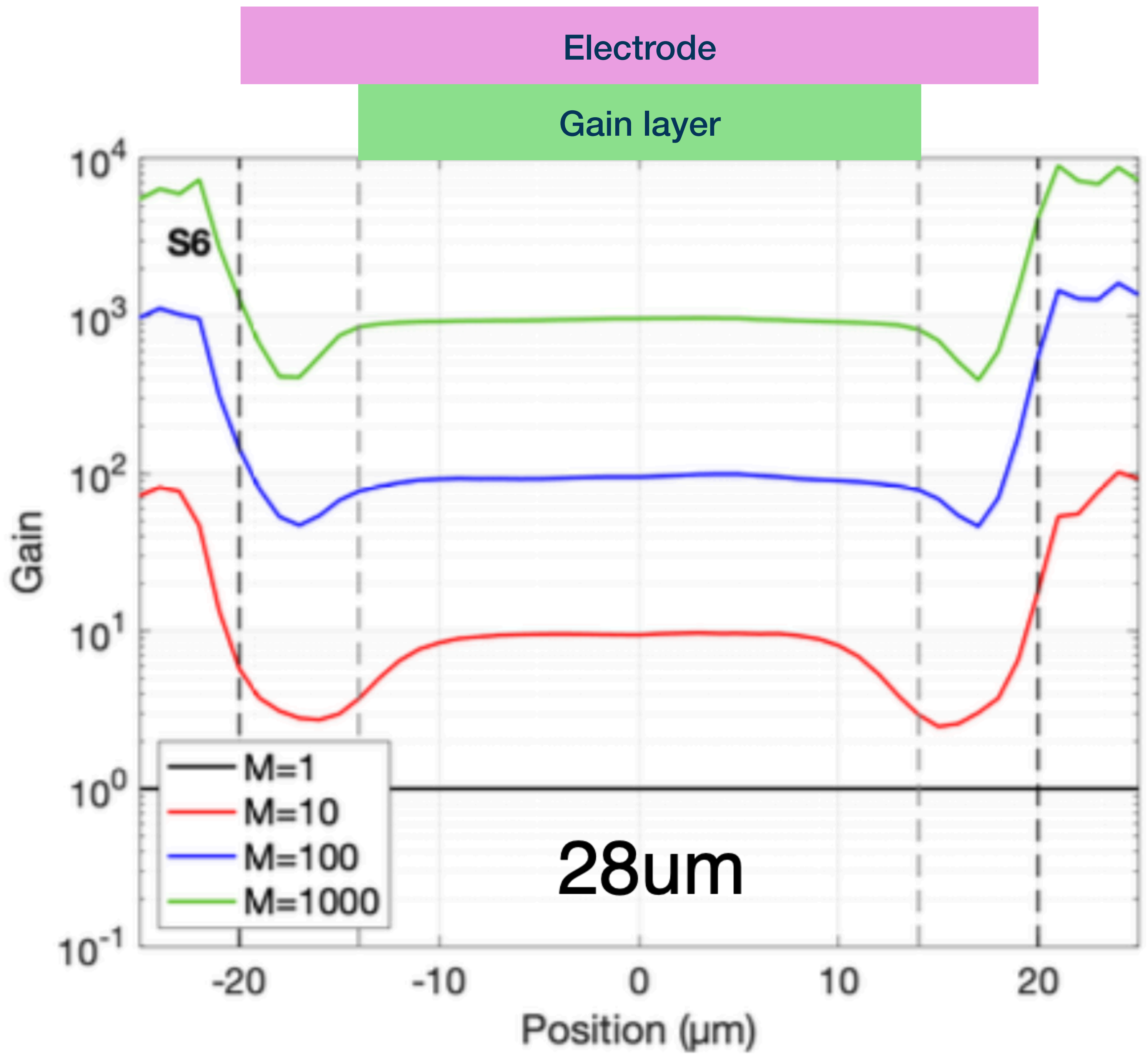


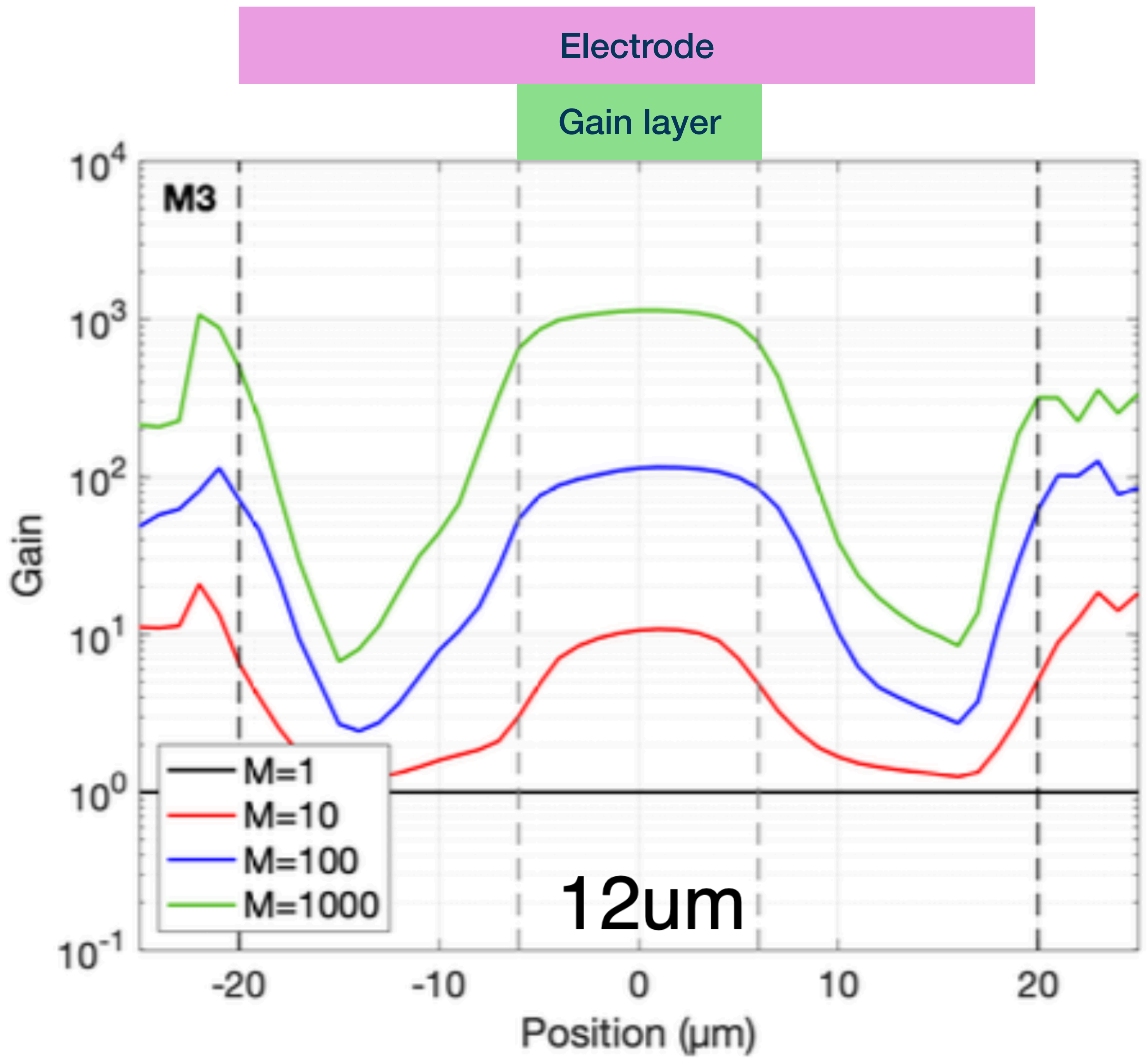
M3 - 12um GL diameter



Photocurrent and gain uniformity across pixel

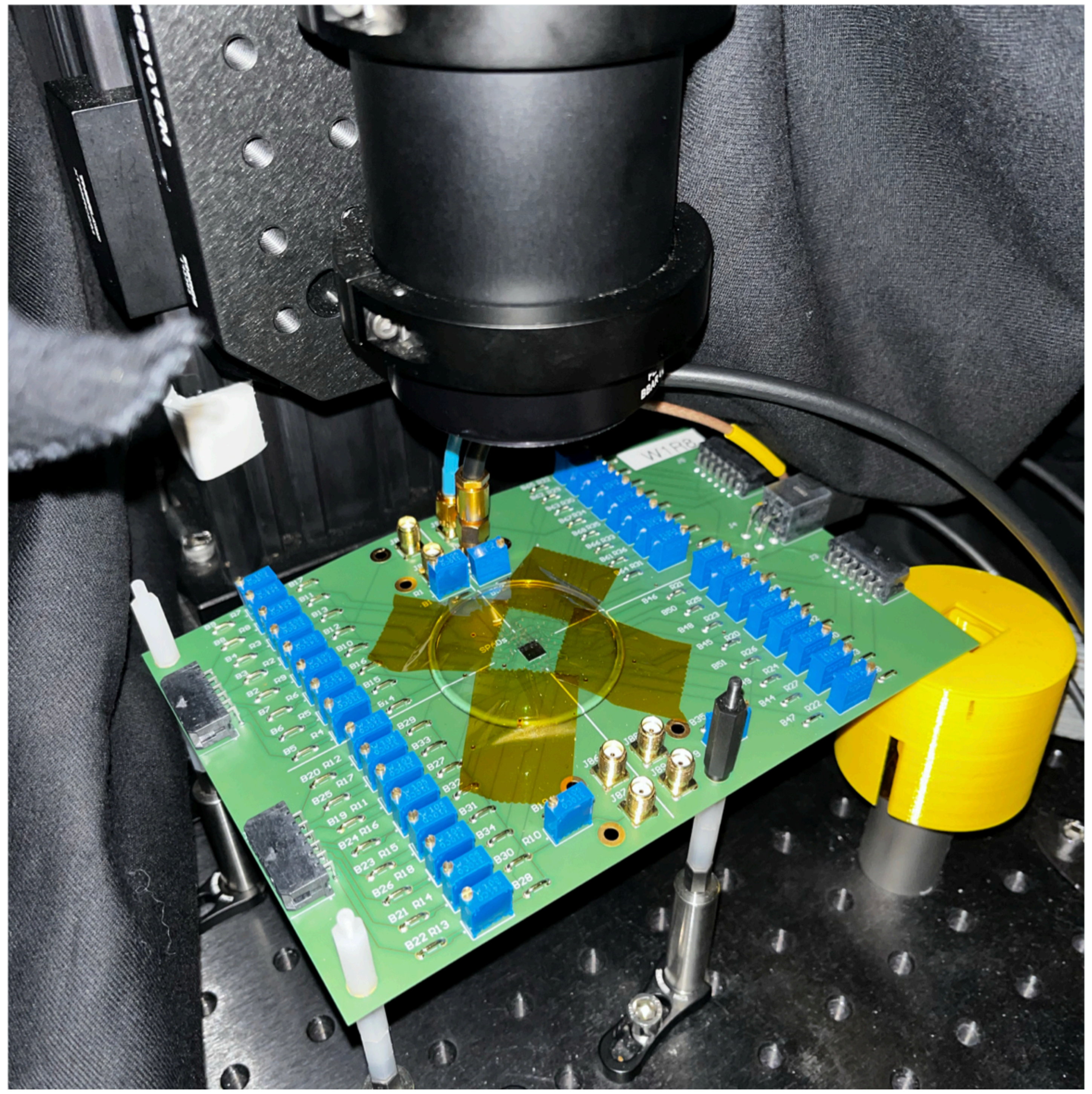
- Focused 2µm FWHM laser beam of 782nm
- Scanned across pixel
- Compare GL diameter:
  - 12um
  - 28um
- Very uniform gain across gain layer area
- Still significant gain outside GL area
  - ~x2 in fill factor

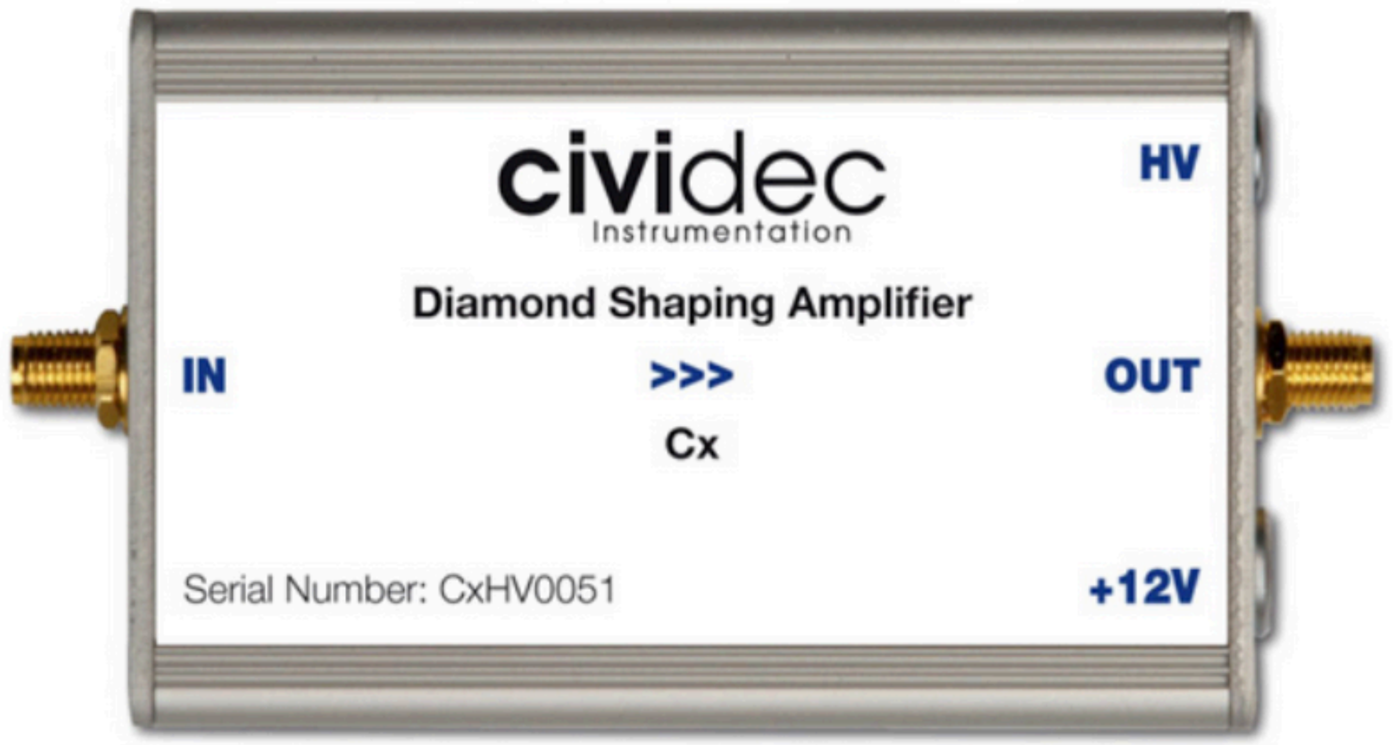




Pulsed laser measurements

- Pixel matrix exposed to triggered pulsed laser
  - Pulse width <100ps
  - Laser not focused (expose area>pixel)
- Pixel connected to external amplifier
  - Bias electrode through amplifier
  - Record single pulse waveform to analyse amplitude and arrival time wrt to external trigger
  - Record electrode current as function of pulse frequency
  - Record electrode current without laser (dark current)



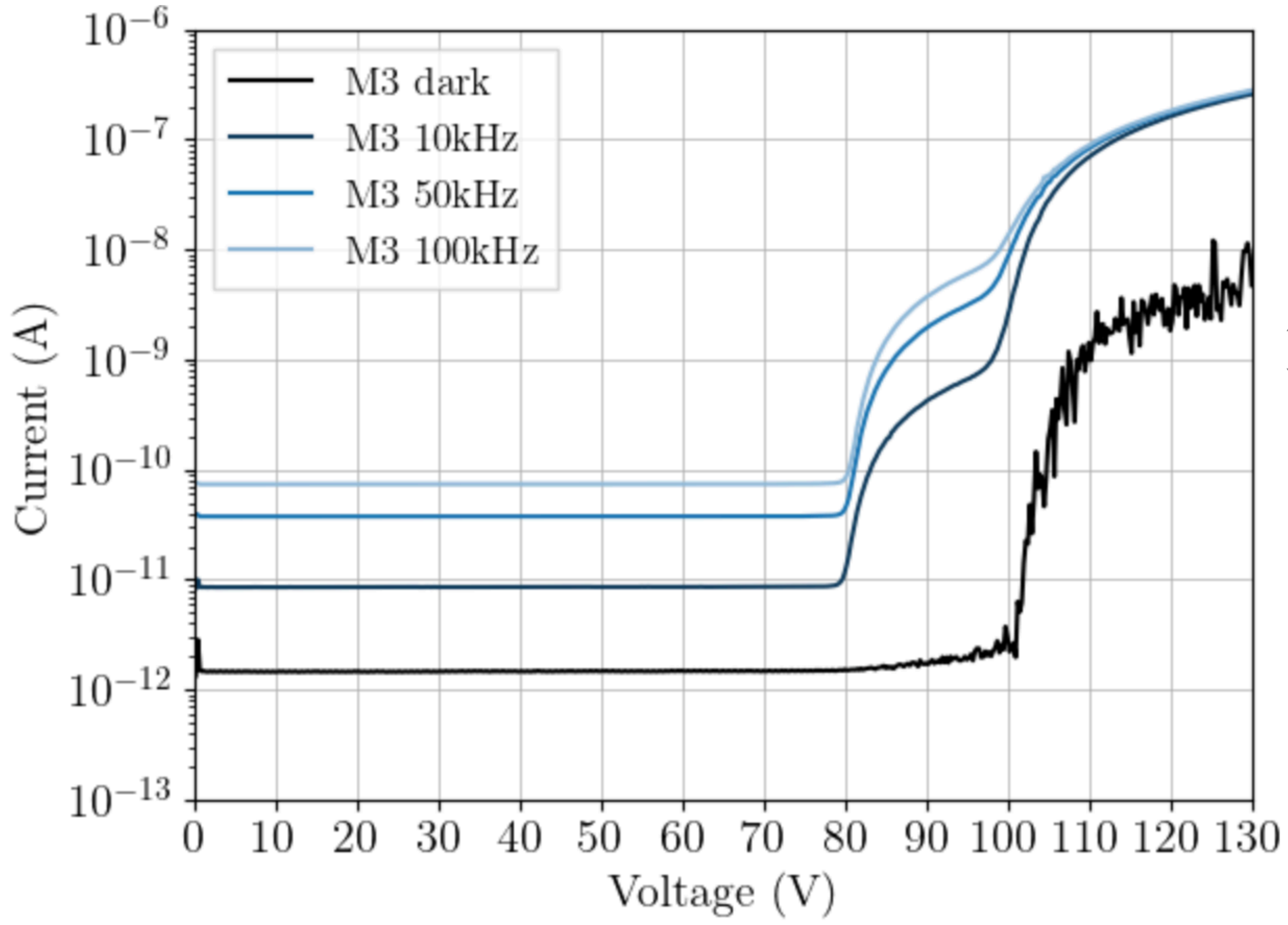


IV in pulsed laser measurements (triggered 1060nm laser)

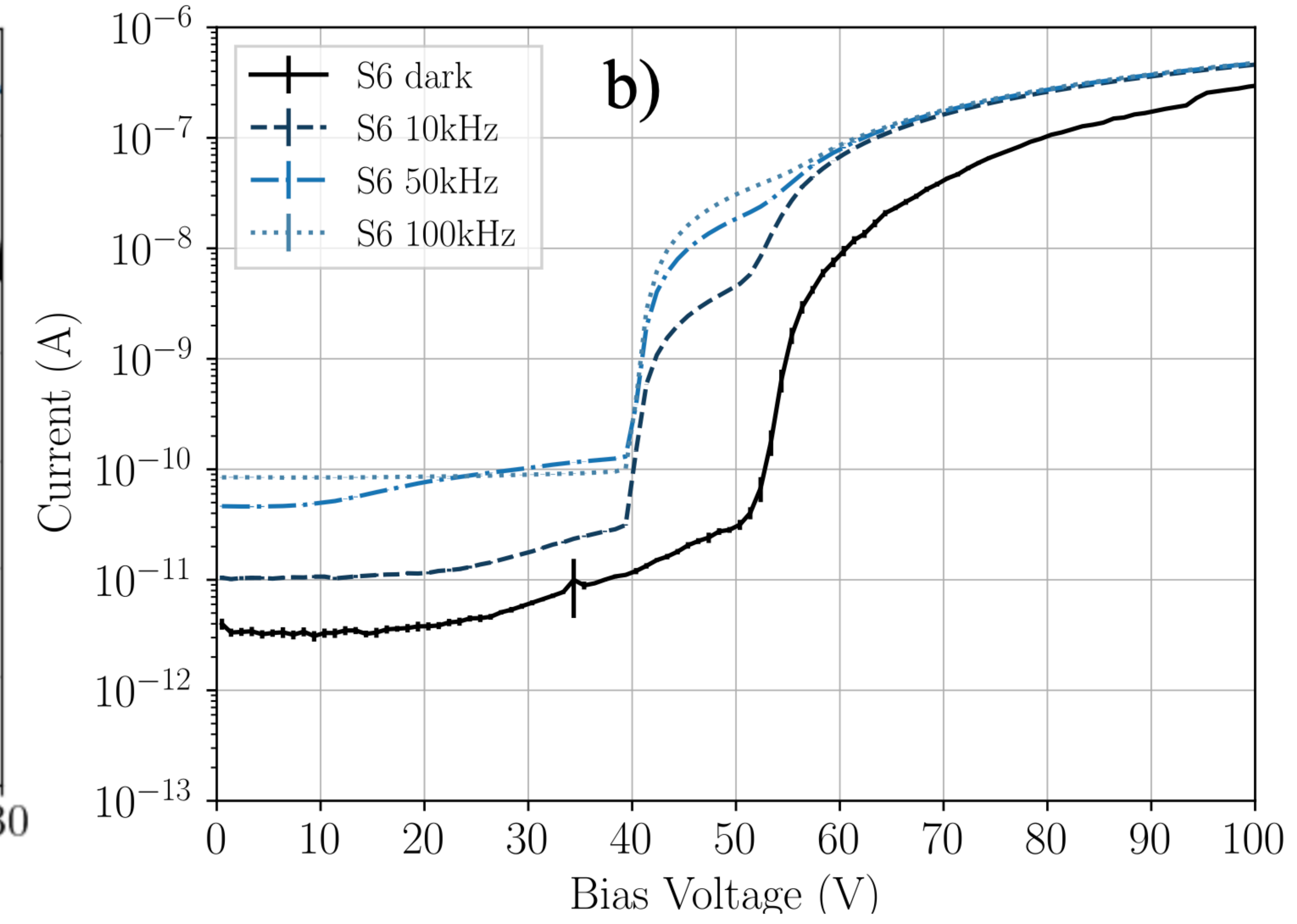
- IV in dark, and with 10kHz, 50kHz and 100kHz pulse frequency
  - substrate and PW on GND
  - n+ electrode biased
  - matrix without GL 1pA/pixel until 160V
- Study charge amplification as function of electrode and GL implant configuration
  - different gain layer diameter for each configuration

Example: NW electrode, gain layer depth 2

GL radius: 12µm



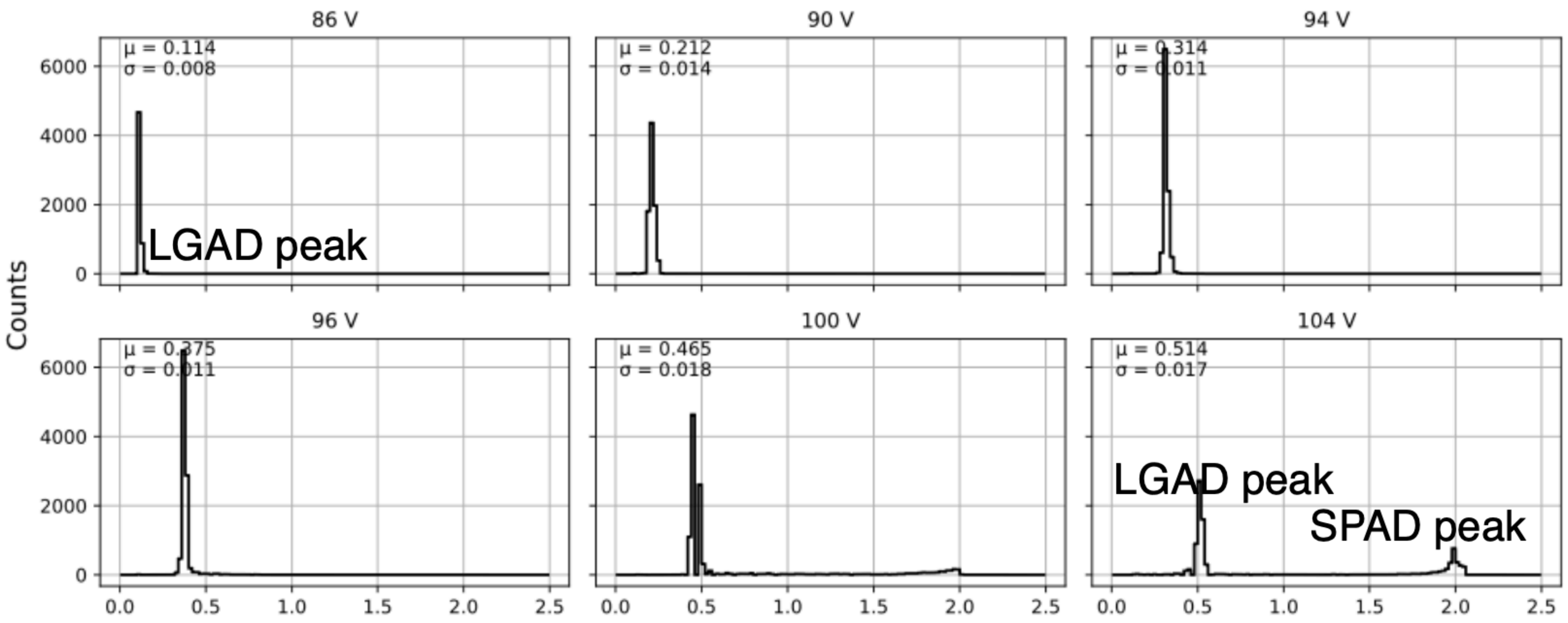
GL radius: 28µm



Single pulse amplitude distribution (triggered 1060nm laser)

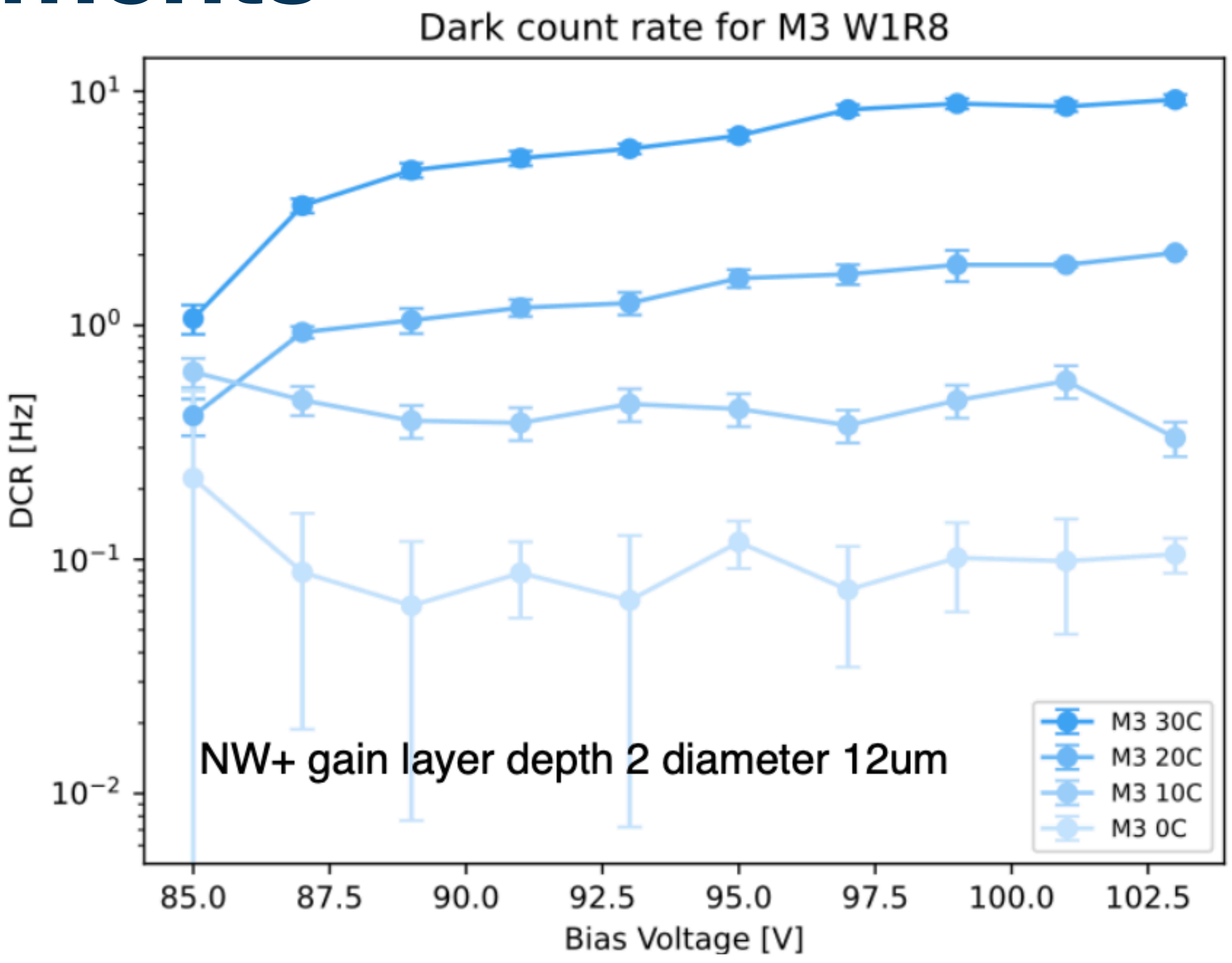
- Single pulse measurements:
    - for each external laser trigger the CASSIA single pulse signal is recorded for the central pixel on amplifier output
    - amplifier gain = 6.7mV/fC
- Analysis:
    - determine amplitude
    - use arrival time to reject any noise

NW electrode, gain layer depth 2, gl radius 12µm



Dark count measurements

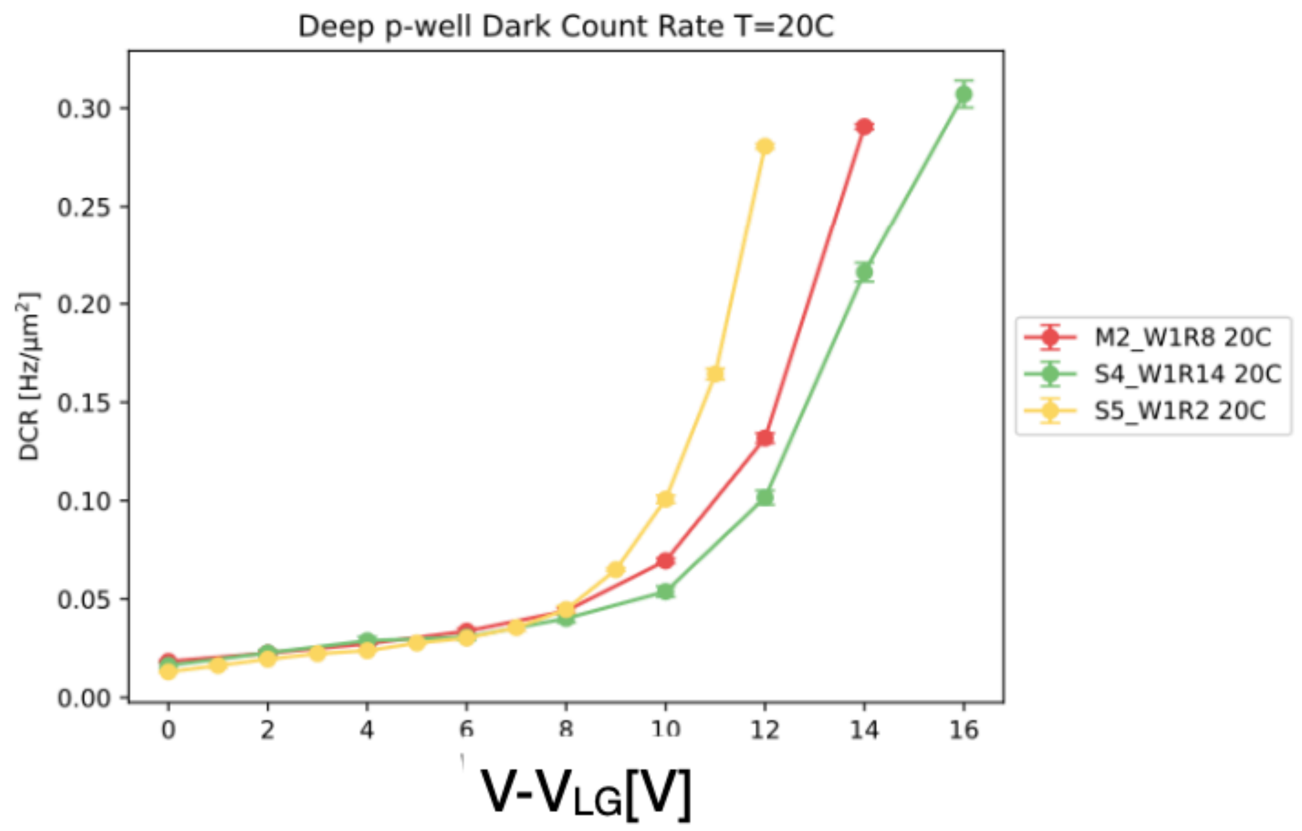
- Pulse frequency in dark
- Controlled temperature and humidity
  - We see exponential dependence on temperature
  - Thermally generated dark counts
- **DCR in LGAD region, with <0.01Hz/µm2 at room temperature**



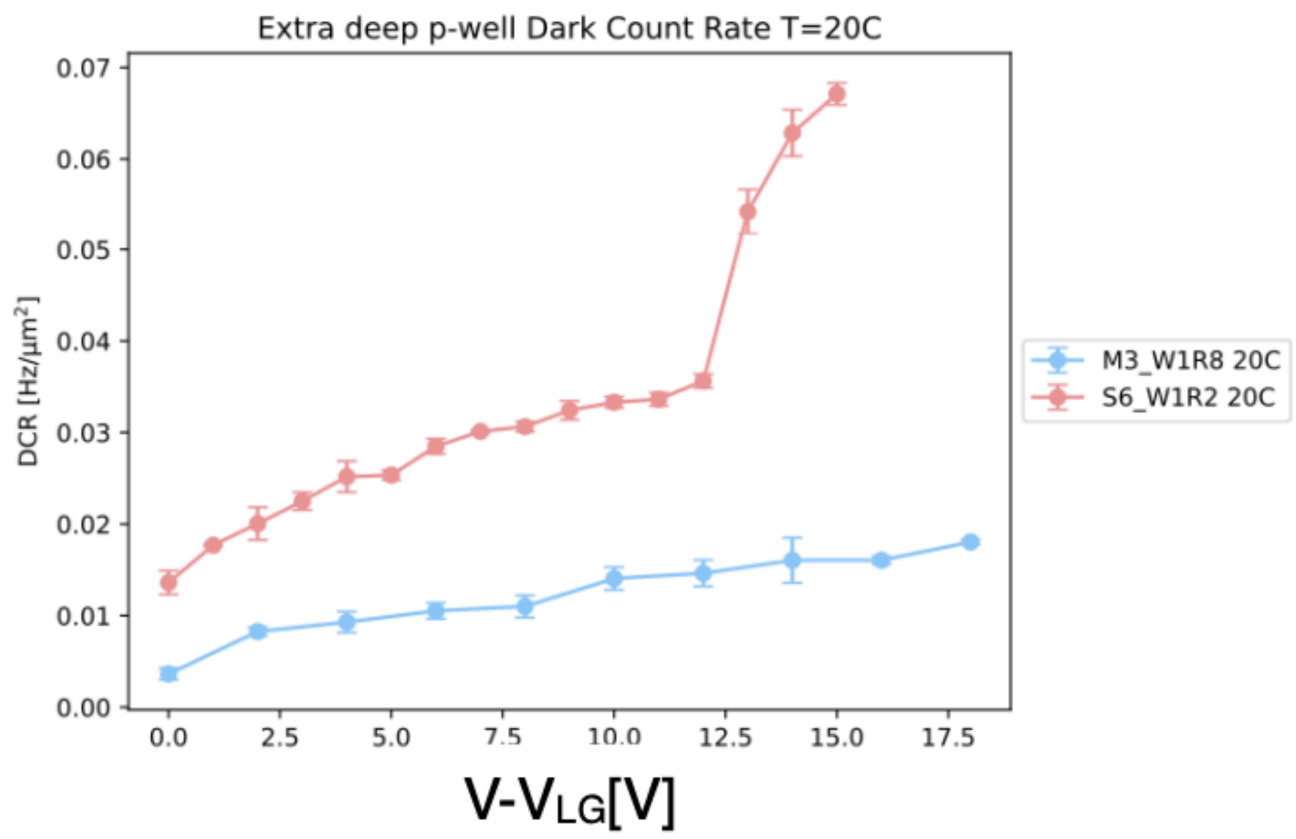
Dark count measurements

- DCR is seen to highly depend on GL/electrode implant combination
- Normalise DCR to gain layer area
- N+ electrode and gain layer depth 2 gives lowest DCR
- Shallow electrode and gain layer depth 2 gives highest DCR

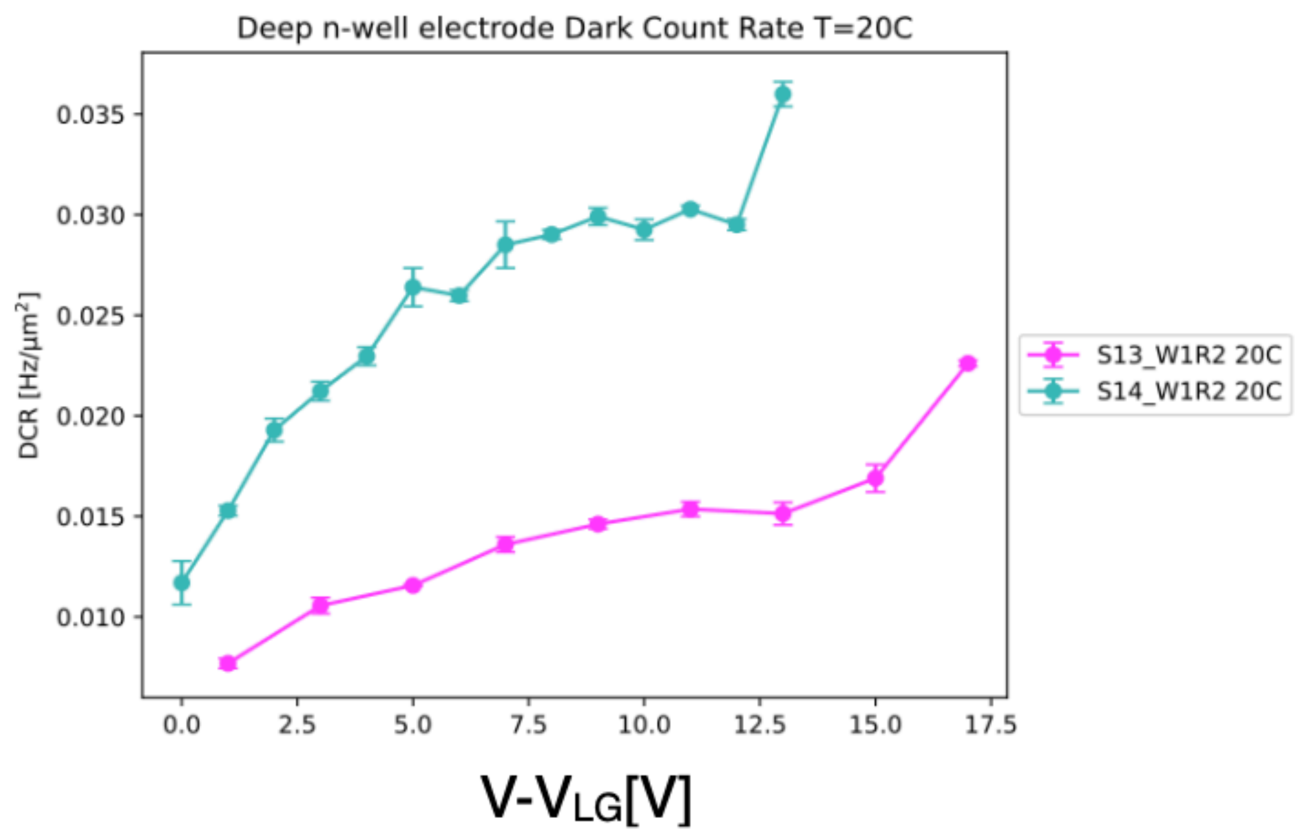
NW electrode + p-type GL depth 1



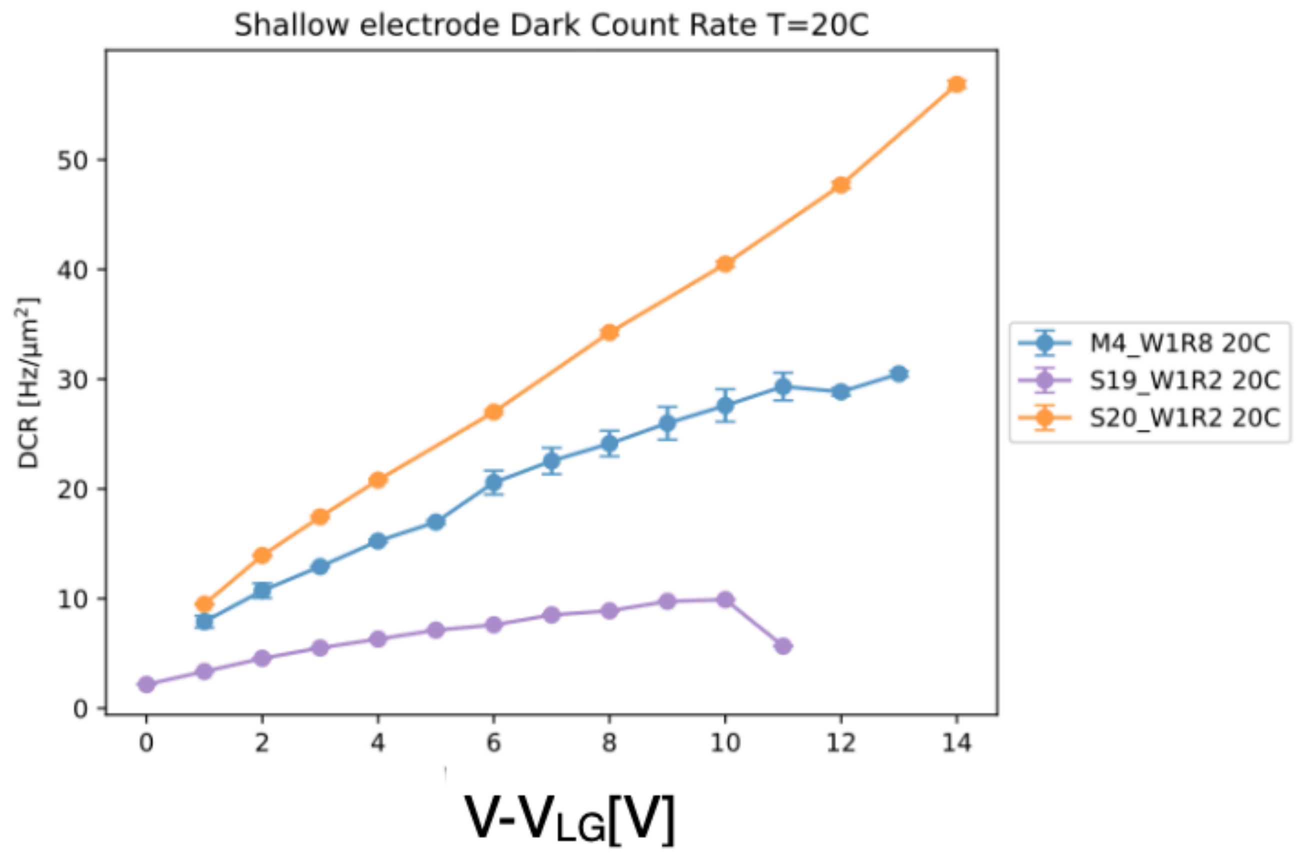
NW electrode + p-type GL depth 2



Deep electrode + p-type GL depth 2



Shallow electrode + p-type GL depth 2



Effect of implant variations

Observations

- Larger gain layer -> earlier breakdown
- Gain layer depth 2 -> later breakdown
- Shallow electrode -> later breakdown
- Shallow electrode -> higher DCR
- Gain layer depth 2 + NW electrode -> Lowest DCR

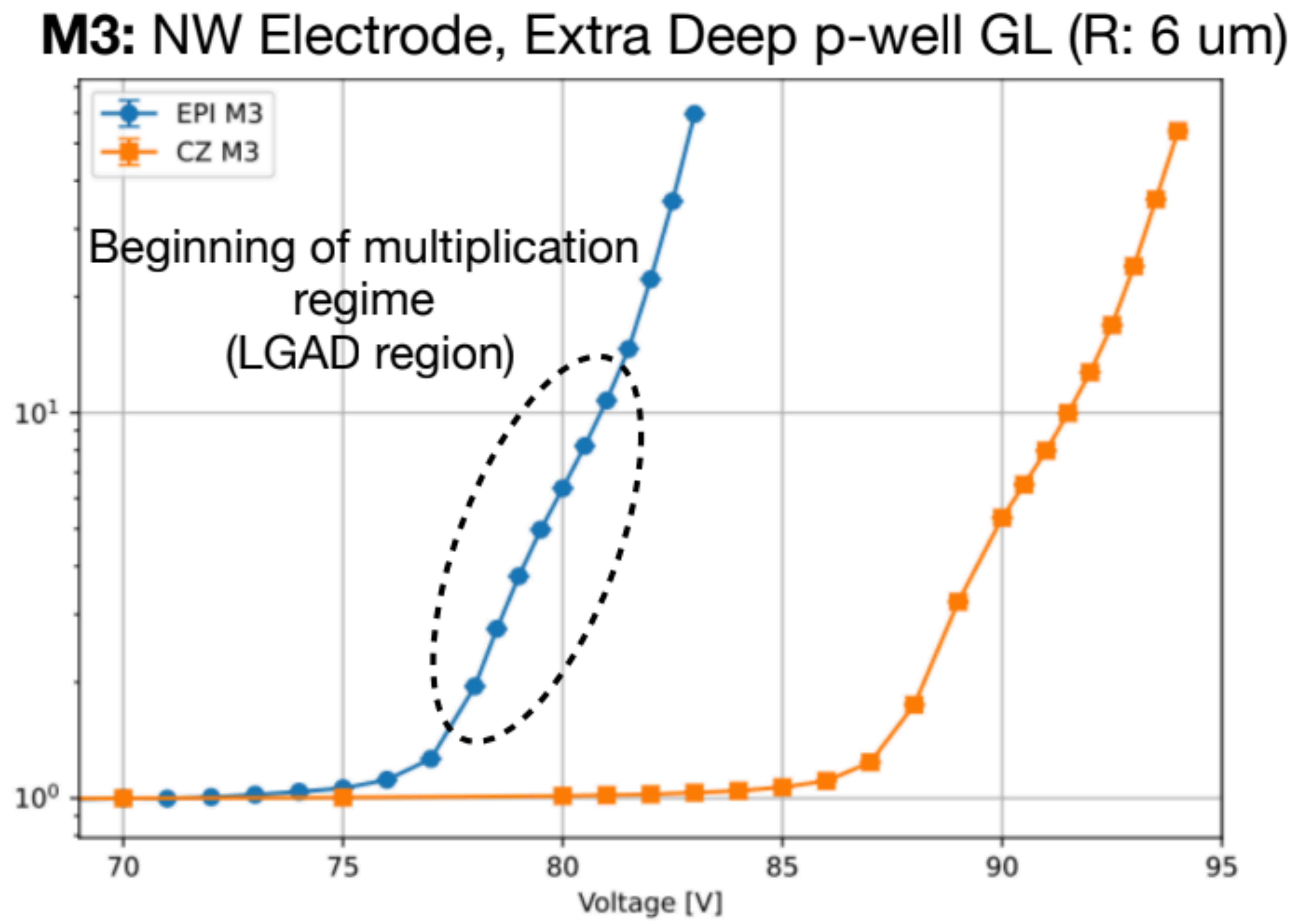
Thanks to Silas Müller for providing plots!

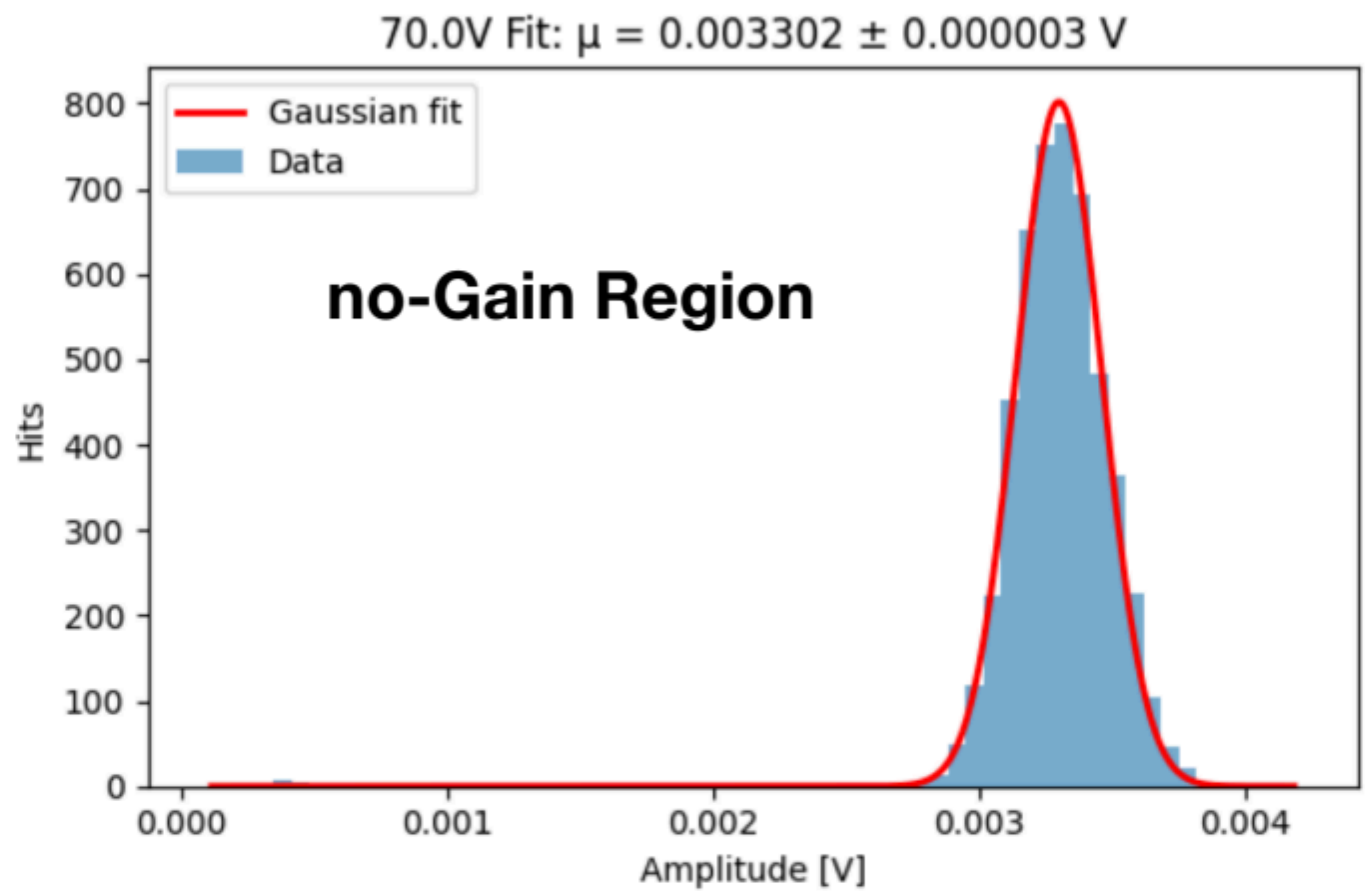
Gain measurements at Bonn

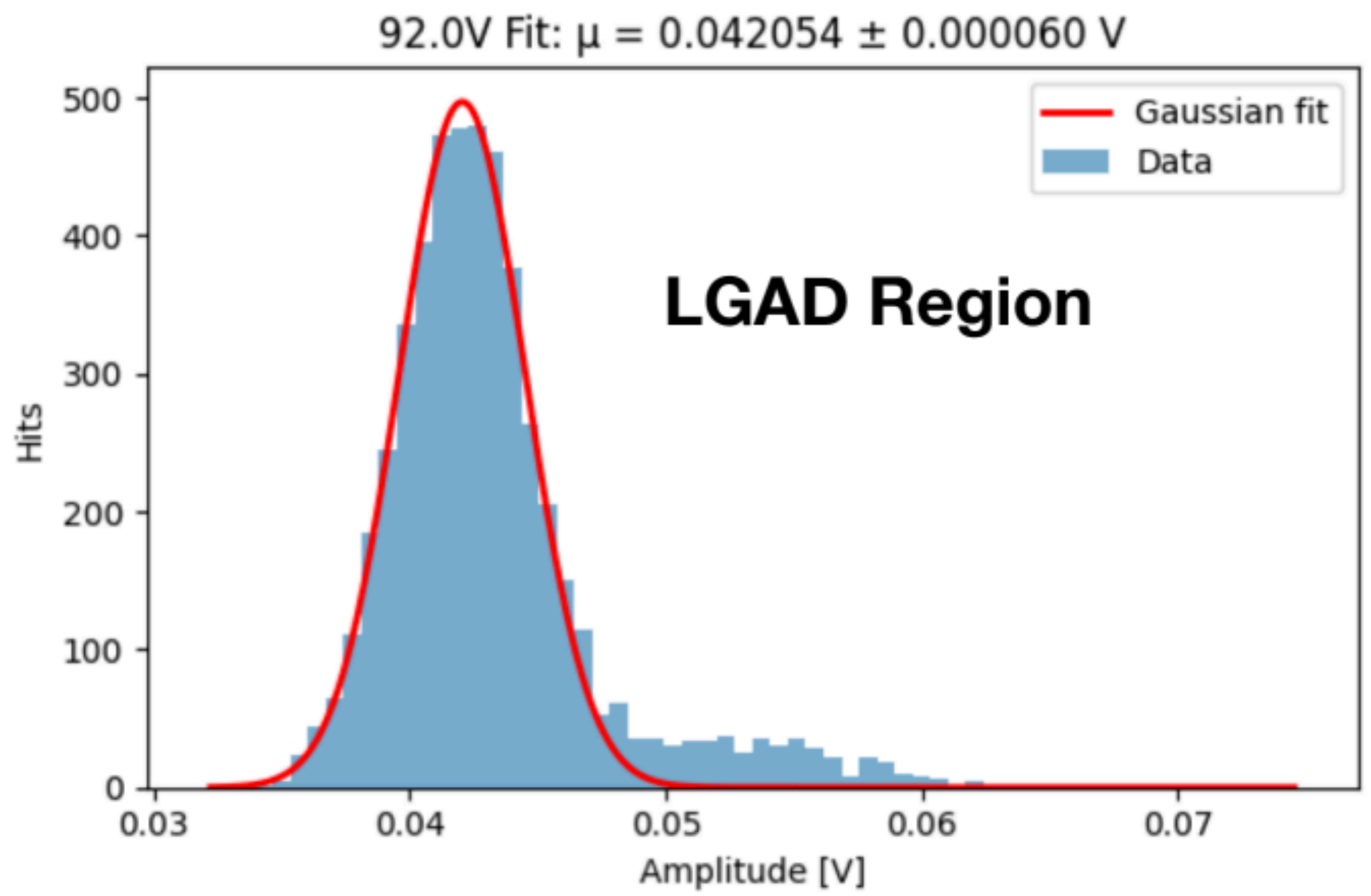
- Source measurements to measure absolute gain
- Gain defined as ration of amplitude in gain region over amplitude below gain region:

$$G = \frac{\text{Amplitude}\left(V_{\text{bias}} > V_{\text{BR,LGAD}}\right)}{\text{Amplitude}\left(V_{\text{bias}} < V_{\text{BR,LGAD}}\right)}$$

- Using 650nm laser focused on central electrode
- Measured on both EPI and Cz samples

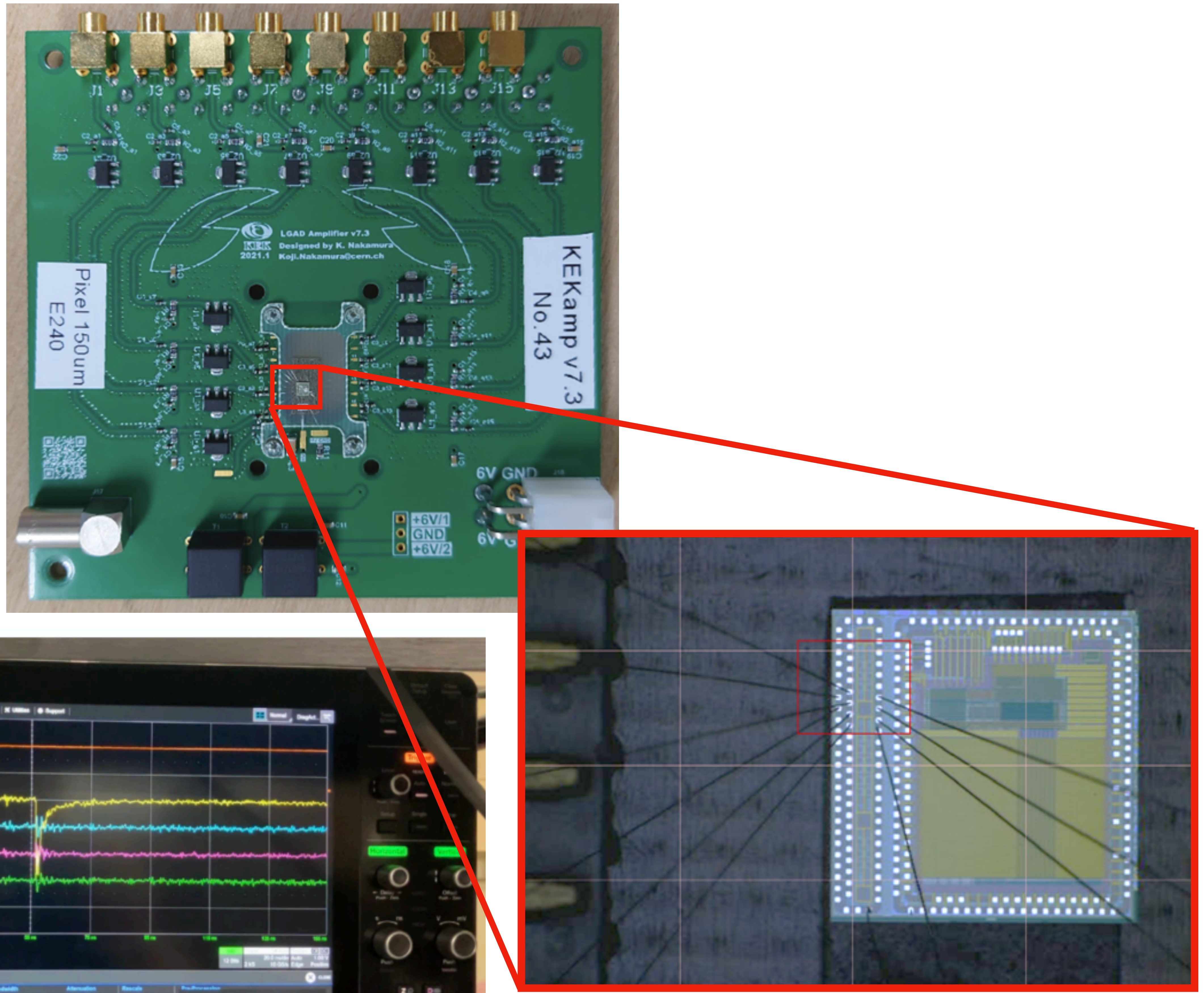


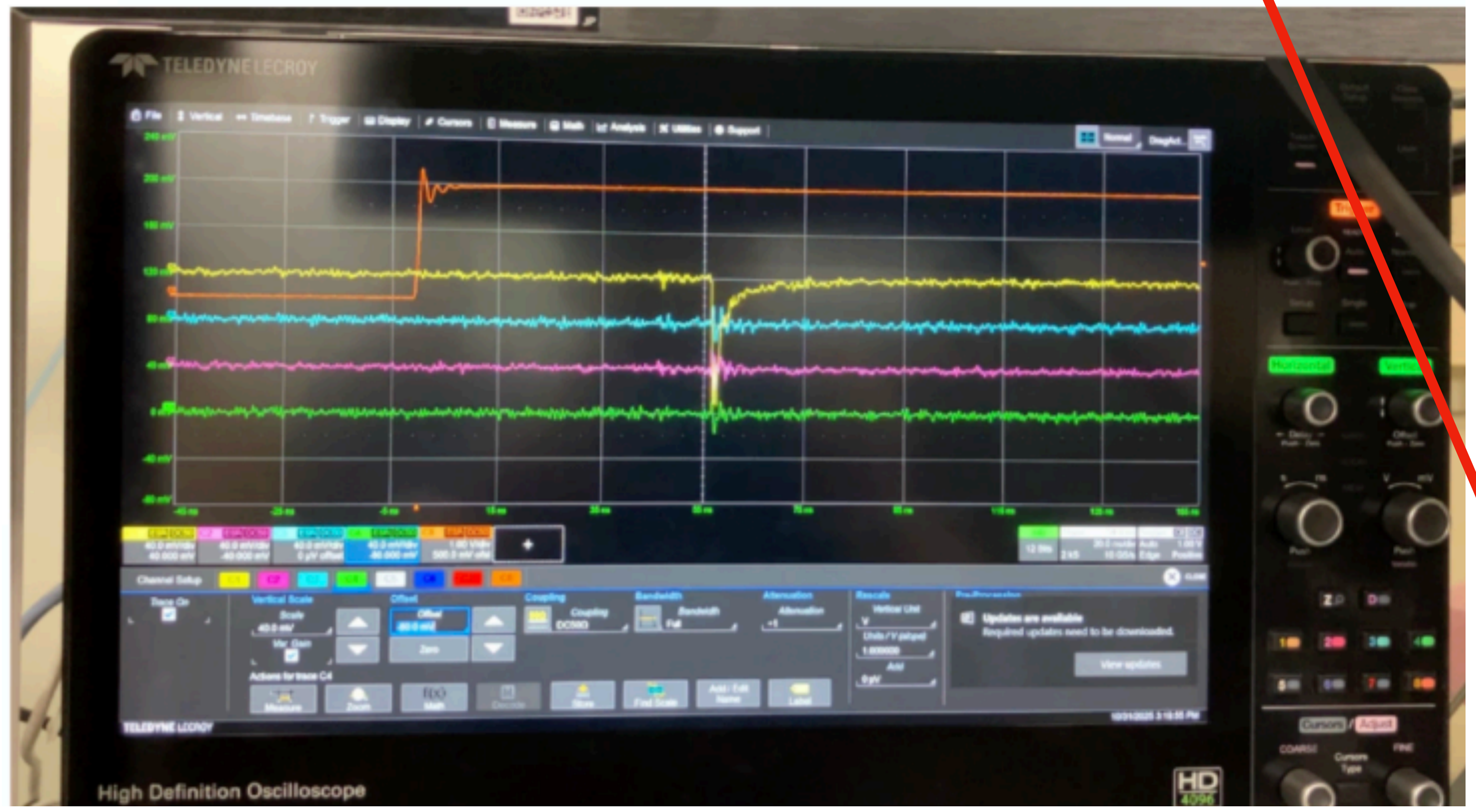




Upcoming timing measurements at KEK

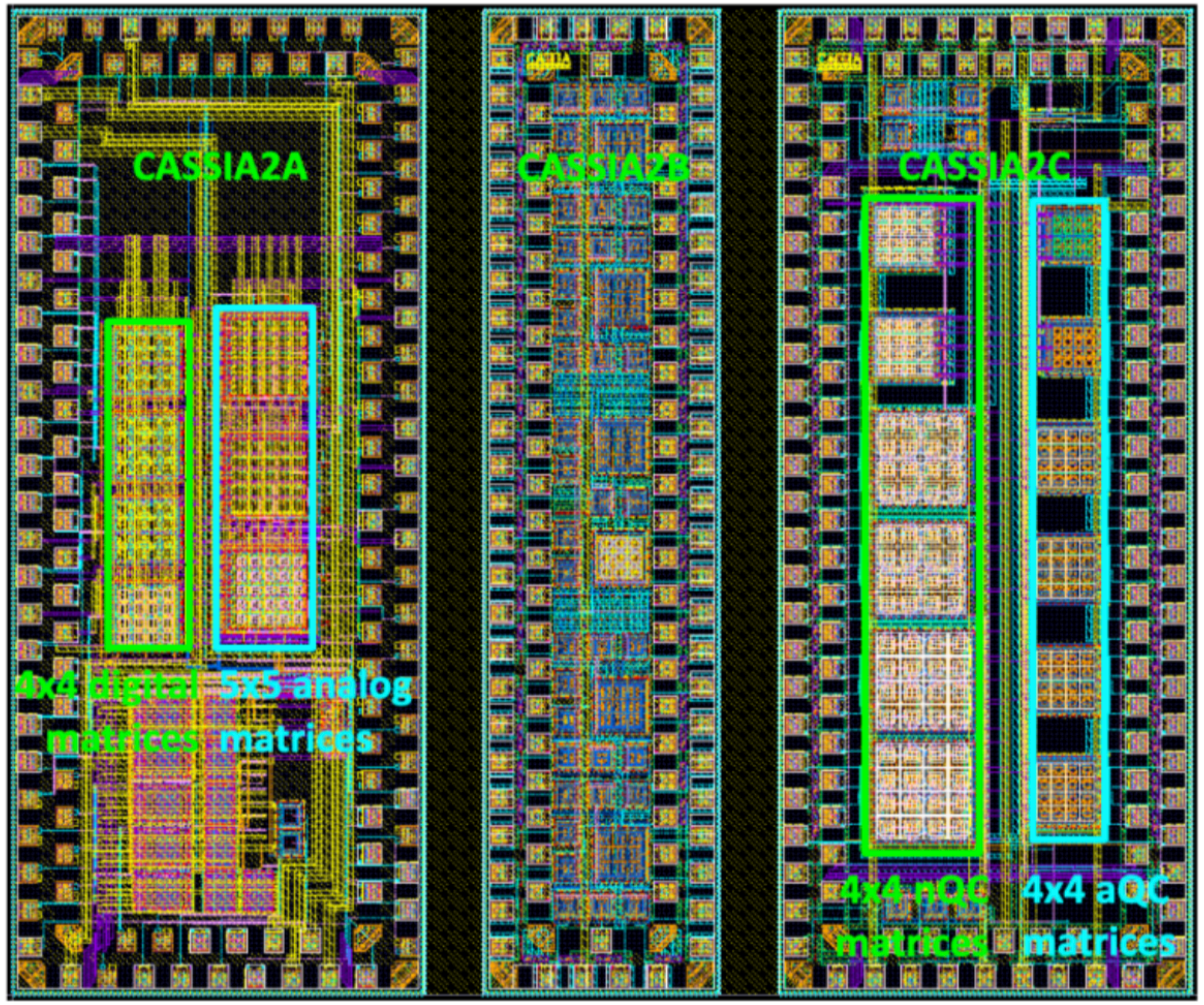
- Starting CASSIA1 measurements at KEK
- Two PCB boards sent from CERN + CASSIA bonded to KEK-designed amplifier board
- First IV measurements done
- Aiming for timing measurements with Sr-90 source





CASSIA2: Integrating on-chip electronics

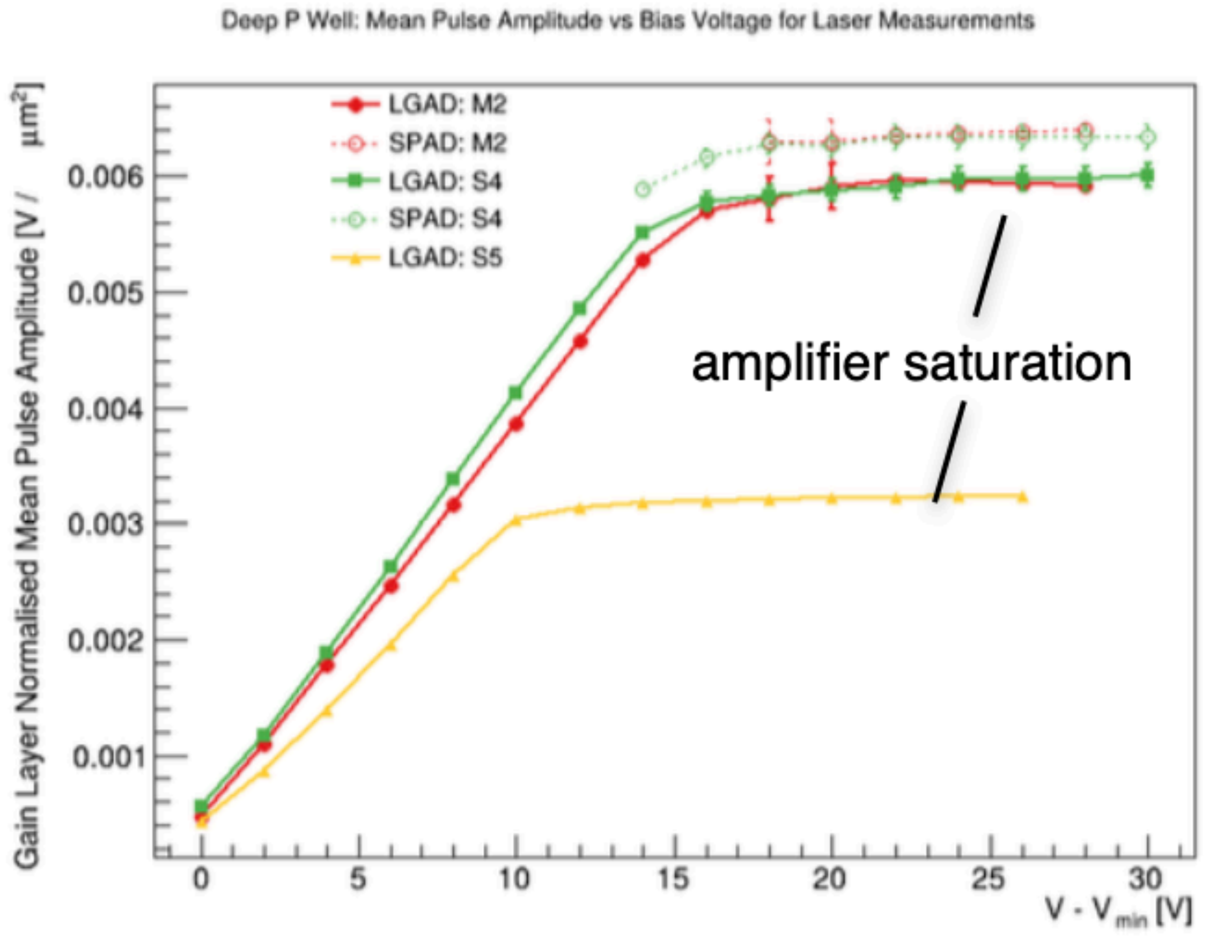
- **CASSIA2-A**
  - Focus on LGAD operation
  - Analog (4x4 matrices) and digital readout (5x5 matrices)
- **CASSIA2-B**
  - Multiple test structures without on-chip readout
  - Explore new structures, aiming for improved fill factor
- **CASSIA2-C**
  - Focus on SPAD operation
  - Quenching circuits (4x4 matrices)



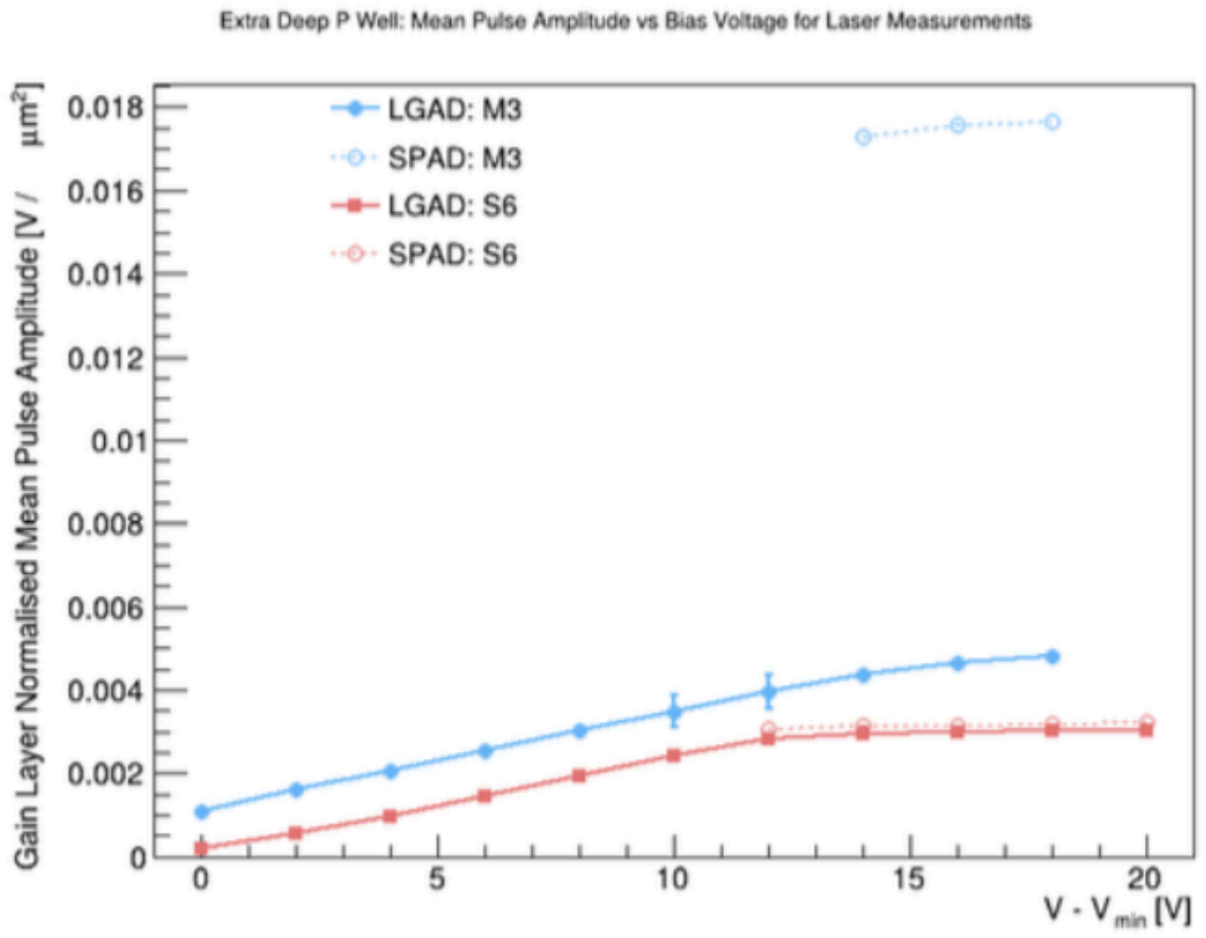
Summary

- With the CASSIA project we propose to develop CMOS sensors with **internal amplification**
  - Implemented in **TJ180nm**, 65nm envisaged for the future
- The CASSIA project is included in the **DRD3 working group** on monolithic sensors to address the research program through the design and test of dedicated prototype sensors
- Test from CASSIA1 show **clear gain modes observed for all structures**
  - LGAD and SPAD operational modes
- Breakdown and DCR dependent on implants and sensor geometry
  - **<0.01Hz/µm2 DCR** for n+ electrode and gain layer depth 2
- CASSIA2 designed with **analog and digital matrices**
  - Aiming to **improve fill factor**

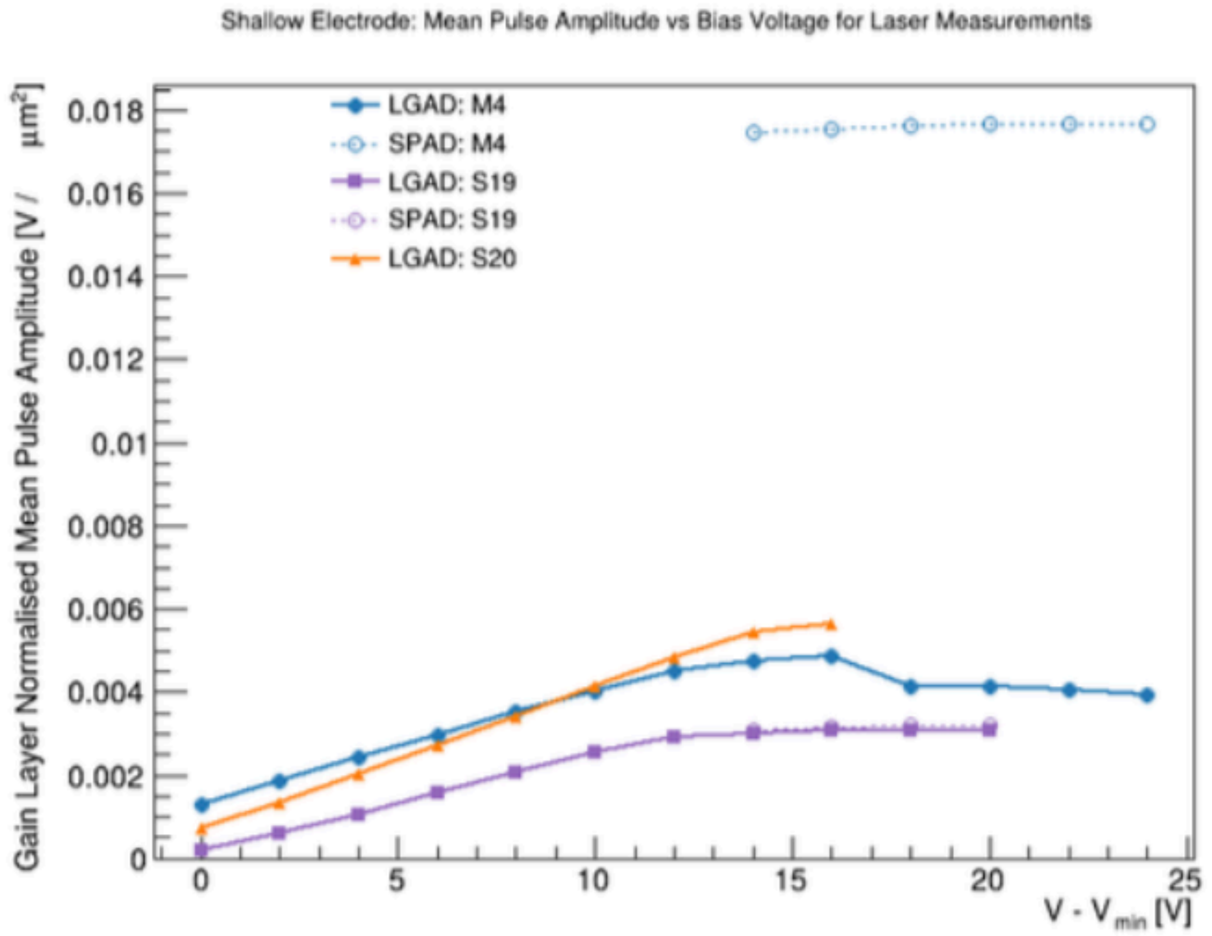
Back up



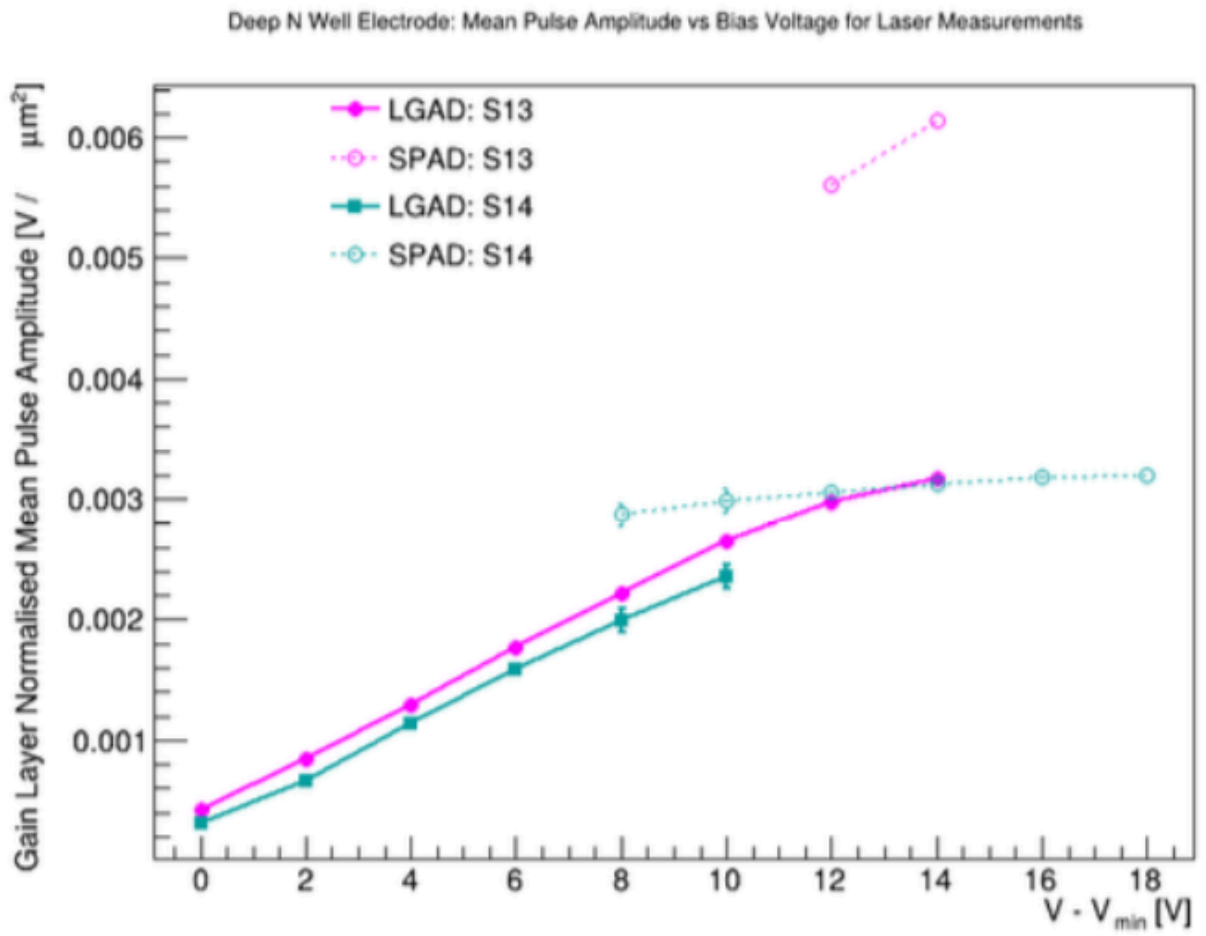
NW electrode + p-type GL depth 1
(a)



NW electrode + p-type GL depth 2
(b)

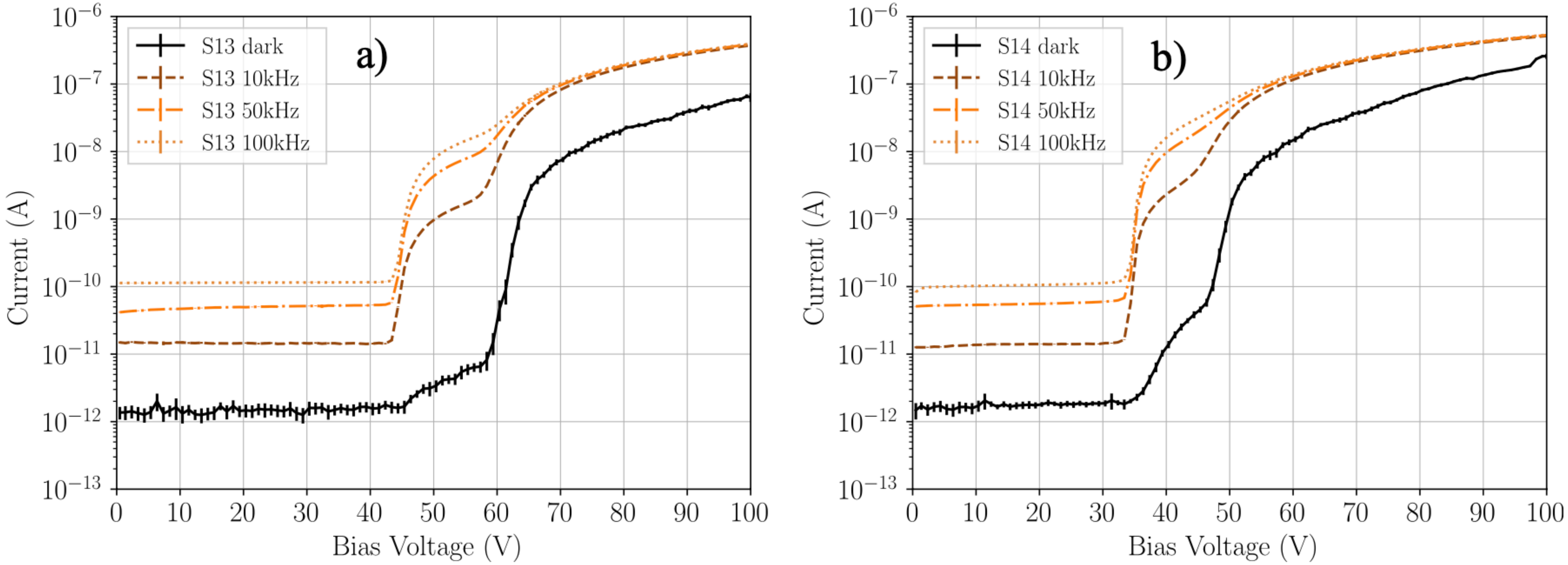


Shallow electrode + p-type GL depth 2
(c)

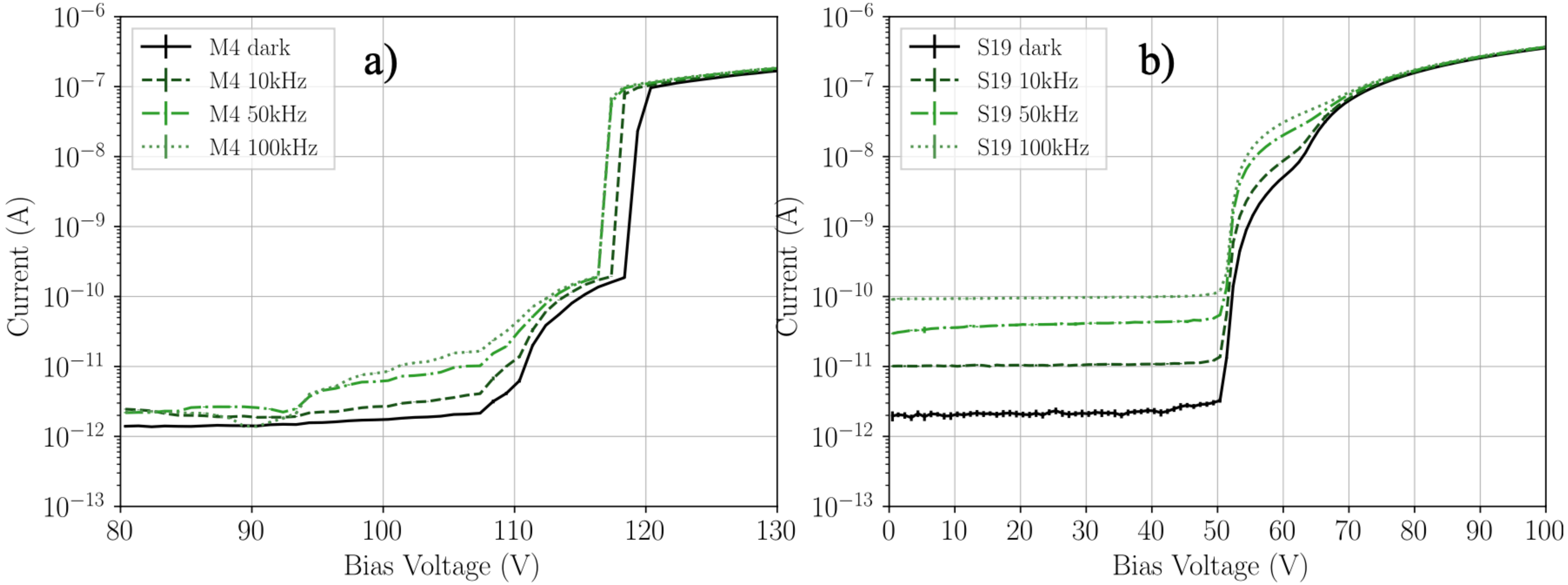


Deep electrode + p-type GL depth 2
(d)

Deep electrode, gain layer depth 2, gl radius 10μm & 14μm



Shallow electrode, gain layer depth 2, gl radius 6µm & 14µm



NW electrode, gain layer depth 1, gl radius 10µm, 10µm & 14µm