TCAD Optimization and Validation of MAPS with Internal Low-Gain Amplification

H. Shamas

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Future tracking and vertex detectors require sensors with finer pitch, improved timing resolution, and minimal power consumption. While monolithic CMOS pixel sensors (MAPS) offer a promising solution, their performance is somewhat limited by the small signal generated in their thin sensitive layers, down to 10 μm in some technologies.

The APICS (Impact Amplification with CMOS Pixel Sensor) project investigates the use of internal low-gain amplification structures to enhance signal levels and enable fast readout in small pitch designs. TCAD simulations are used to design and optimize gain-layer doping profiles and electric field configurations within a standard 180 nm CMOS imaging process. Simulations predict a gain of around $\times$10 at 55 V. With such gain, the signal from minimum ionising particles will exceed 0.7 V for an input capacitance of 2 fF, allowing to design a compact and power-saving in-pixel front-end circuits. The target pixel pitch is 15 μm, supporting integration into sensors featuring about 1 Megapixel.

To validate the simulation framework, experimental data from the CASSIA (CMOS Active Sensor with Internal Amplification) project at CERN was used. The test chips developed within this project, fabricated in the same technology and implementing similar gain structures but larger pitch, were characterized through laser-based measurements. The measurements confirm gain onset and signal behavior consistent with simulation, validating the TCAD optimization approach.

These results help guide the design of two prototype chips, which are planned for submission in the second half of 2025.

Authors List
IPHC: H.Shamas, J.Baudot, A.Dorokhov
ICube: T.Cocquerelle, W.Uhring
CERN: E. K. Anderson, S.Haberl, A.Kotsokechagia, J.Lunde, H.Pernegger, C.Solans Sanchez
University of Zagreb: P.Bartulović, I.Berdalović, M.Jugović, B.Požar, T.Suligoj