Fundação
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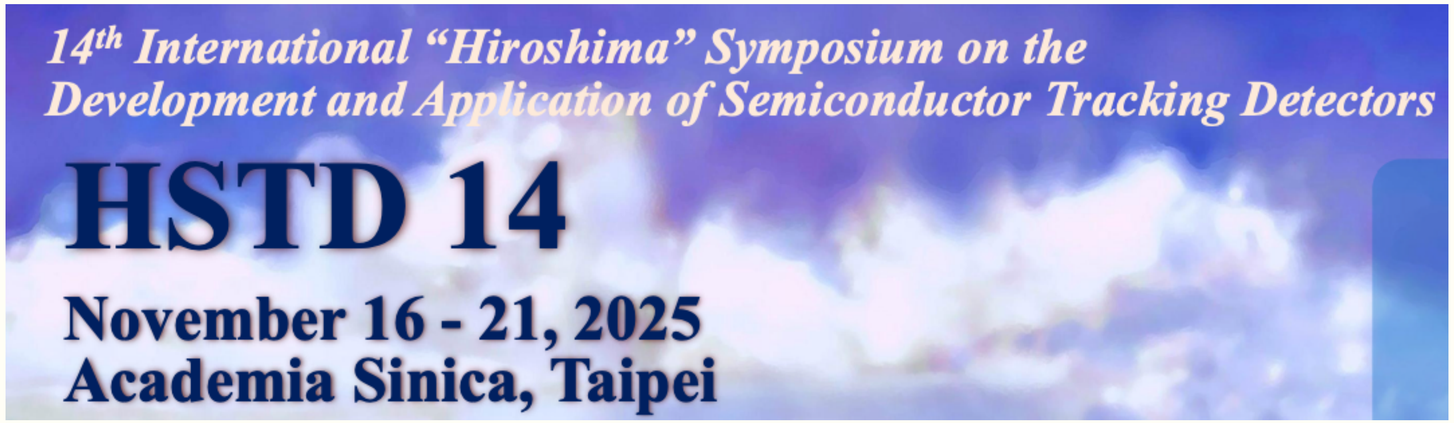
This work was financially supported by 2024.06584.CERN

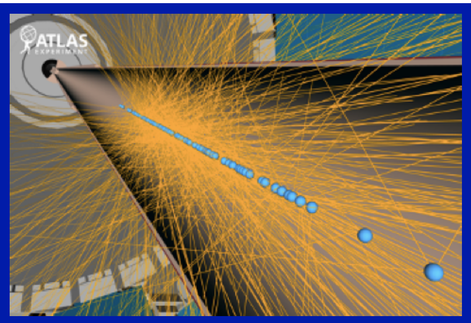
The ATLAS High-Granularity Timing Detector for the HL-LHC
Project Status and Results

Helena Santos (LIP) on behalf of the ATLAS HGTD Collaboration

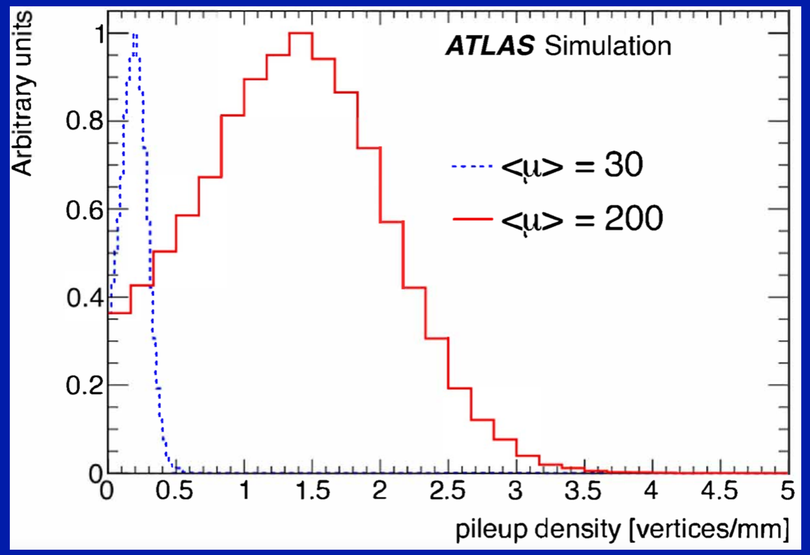


Why do we need a timing detector in ATLAS

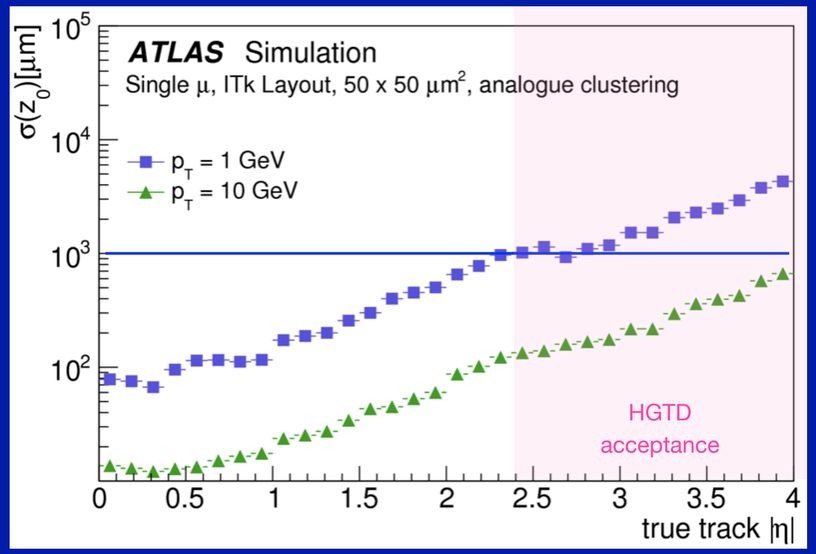
HGTD Public Results



Pileup ⟨μ⟩ can be 200 interactions per bunch-crossing at the HL-LHC. Vertex density will be on average 1.6 vertices/mm



Longitudinal impact-parameter track resolution, $\sigma(z_0)$, worsens at large η



→ Vertex spacing (~0.6 mm) smaller than z_0 resolution in the forward region

→ Reconstructed vertices overlap

→ Tracks from different vertices can be assigned to a given vertex

Ambiguity in track to vertex association

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HGTD Public Results

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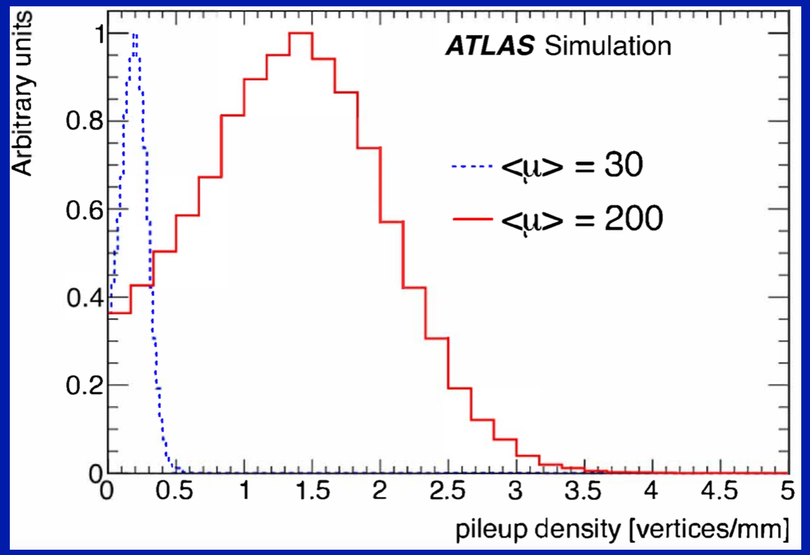

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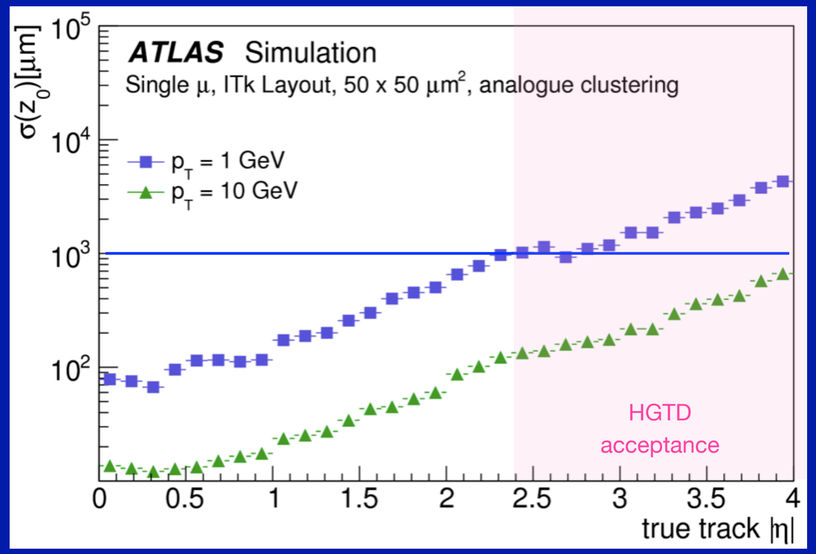

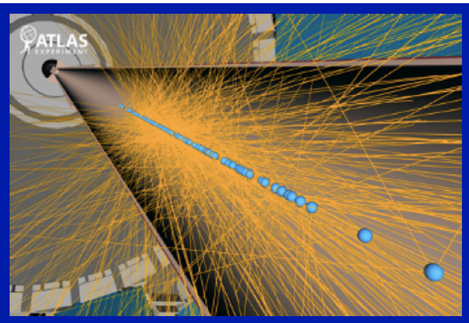

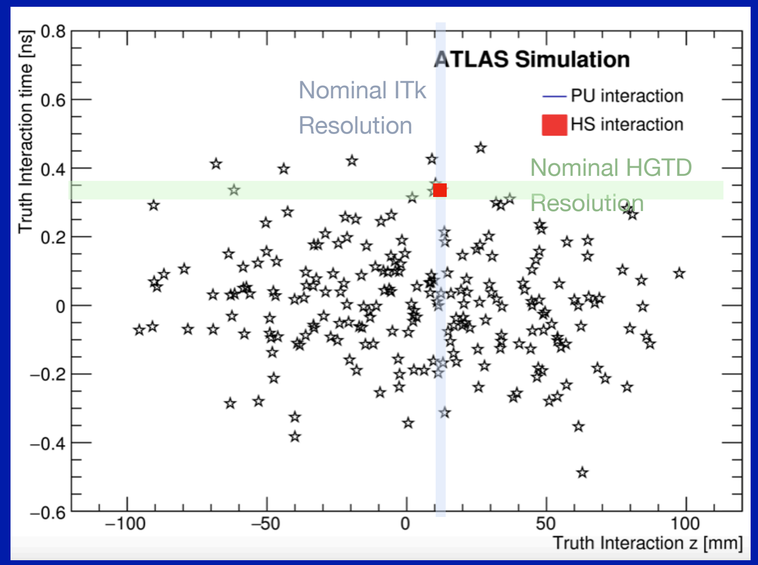

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Ambiguity in track to vertex association

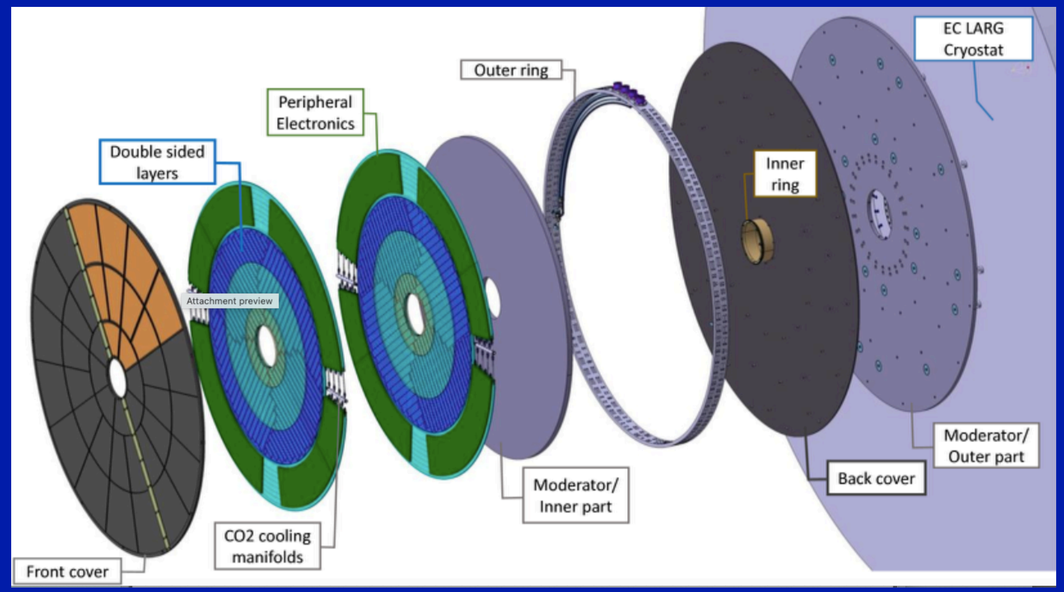
HGTD, with its precise timing, can associate a time to each track with unprecedented accuracy

It will work if σ_{time} << vertex spread in time is (~180 ps)

HGTD - Characteristics

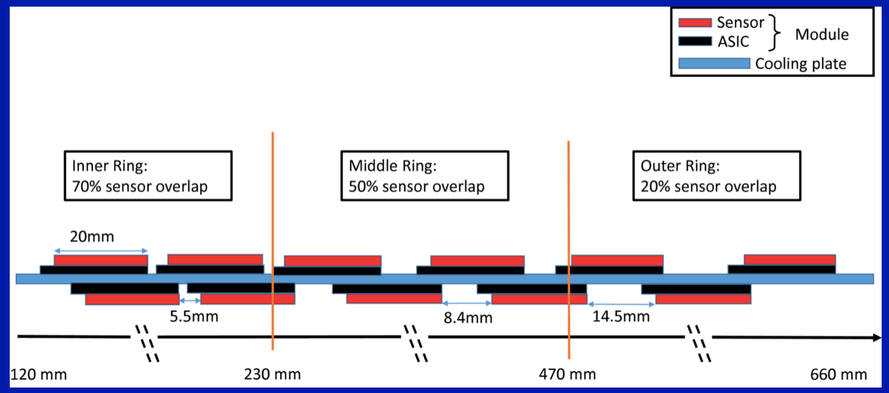
Pad detector for precision timing in the forward region of ATLAS:

- Two endcaps positioned between the barrel and endcap calorimeters
- Each endcap: two disks with detectors mounted on both sides
- Located at ±3.5 m from the interaction point
- Active coverage: $2.4 < |\eta| < 4$
- Radial range: 120 mm < r < 640 mm
- Radiation hardness:
  - Up to 2.5×10^{15} n_{eq}/cm^2
  - 2 MGy total ionising dose (TID)



Performance Goals

- Time resolution (per hit): 40–85 ps up to 4000 fb^{-1}
- Time resolution (per track): 30–50 ps up to 4000 fb^{-1}



Luminosity Measurement

- Counts hits at 40 MHz, bunch-by-bunch
- Target precision: 1% luminosity uncertainty for HL-LHC

Sensor Technology - LGAD

16064 silicon sensors with internal gain based on LGAD (Low Gain Avalanche Diode) technology

Pad & Sensor specifications

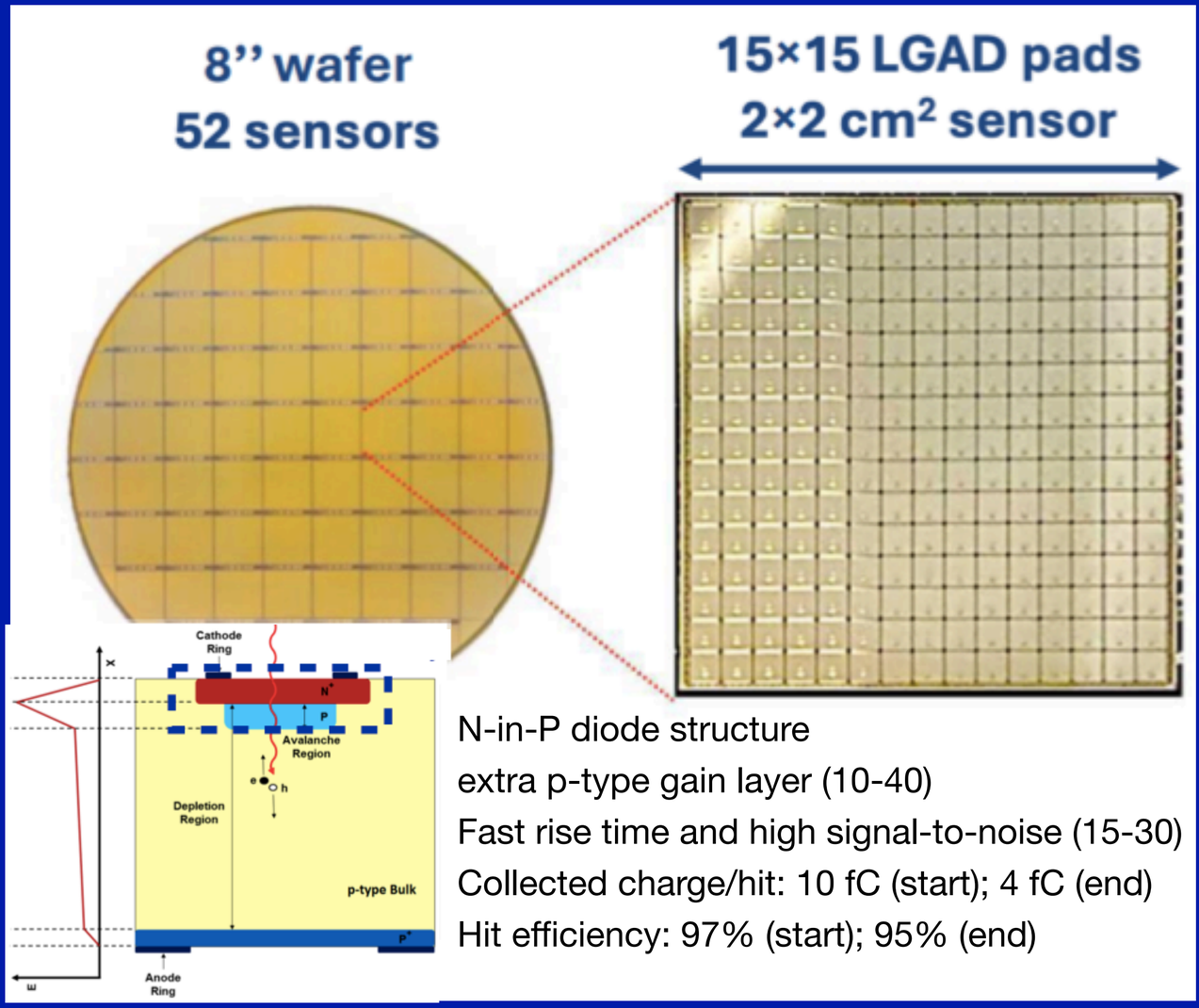
- Pad matrix: 15 × 15 = 225 pad per sensor
- Pad size: 1.3 mm × 1.3 mm
- Active thickness: 50 μm
- Total thickness: 775 μm

Detector design

- Four sensor layers → ensures ≥ 2 hits per track

Sensor production

- 8-inch silicon wafers
- 52 sensor arrays per wafer

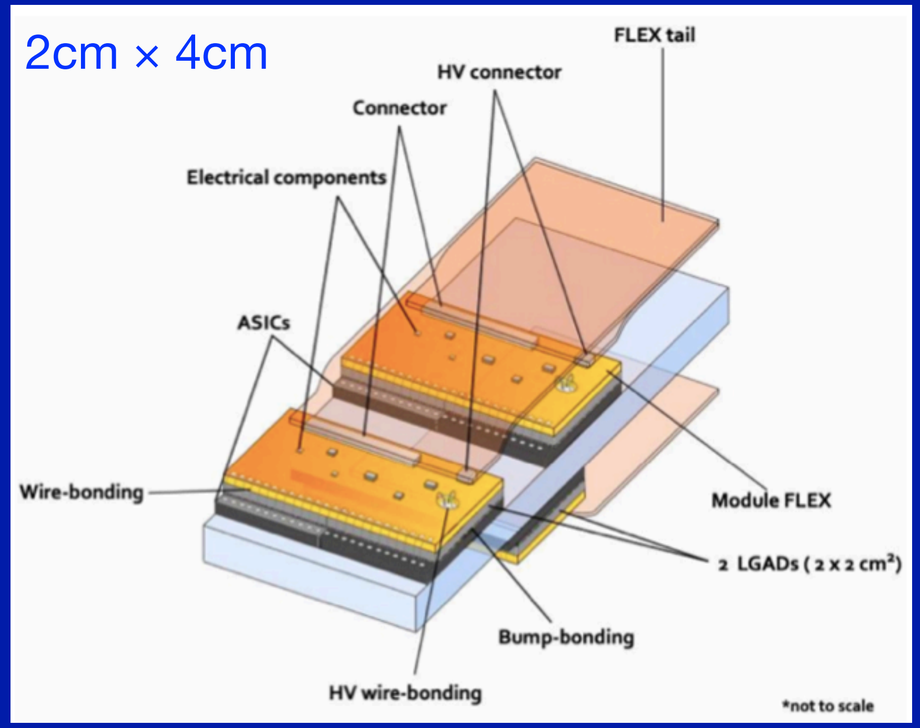


N-in-P diode structure
extra p-type gain layer (10-40)
Fast rise time and high signal-to-noise (15-30)
Collected charge/hit: 10 fC (start); 4 fC (end)
Hit efficiency: 97% (start); 95% (end)

The ALTIROC Module

ATLAS LGAD Timing Integrated ReadOut Chip

- Two readout ASICs bump-bonded to two LGAD sensors, mounted on a PCB for power and communication
- A FLEX tail carrying HV, LV and signals to/from peripheral electronics boards (PEB)
- Per-module HV settings to accommodate the variation of radial fluence
- LGAD sensor temperature will be maintained at -30 °C using an evaporative CO_2 cooling manifold integrated in the disks



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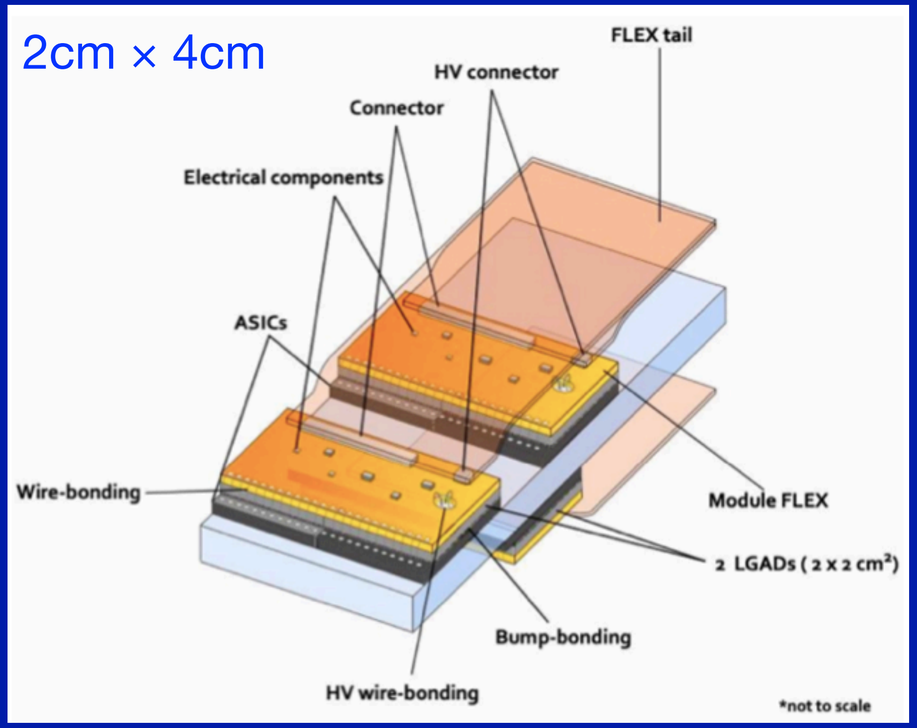
Specifications:

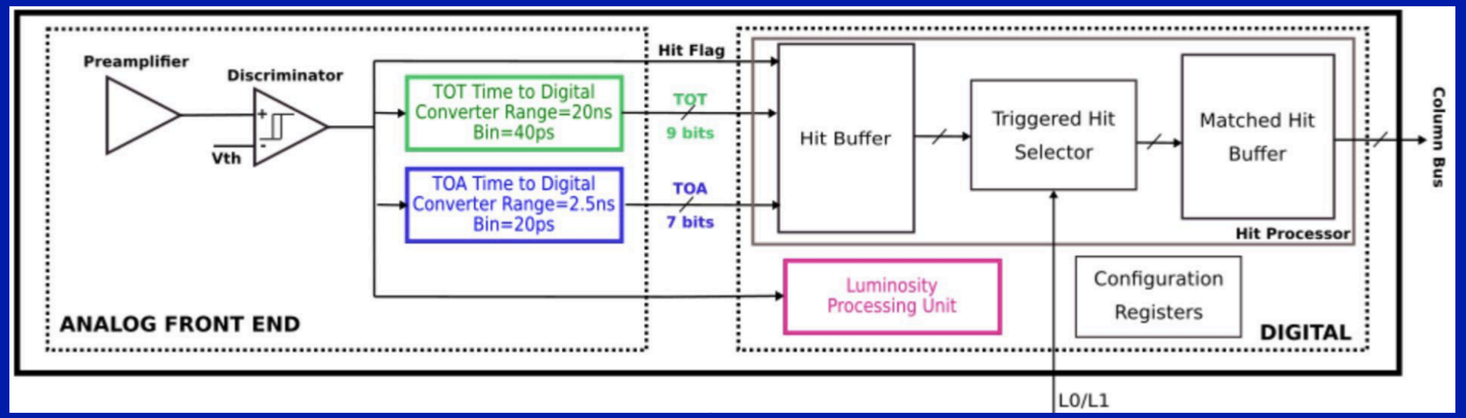
- Rad-Tolerant 130 nm CMOS (TSMC)
- 225 (15x15) channels, matching the sensor number
- Measures the Time Of Arrival (TOA) and Time Over Threshold (TOT, for time-walk correction)
- Minimum discriminator threshold: 2 fC
- Timing resolution: Jitter < 25 ps @ 10 fC and <65 ps @ 4 fC
- Cooling power requirement (20 kW/vessel):
  Overall (sensor) power density: < 300 mW/cm² (100 mW/cm²)



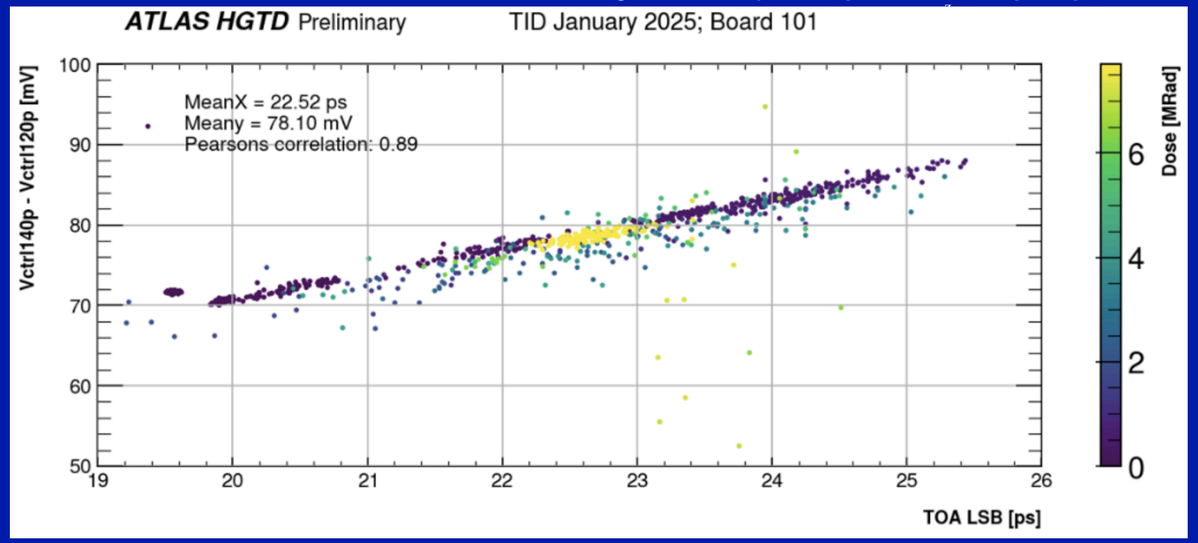
The ALTIROC Module

HGTD Public Results

- Timing and hit data stored in local registers
- On Level0 Accept they are sent off-chip (≤ 35 μs latency)
- Luminosity derived from hit rate per ASIC per bunch-crossing



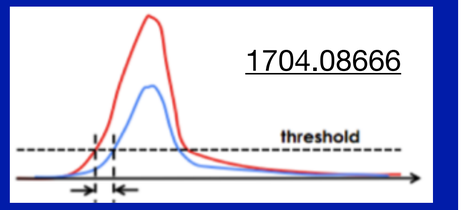
TOA TDC calibration: Vernier delay lines (120 ps / 140 ps per stage)



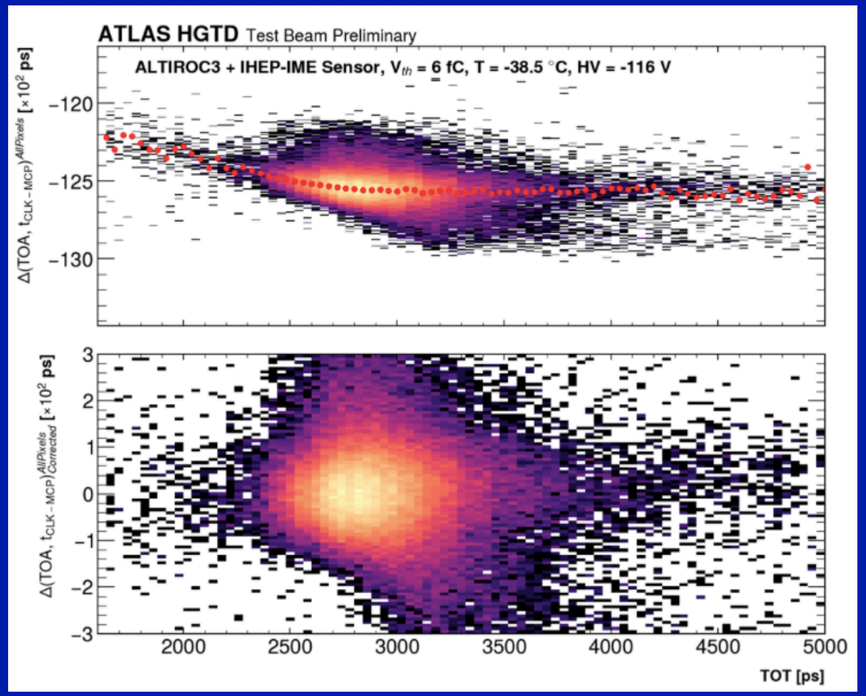
Larger V_{ctrl} difference → wider time bin

Stable correlation under irradiation

TOT: used to correct TOA shifts due to time-walk



TOA before and after TOT-based time-walk correction



TOA residuals are flat

Time Resolution

HGTD Public Results

$$\sigma^2_{total} = \overbrace{\sigma^2_{Landau} + \sigma^2_{jitter}}^{sensor} + \overbrace{\sigma^2_{TDC} + \sigma^2_{clock} + \sigma^2_{time\text{-}walk}}^{ASIC\ +\ readout}$$

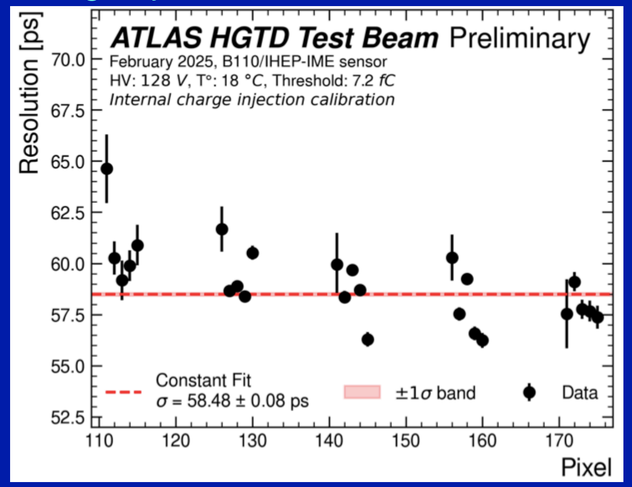
- TOA calibration applied here includes:

  - Per-channel TOA linearization, performed using either internal charge injection (ASIC) or testbeam data (with LGAD signals)

  - TOT-based time-walk correction, derived from testbeam TOT–TOA curves

-

Charge injection, no TWC



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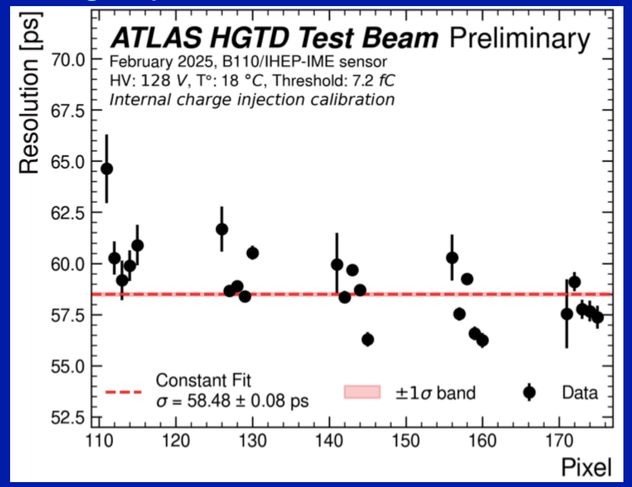
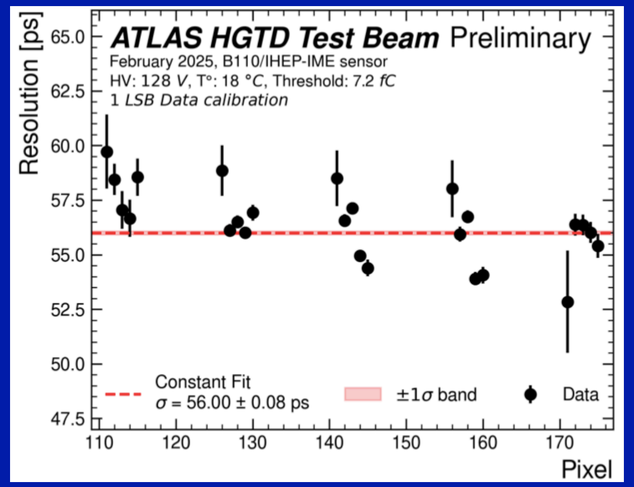
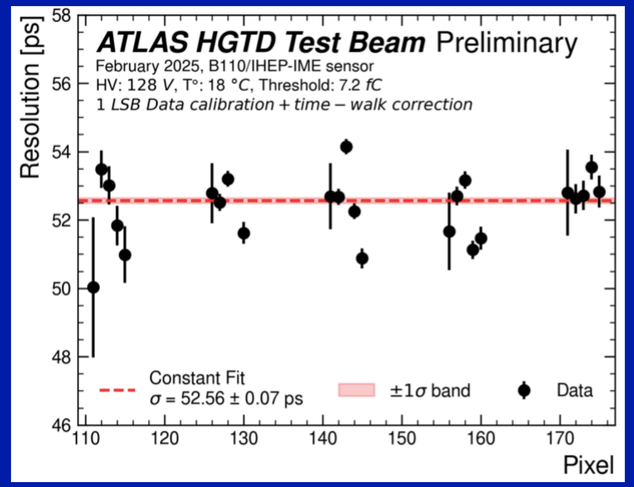


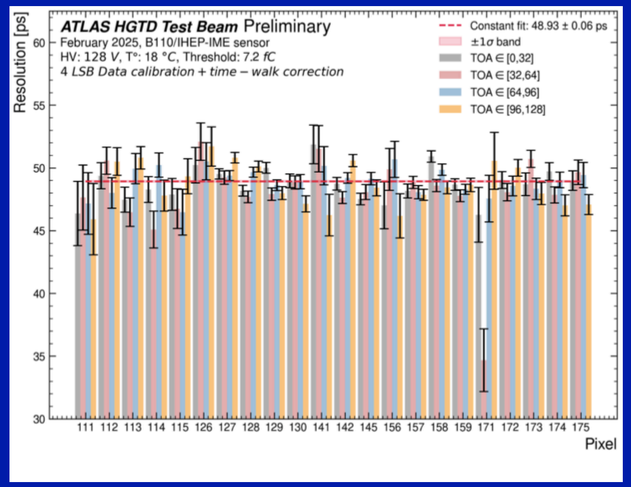
TB data, no TWC



TB data, with TWC



TB data, 4 LSB corr. for DNL, with TWC



In testbeam data, time resolution is extracted from residuals between calibrated TOA (ASIC) and MCP-PMT reference

Data-driven method improves resolution significantly, exposing the intrinsic sensor limit

Time Resolution

HGTD Public Results

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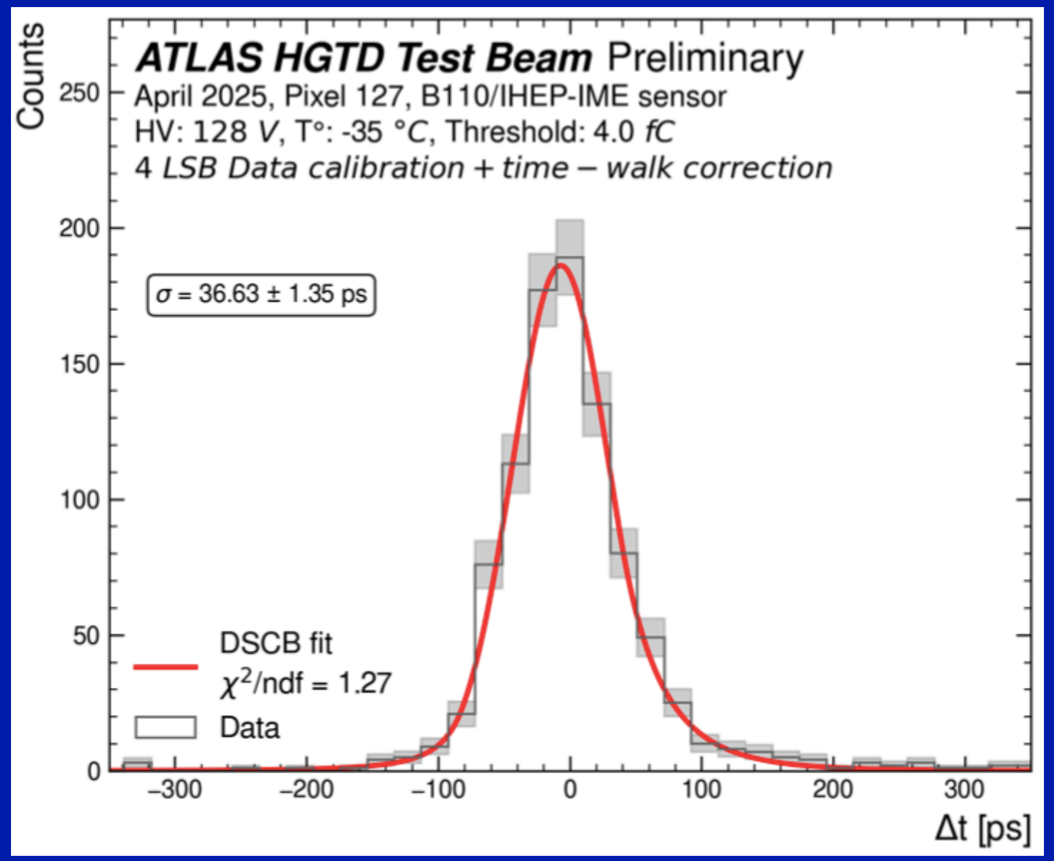
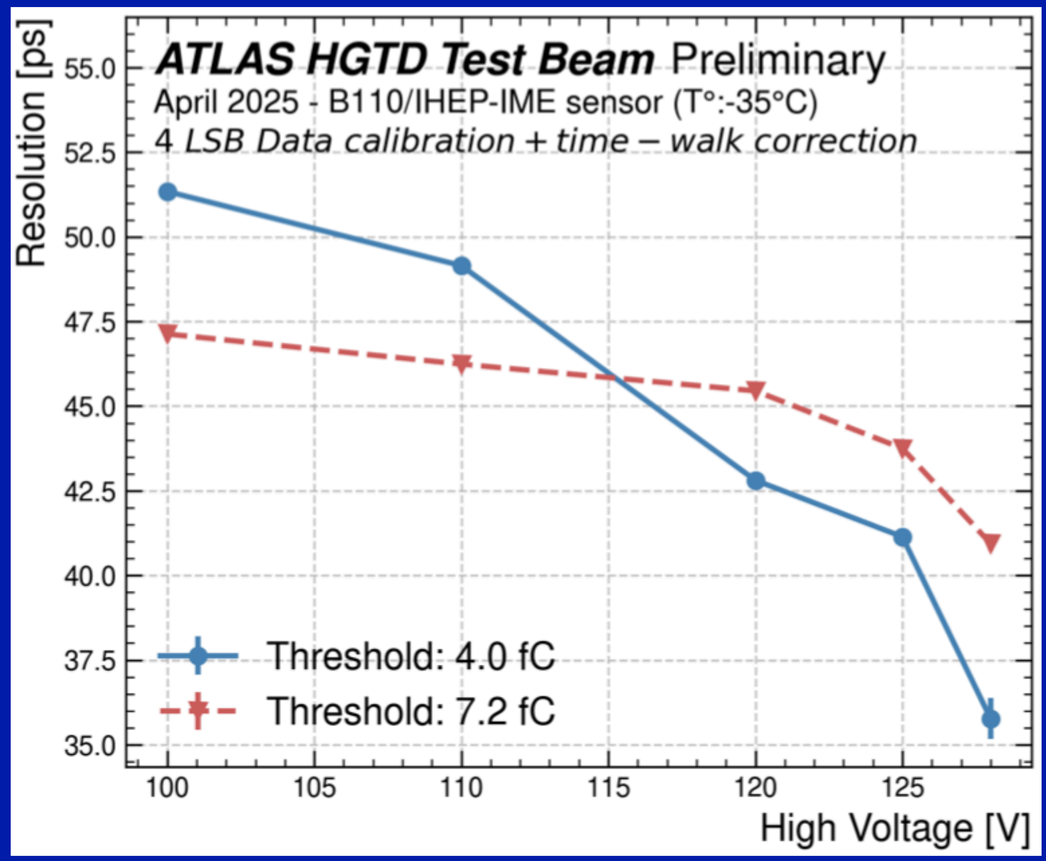
Performance of ALTIROC3 in optimal operating conditions:

– Low temperature (–35 °C), high bias (>120 V), low threshold (4 fC)



$\Delta t = TOA \times LSB - (t_{Clock} - t_{MCP})$



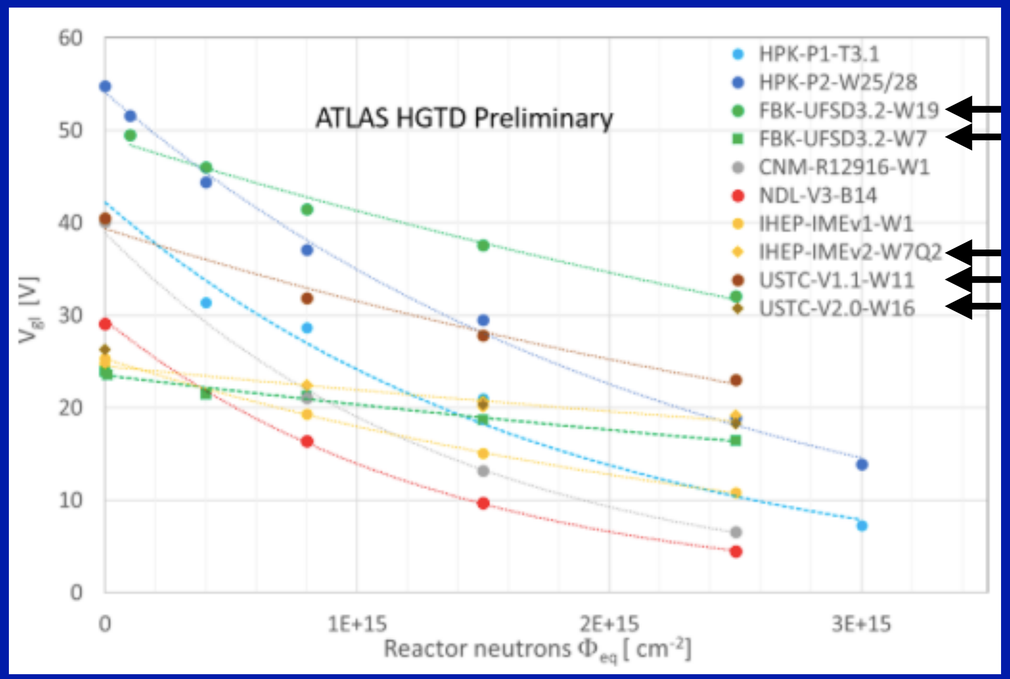
Timing resolution reaches 36 ps

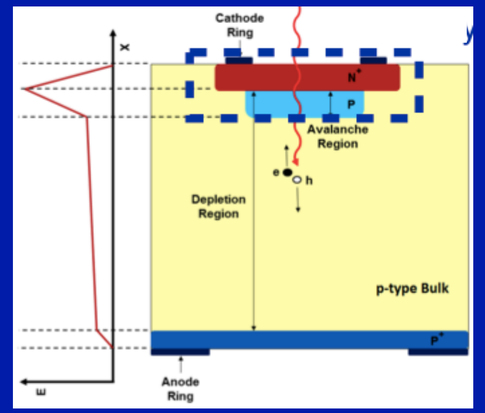
Radiation Hardness

HGTD Public Results

Radiation induces acceptor removal in the p+ gain layer, reducing the electric field and leading to loss of gain

→ Study gain layer depletion voltage, V_{gl}, dependence on fluence: $V_{gl} = V_{gl,0} \times e^{-c\Phi_{eq}}$





From C-V measurements: lowest acceptor removal with carbon-enriched wafers

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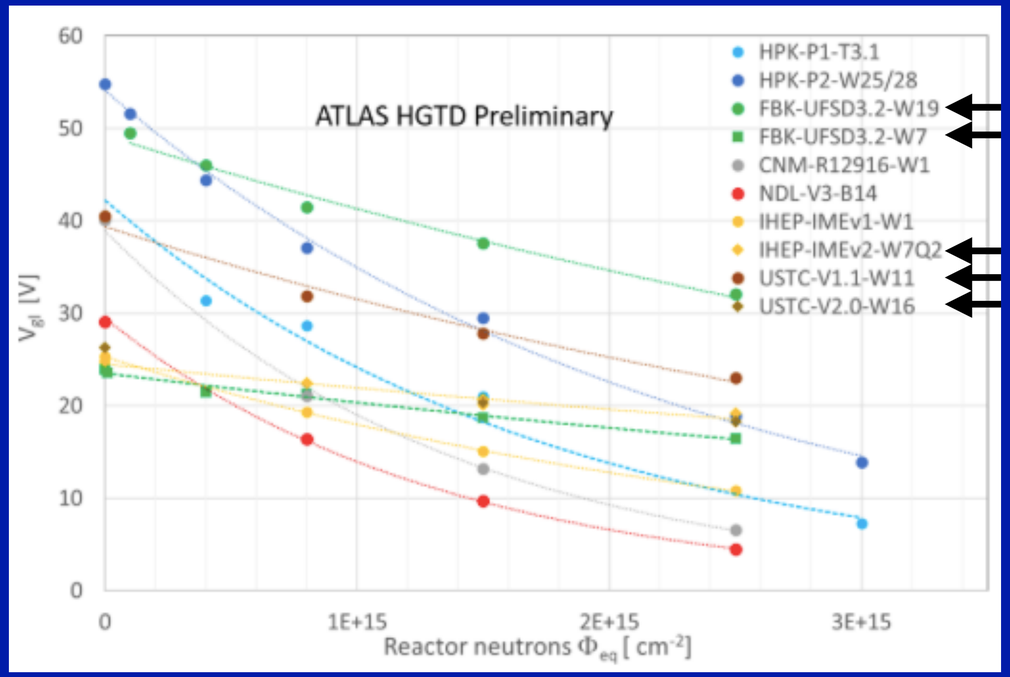
Recover by increasing the bias
- Limit imposed by Single Event Burnout (SEB) effect (local breakdown of electric field)
→ Vmax~550 V for 50 µm thickness



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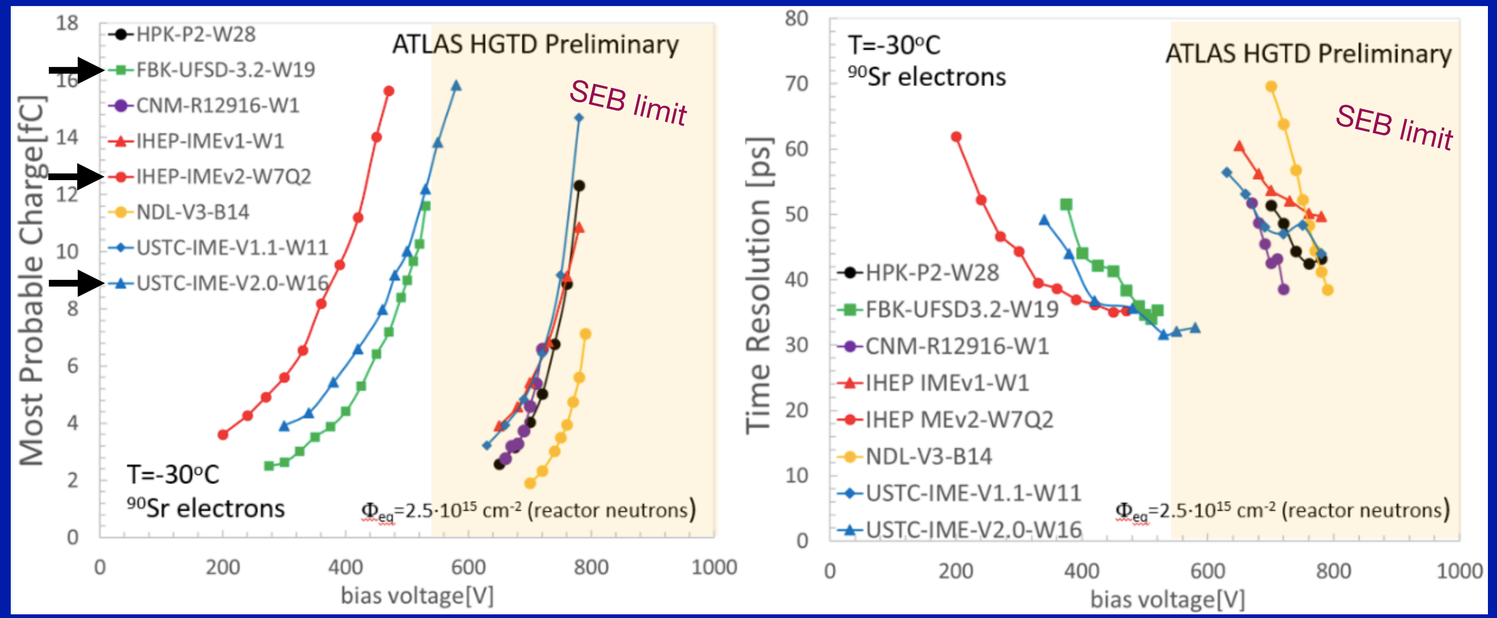


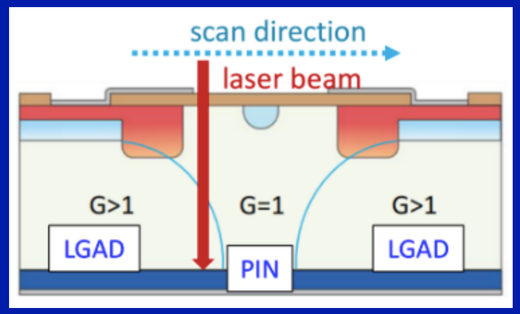
FBK-UFSC-2.3-W19, IHEP-IMEv2-W7Q2, USTC-IME-V2.0-W16 sensors show stable performance at much lower bias voltages than non-carbon enriched wafers

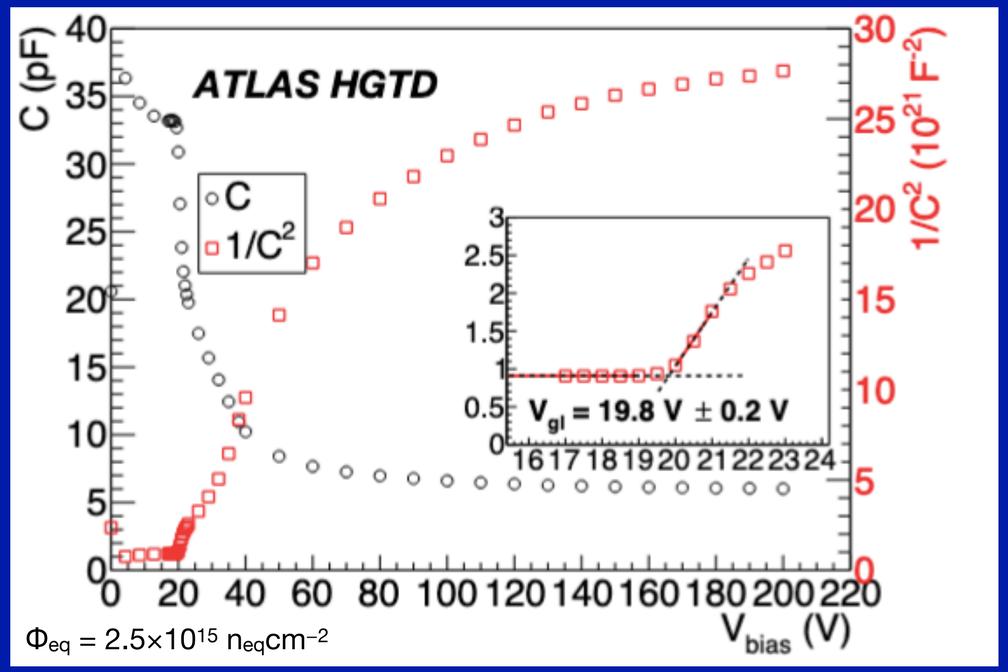
Irradiation Tests - TCT Measurements

arXiv:2509.09187

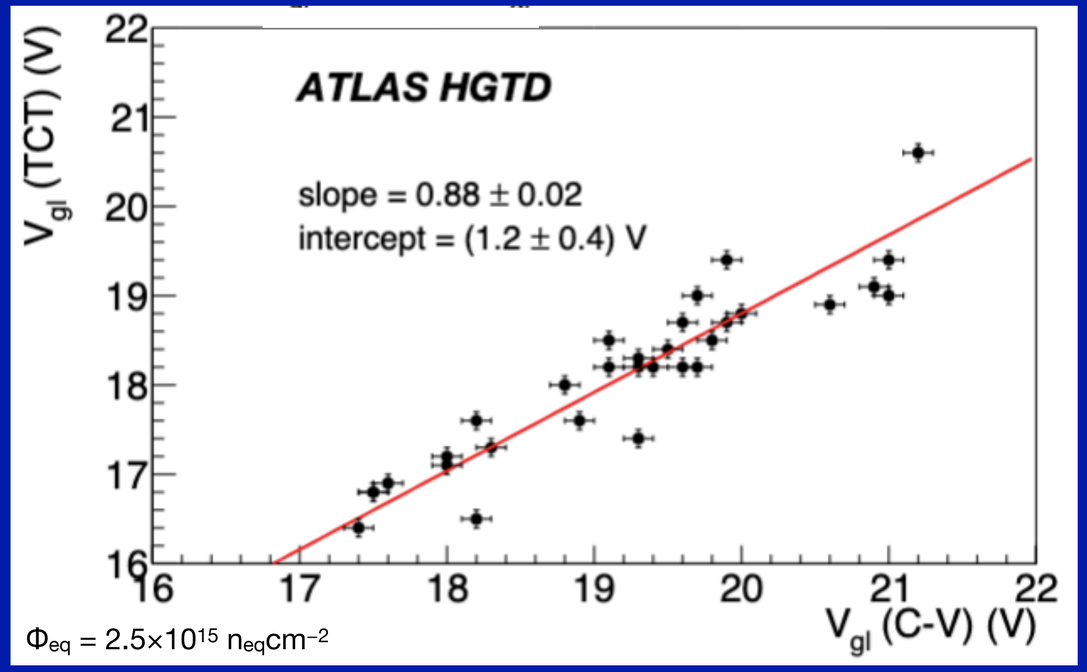
Transition Current Technique - performed in the interface region of two LGAD devices

- V_{gl} extraction
- Gain dependence on bias voltage
- Sensor leakage current
- Effective interpad distance





Inset shows V_{gl} extraction from the intersection of linear fits



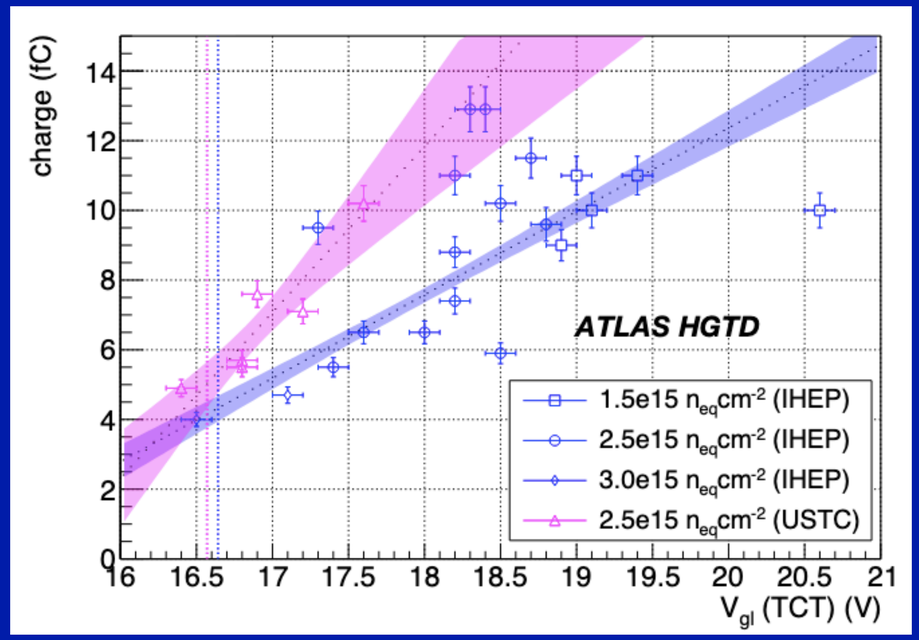
Systematic offset between V_{gl} from TCT and C–V measurements

→Charge-collection vs AC electrical responses

Irradiation Tests - Wafer Acceptance

Correlation between most probable collected charge from ^{90}Sr MIP and V_{gl} for two sensor designs: IHEP and USTC, both from IME

arXiv:2509.09187



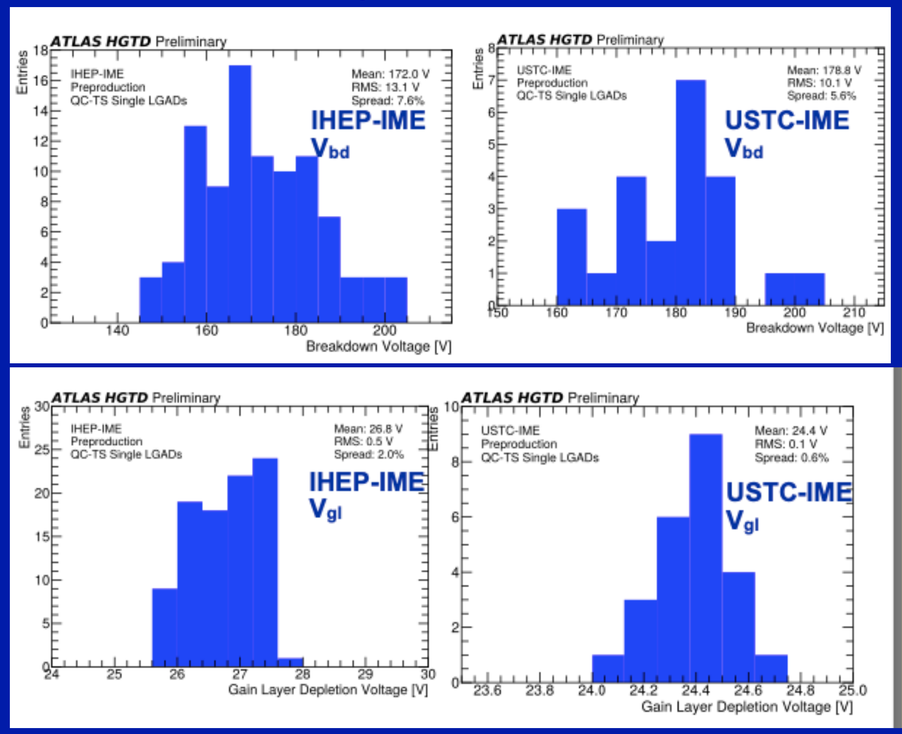
- Several fluences studied: ^{90}Sr data for fluences of 2.5×10^{15} $n_{eq}cm^{-2}$ and above are shown for the operating voltage at the SEB limit of 550 V
- Data for each design is fitted with a linear fit and uncertainty band represents 1σ fit parameter variation
- The wafer acceptance threshold is defined by the point where the fit intersects a charge of 5 fC

QC-TS pre-production results

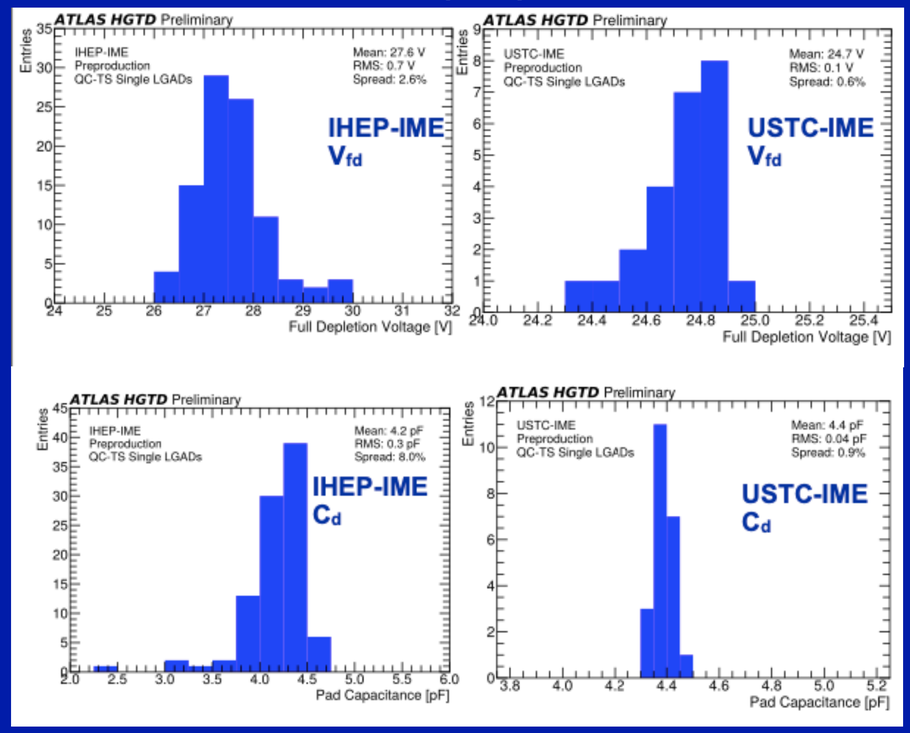
https://indico.cern.ch/event/1386009/contributions/6279120

Measurements on ~10 QC-TS per wafer for IHEP-IME and USTC-IME

Gain layer properties



Substrate properties



Breakdown of single-pad sensor defined as: V @ 500 nA

- V_{bd} spread:
  7.59% for IHEP-IME and 5.64% for USTC-IME → within specs (8%)

Gain layer depletion voltage:

- Specification: 24V<Vgl<55V with spread 2.02% for IHEP-IME and 0.57% for USTC-IME
  All wafers met the criteria

Full-depletion voltage [V_{fd}]:

- Specification < 70 V —> Spread inside specs (<10%) for both designs
- Resistivity of the substrate is larger than 1kΩ*cm

Detector Capacitance [C_d]:

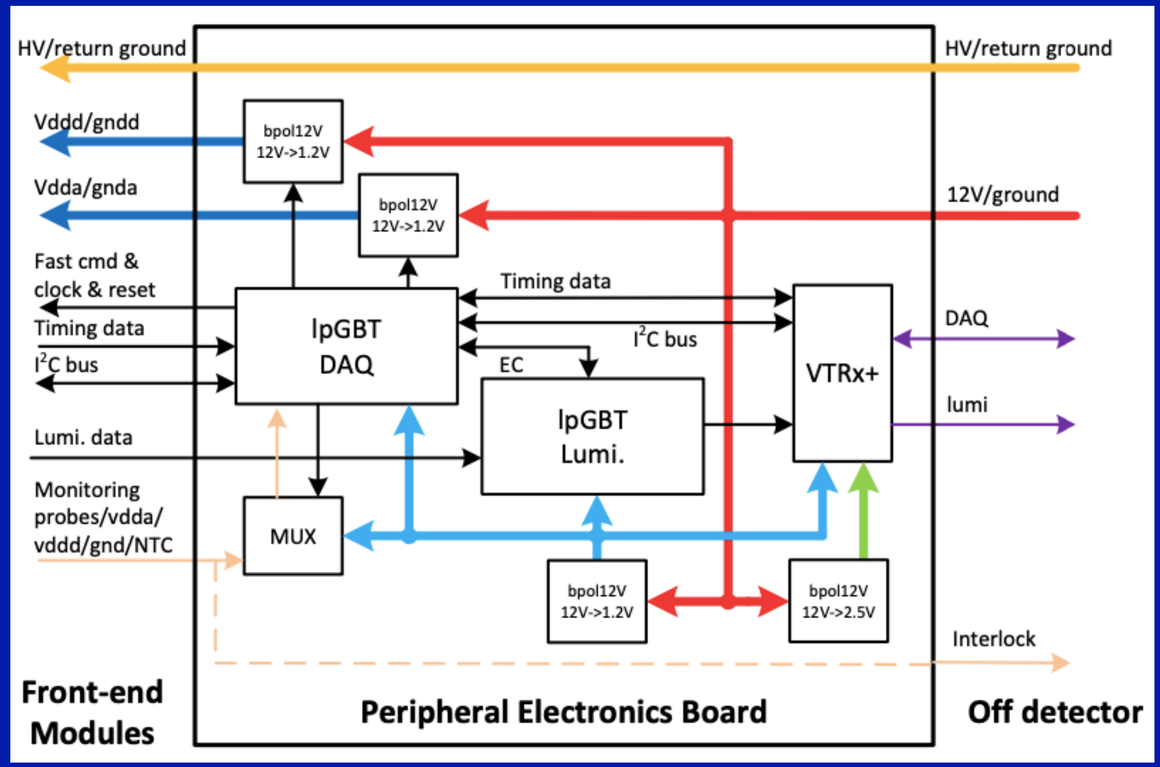
- Specs: < 4.5 pF —> met

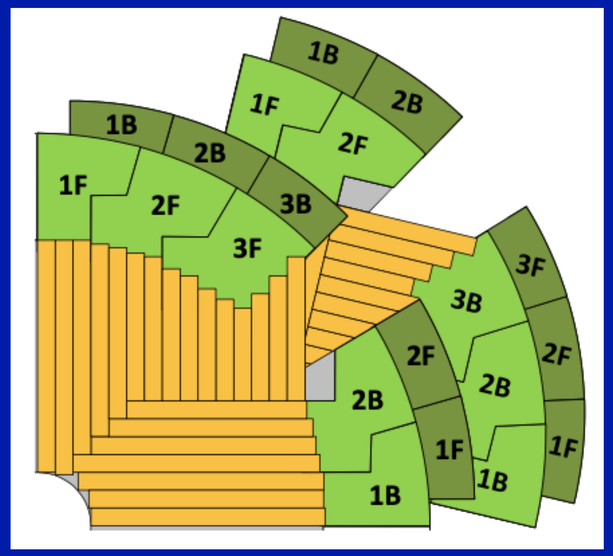
Results consistent within the specifications / expectations

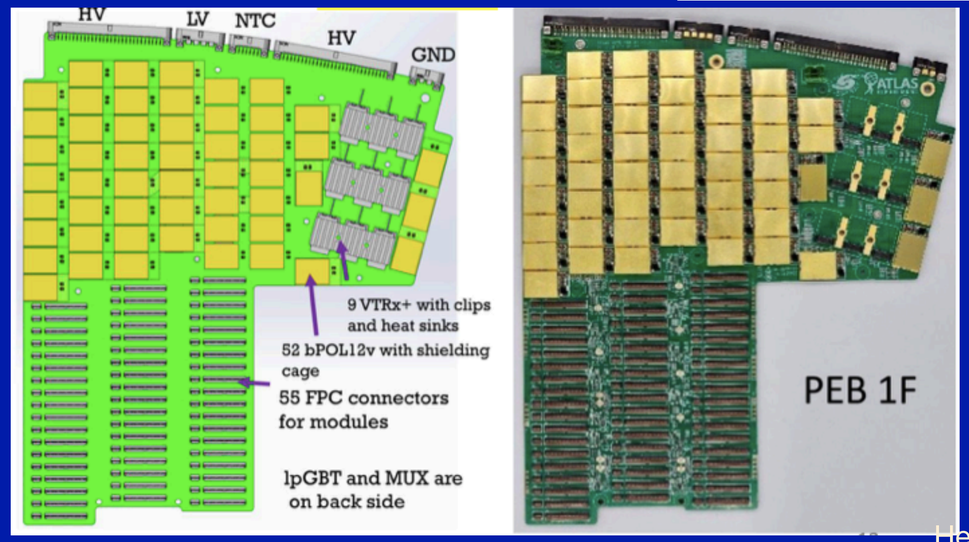
Peripheral Electronics Board (PEB)

- Handles data transmission, LV & HV, monitoring and control
- Main components: lpGBT (data aggregation), VTRx+ (optical), bPOL12V (LV converters), MUX64
- Dedicated data paths for timing and luminosity

- The PEB1F case: 55 FPC, 52 bPol12V, 12 lpGBT, 9 VTRx+, 9 MUX64 within 9.7 mm thickness
- 22 layer PCB, with HDI micro via and VIPPO techniques, High speed, low loss multi-layer material for impedance control







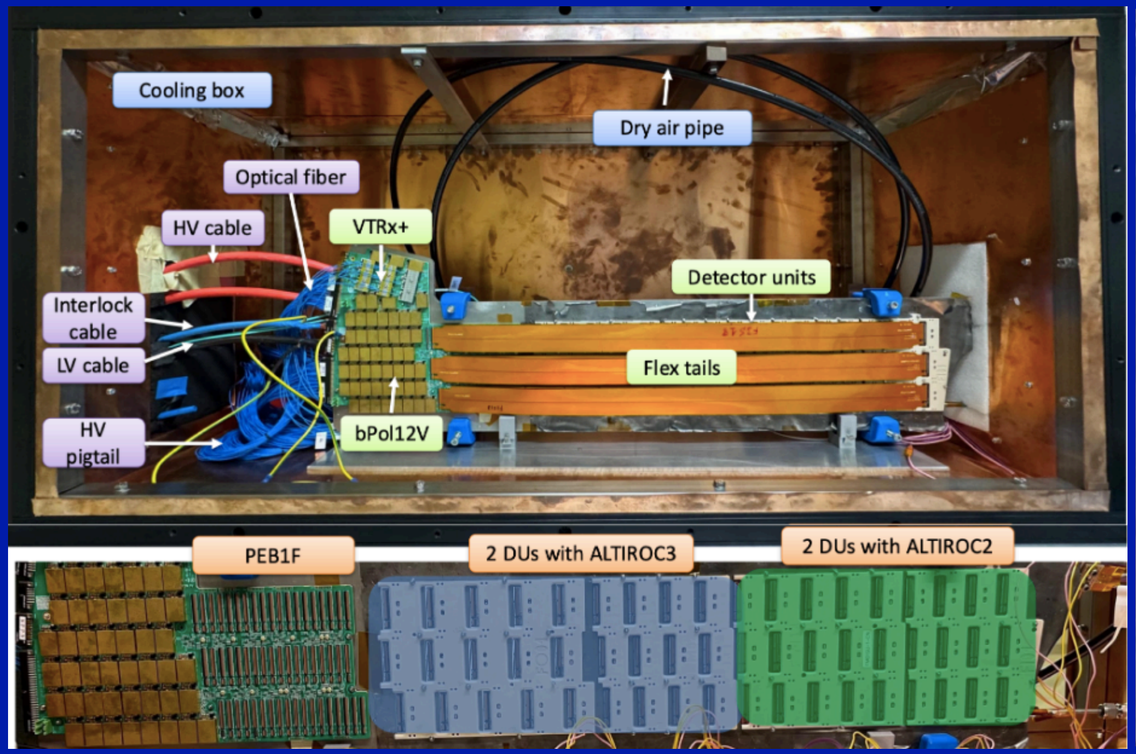
... the most difficult boards manufactured in HEP projects...,

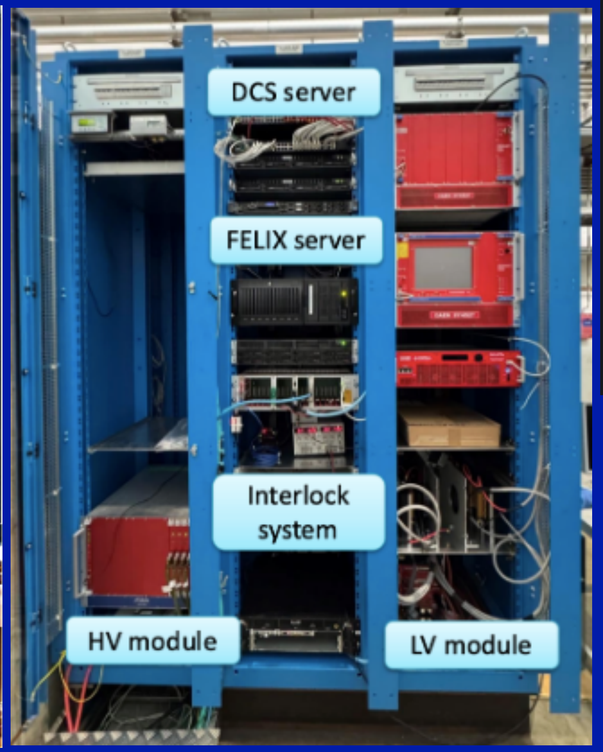
ATLAS P2UG Review committee

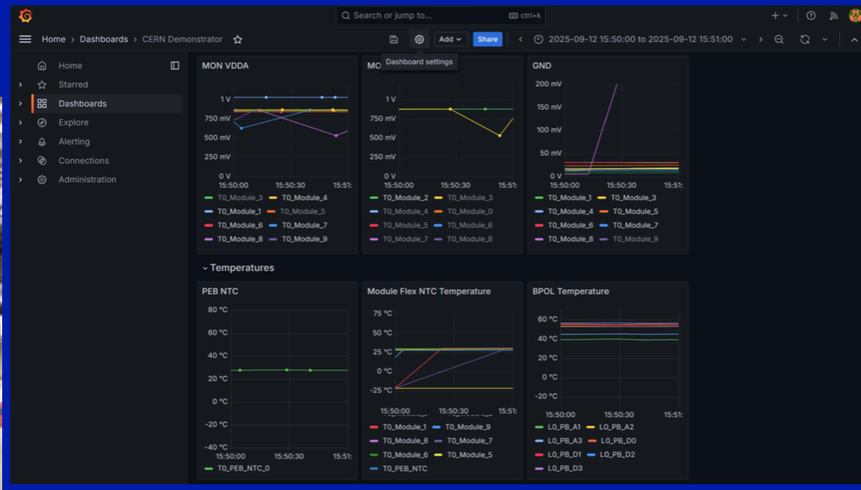
The Demonstrator

HGTD Public Results

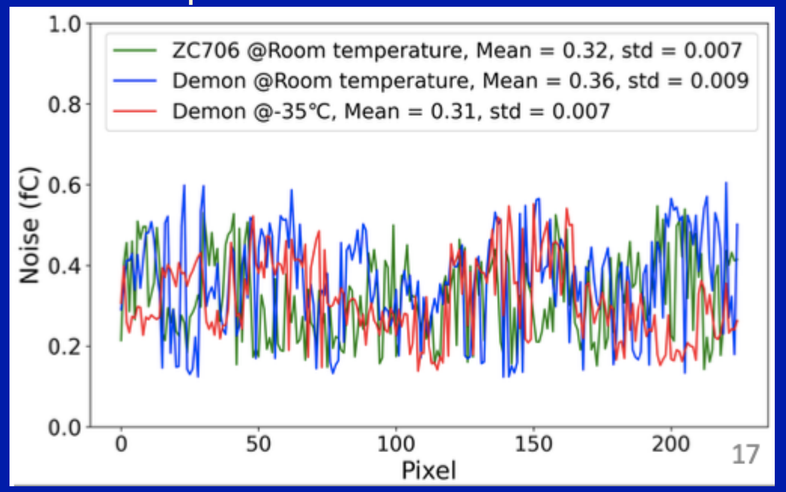
- Full chain and detector level test with all components.
- One PEB (1F) connecting 54 modules loaded on 4 support units
- LV + HV + PEB + ALTIROC DUs + cooling + DCS&Interlock in a cold box (= -30 C)
- Allows system-level testing of all components







Noise comparison demonstrator/test bench

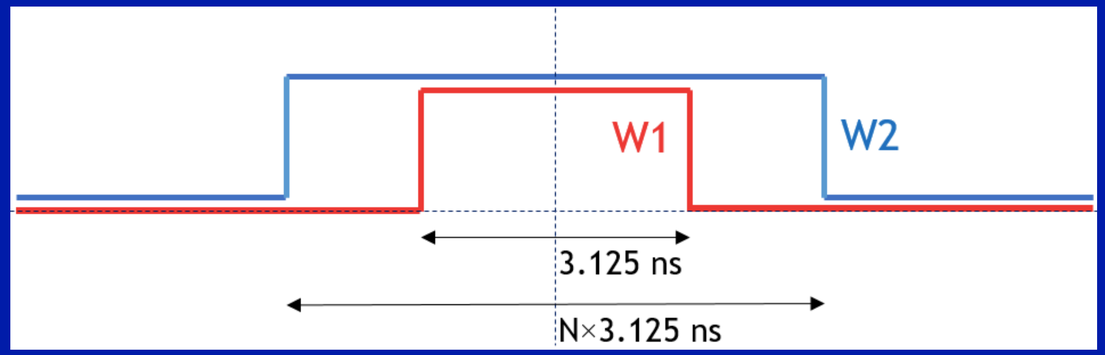


A Module-0 construction (fully integrated prototype consisting in 1/4 disk) will follow in 2026

Luminosity measurement

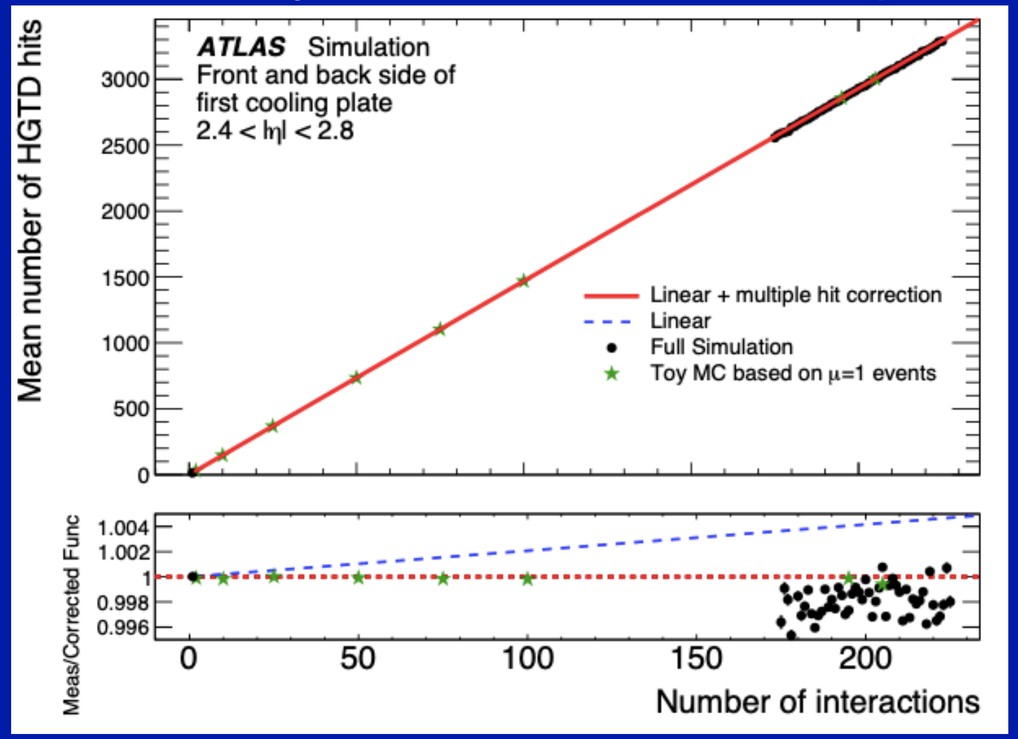
The high granularity of HGTD ensures an occupancy less than 10%
→ excellent linearity between the average number of hits and ⟨μ⟩ over the full range of luminosity expected at the HL-LHC

- ALTIROC in $2.4 < |\eta| < 2.8$ (outer ring) provides per-sensor occupancy per bunch-crossing with 1% accuracy
- Hit counting at 40 MHz
- Dedicated readout chain, independent of the trigger and timing data



Windows of counting hits centred at the bunch-crossing time
W2 for background correction

Linearity of $\langle n_{hits} \rangle$ as a function of ⟨μ⟩



Summary - HGTD performance and status

Per-track timing resolution: 30–50 ps in the forward region, meeting HGTD design targets for precise time tagging of tracks.

It will allow:

- strong suppression of pileup tracks and jets, improving event reconstruction in high-luminosity conditions.
- independent bunch-by-bunch luminosity measurement within 1% precision.

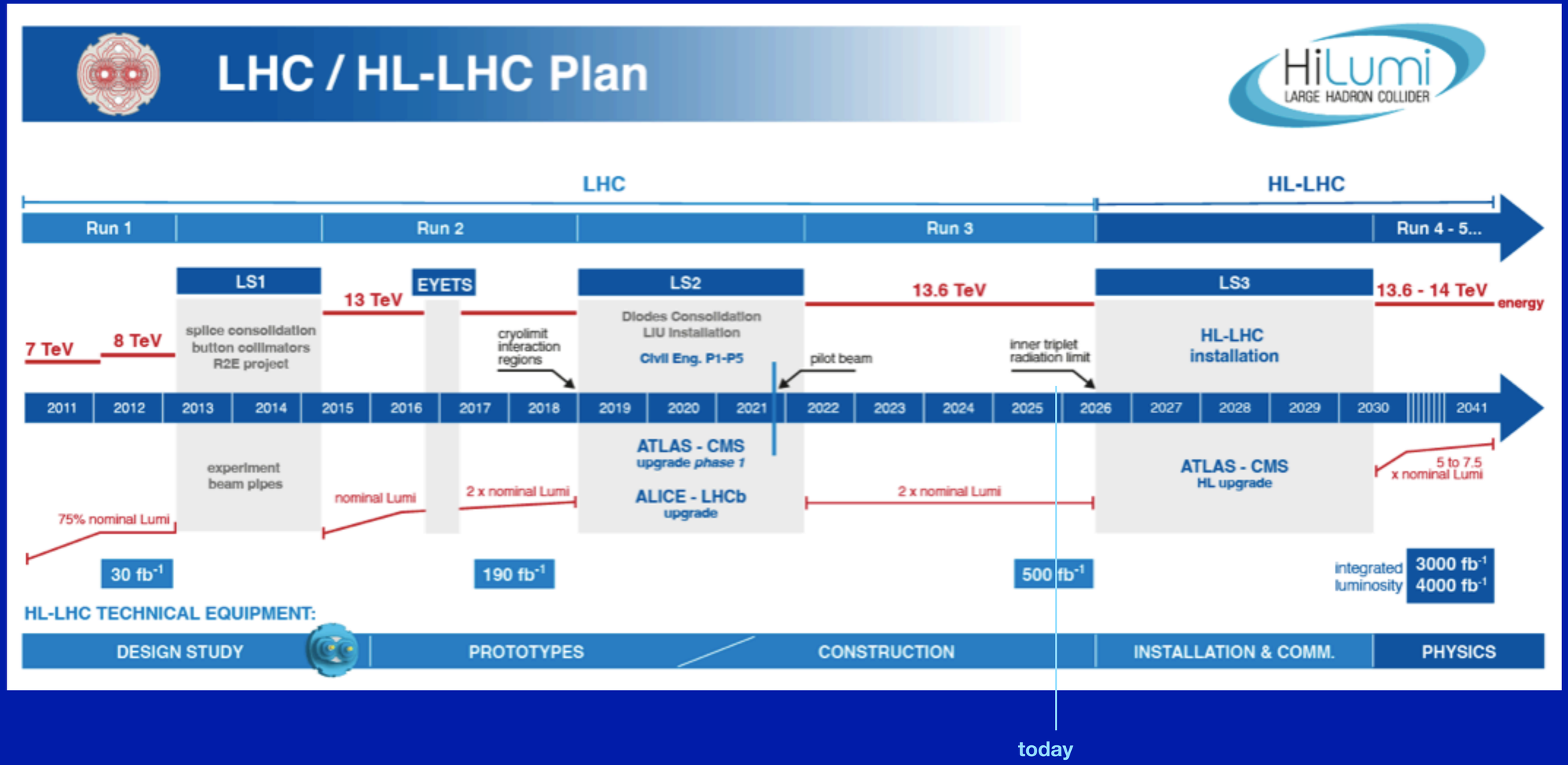
Project status:

- The HGTD is transitioning from R&D to production, with several critical components already under QA/QC.
- A busy construction and integration is ongoing, as we move toward Module0 and full detector assembly and installation.

……Exciting times ahead!

Backup

HL-LHC Roadmap



ATLAS Phase-2 upgrade

Trigger and Data Acquisition:

- First level tigger at 1 MHz, 5.2 TB/s, 10 μs latency
- Event Filter 10 kHz, ~52 GB/s

Electronics upgrade:

- On/Off-detector electronics for Calorimeters and Muon systems
- 40 MHz readout and finer trigger segmentation

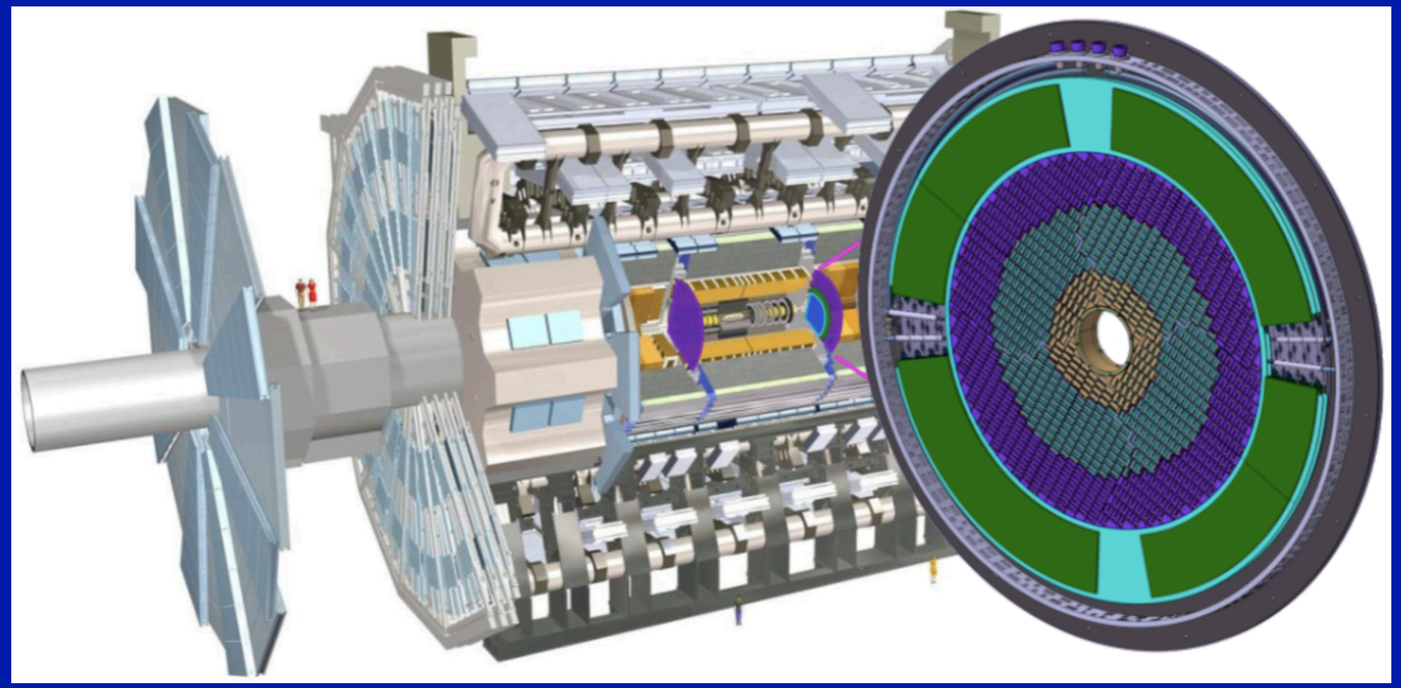
New Inner Tracker Detector:

- All Silicon
- 9 layers for |η|<4
- Reduced material budget
- Finer segmentation

T. Koffas' talk

New muons chambers:

- Inner barrel with new RPCs, sMDTs and TGCs
- Improves momentum resolution, trigger efficiency and fake rejection

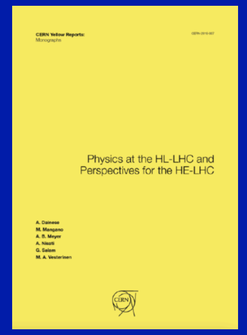


High Granularity Timing Detector (HGTD):

- Precision timing using Silicon Low Gain Avalanche Detectors (LGAD)
- Improves pileup separation and measures luminosity

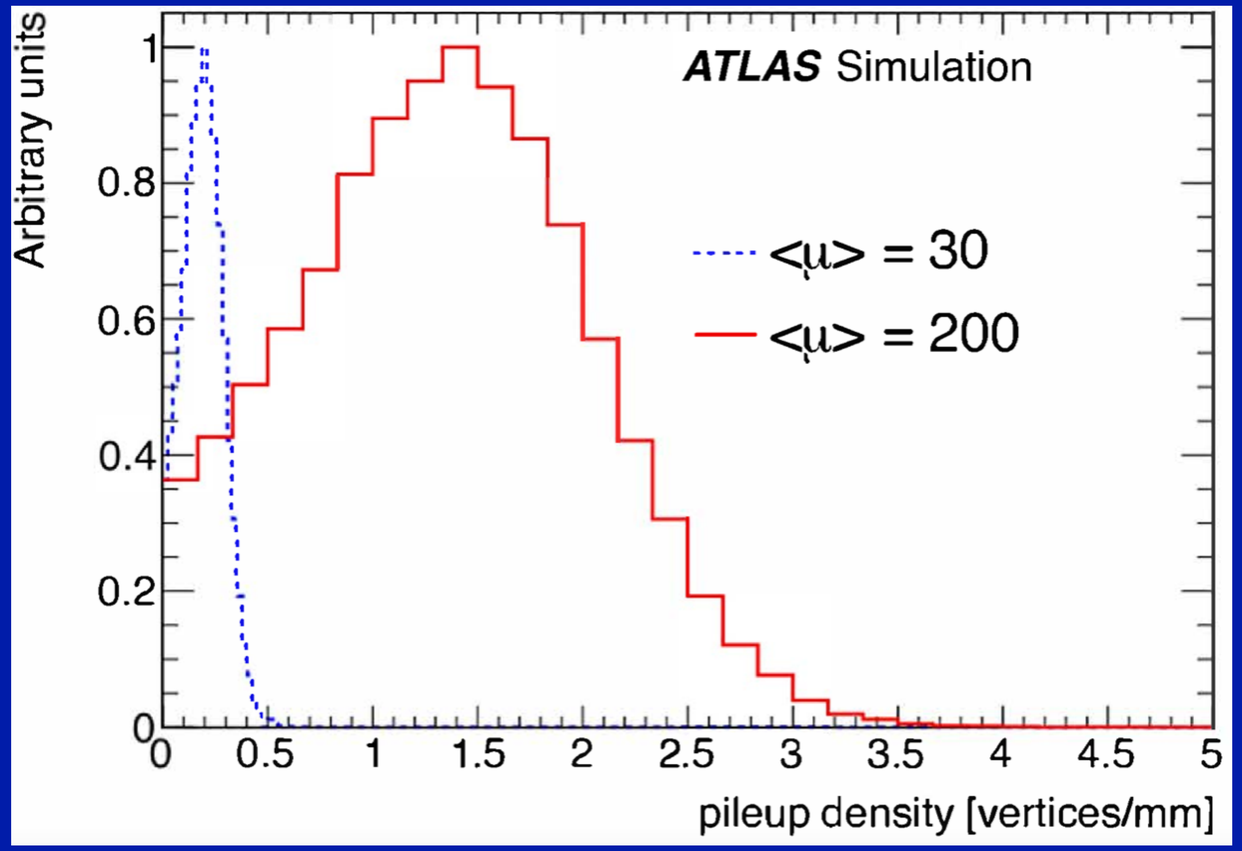
Additional upgrades:

- Luminosity detectors (1% precision),
- Zero degree calorimeter for Heavy Ion physics

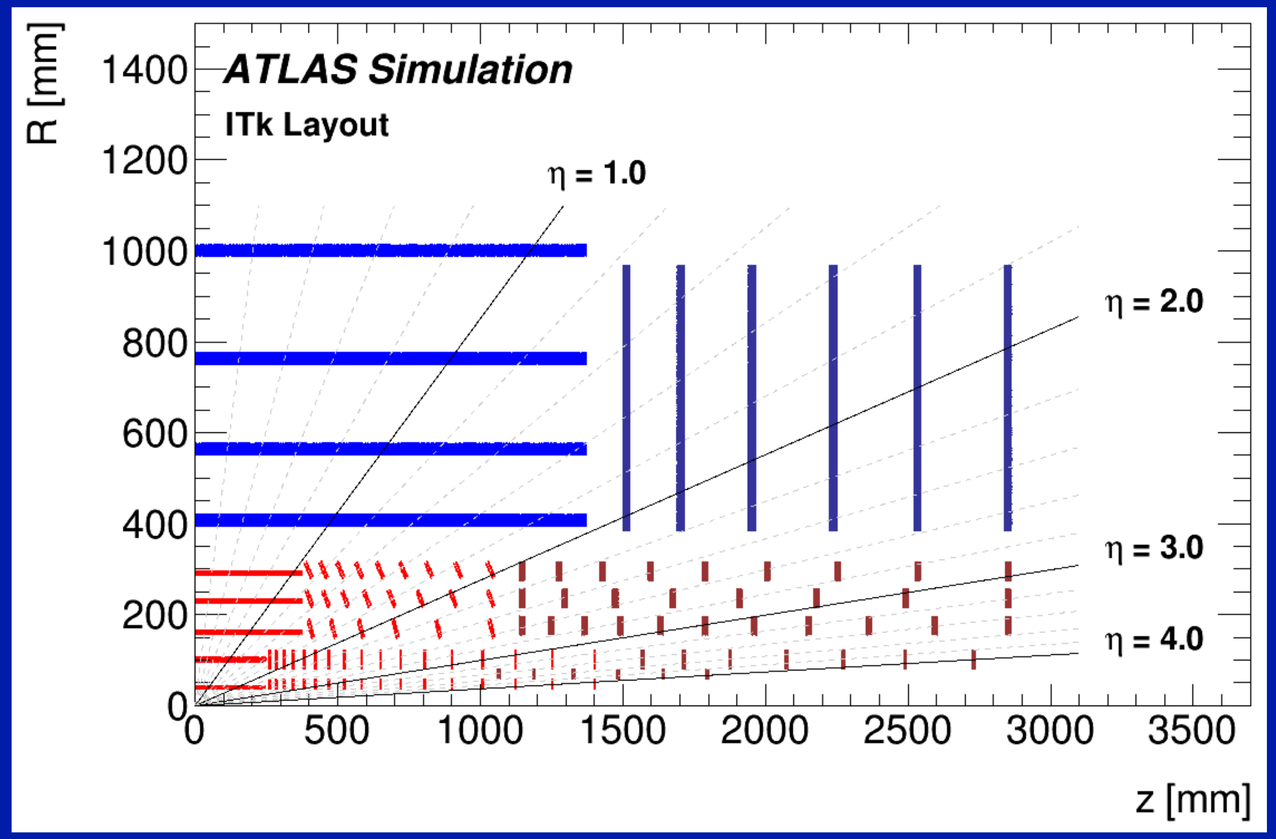


HL-LHC - vertex density and ITk acceptance

HGTD TDR Public Plots

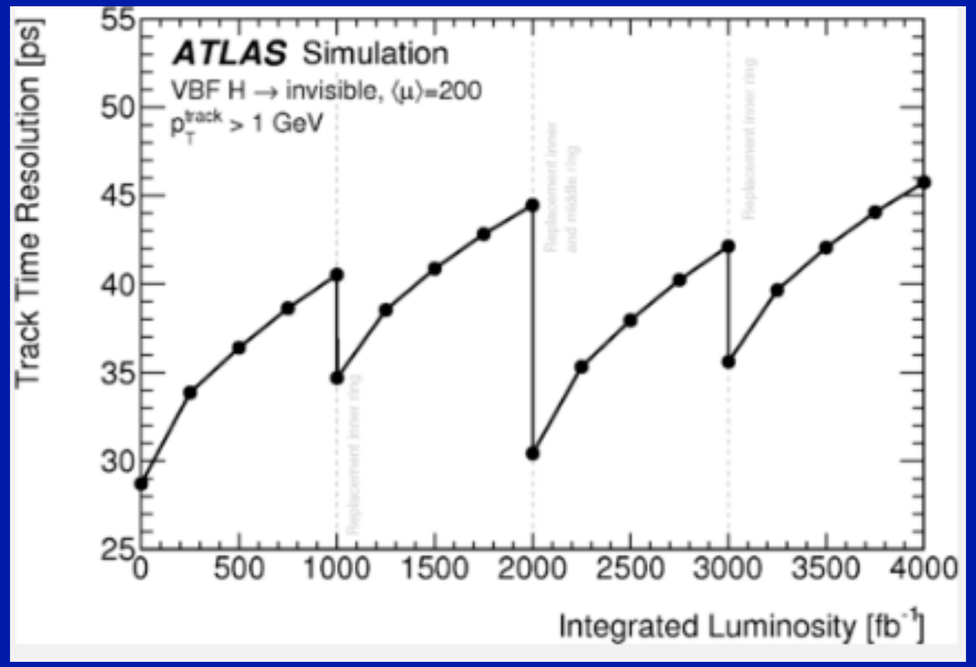


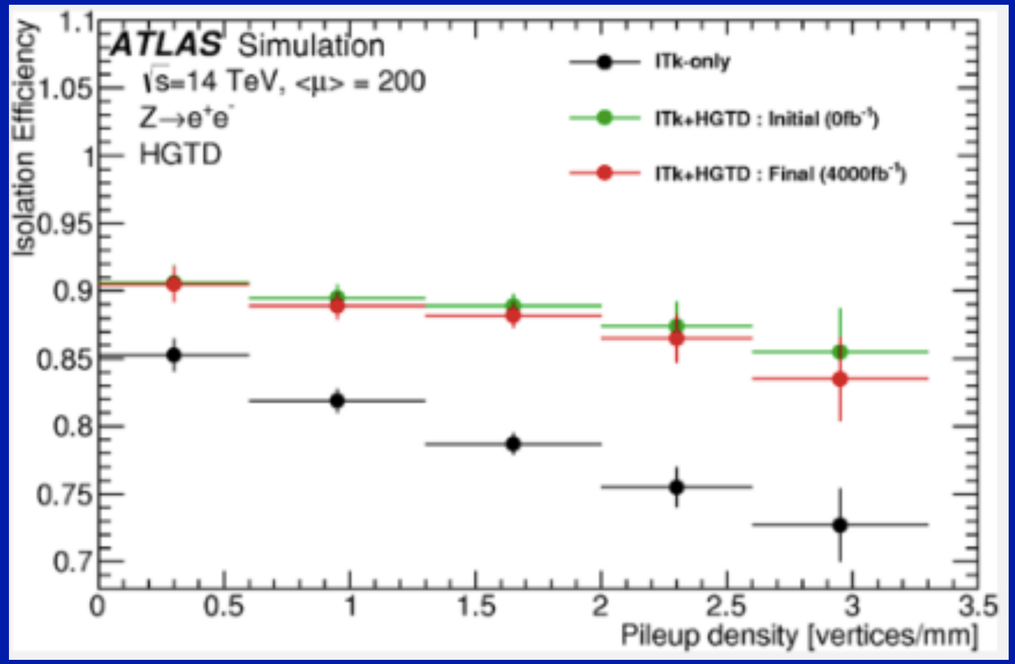
Vertex density in the z-axis



The active elements of the barrel and end-cap ITk Strip detector are shown in blue, for the ITk Pixel detector the sensors are shown in red for the barrel layers and in dark red for the end-cap rings.

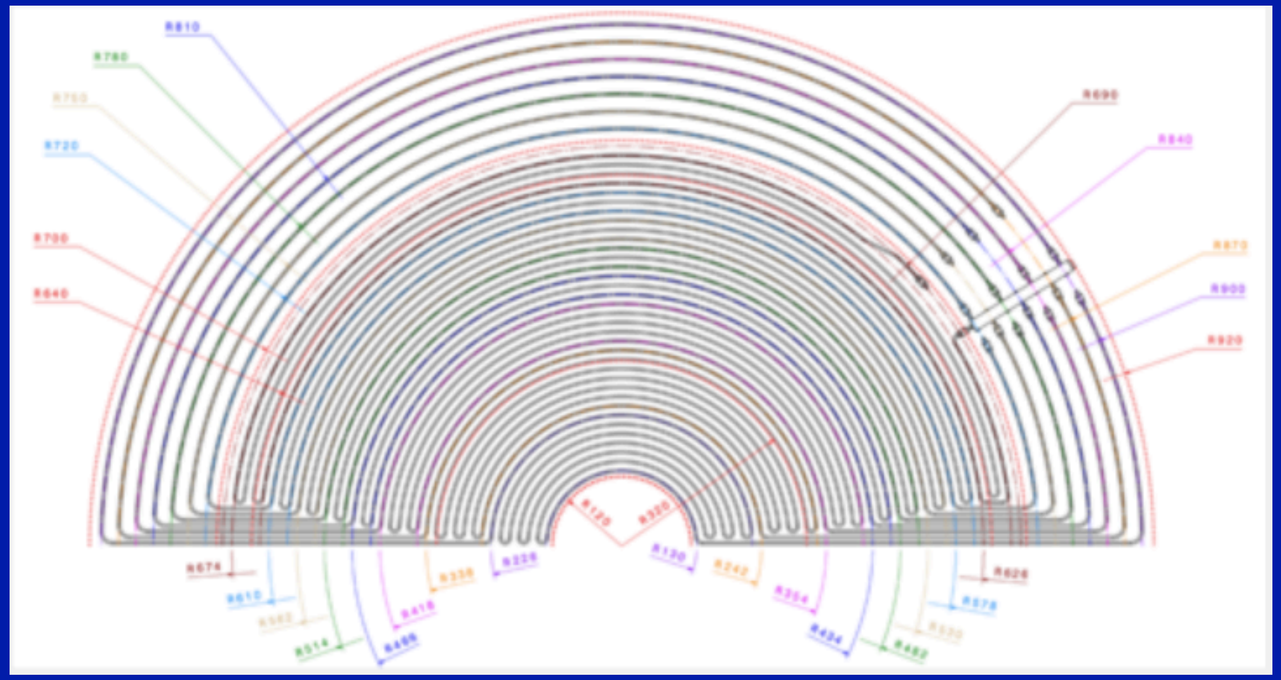
Physics performance with HGTD

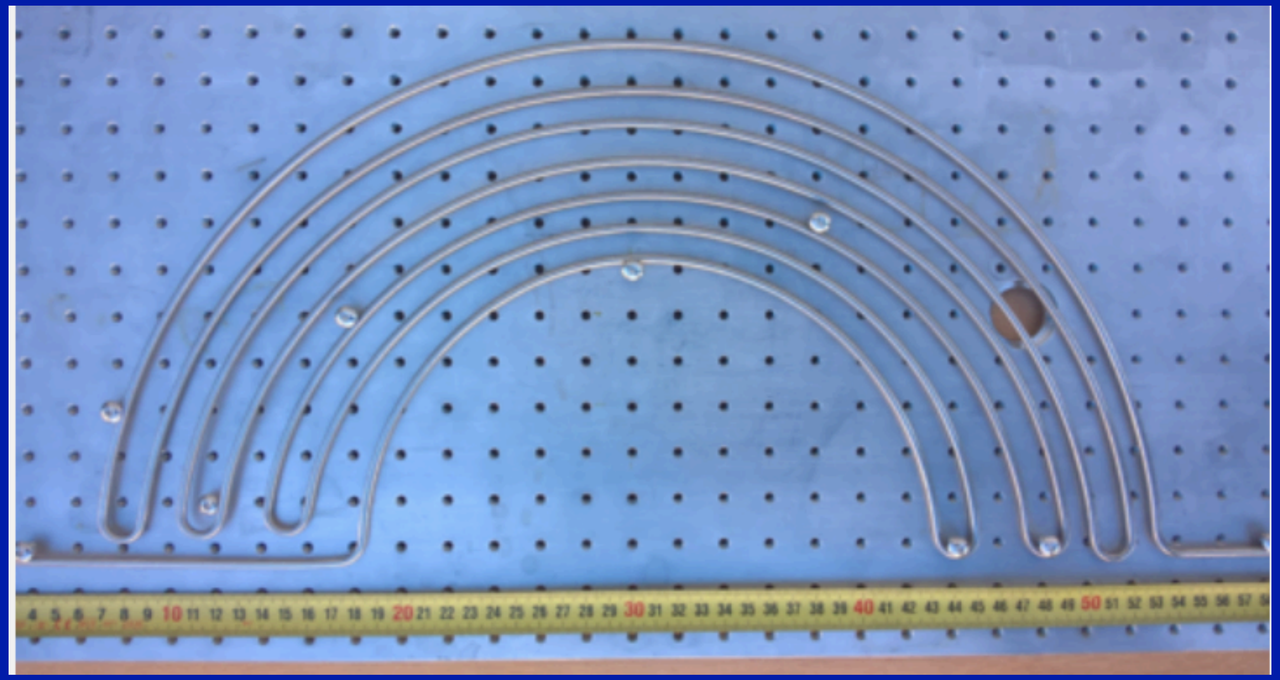




Cooling

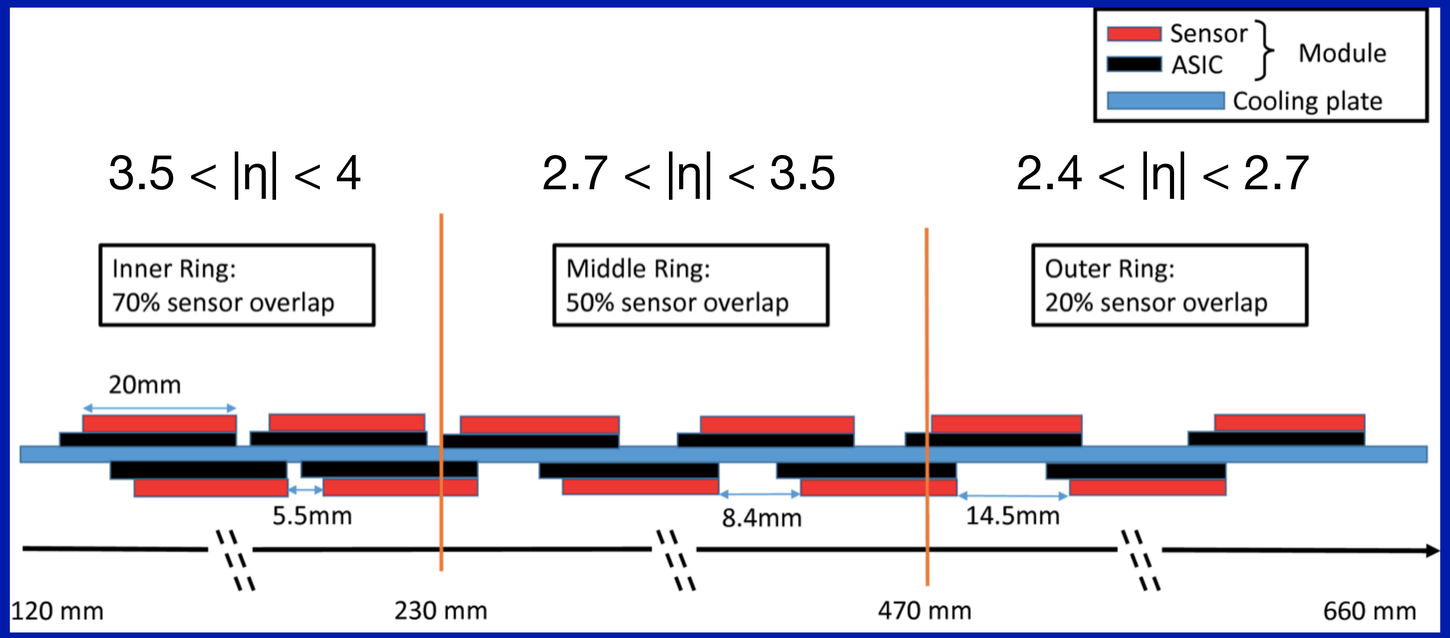
HGTD TDR Public Plots



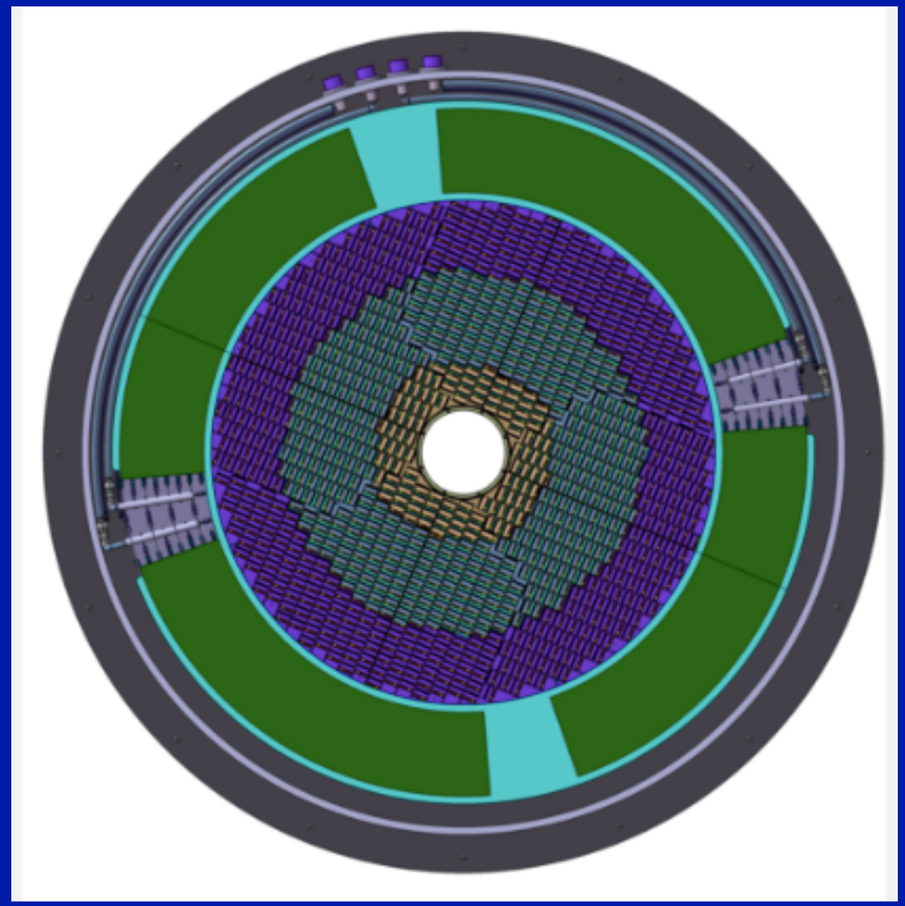


overlap between the modules on the front and back disks

HGTD TDR Public Plots



Replaced every 1000 fb^{-1} Replaced every 2000 fb^{-1} 4000 fb^{-1}



Quality-Control Test Structures (QC-TS)

Monitored process parameters during the production

QC Device	Parameter	Description	Technique used
Single LGAD	Vgl	Gain layer depletion voltage	C-V
	Vfd	Full depletion voltage of the device	C-V
	I@Vfd	Current at full depletion voltage	I-V
	Vbd	Device breakdown voltage	I-V
	Cpad	Electrode capacitance	C-V
PIN	Vbd	Breakdown Voltage	I-V
	Ileak	Leakage Current	I-V
MOS	tox	Oxide Thickness	C-V
	Vfb	Flatband Voltage	C-V
VDP NA	R_sheet	Sheet Resistance for N implantation	I-R
VDP PS	R_sheet	Sheet Resistance for P implantation	I-R
VDP Al	R_sheet	Sheet Resistance for Aluminum	I-R

https://indico.cern.ch/event/1386009/contributions/6279120