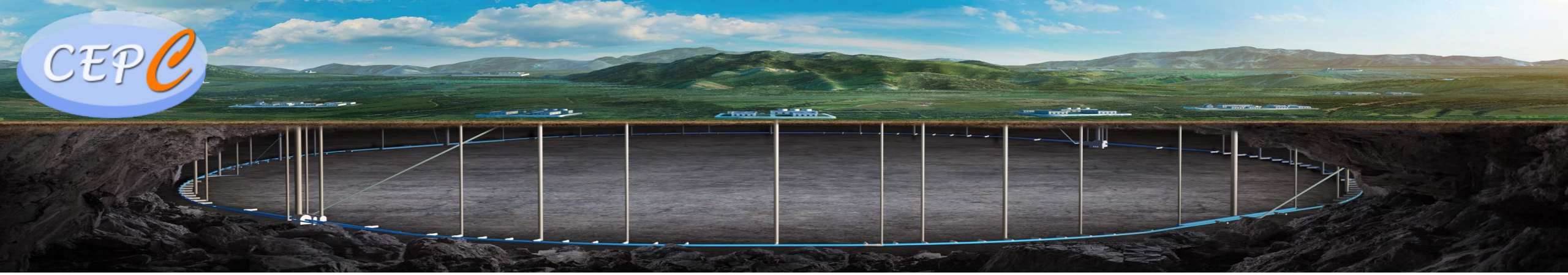

Overview of the CEPC Vertex Detector

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(On behalf of the CEPC vertex detector group)

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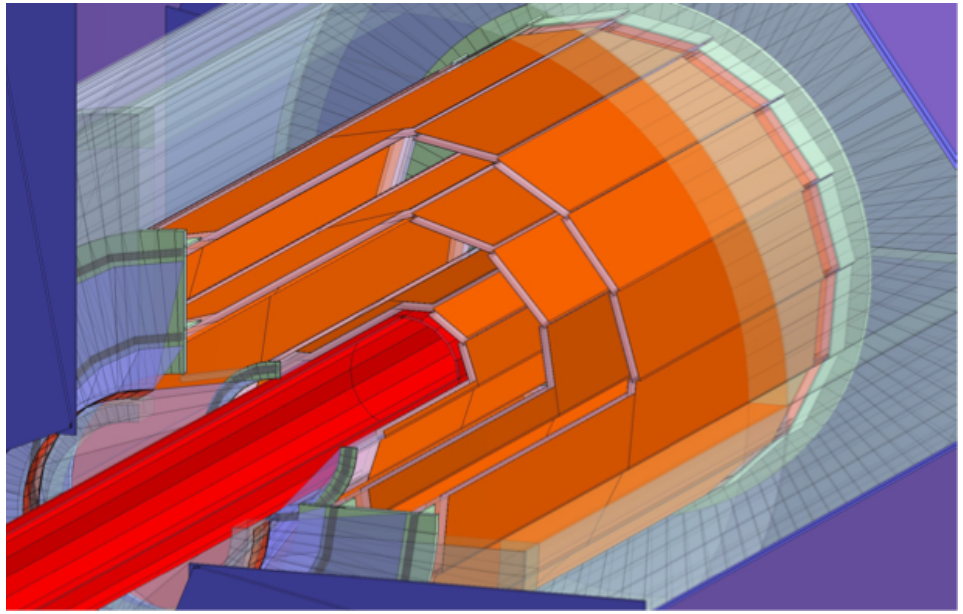
Chinese Academy of Sciences

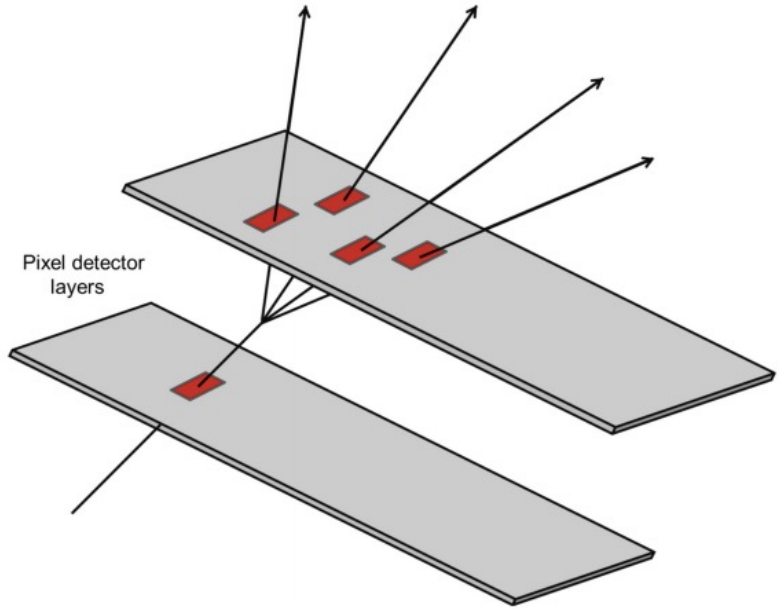
Content

- Introduction
- Requirements
- Technology survey and our choices
- R&D efforts and results
- Detailed design including electronics, cooling and mechanics
- Readout electronics
- Performance from simulation
- Research team and working plan
- Summary

Introduction: vertex detector

- Motivation:
  - Aim to optimize impact parameter resolution and vertexing capability
  - Key detector for Higgs physics (H → cc and H → bb …)
  - which is an important goal for for future lepton collider (eg: CEPC …)





Vertex Requirement in CEPC ref-TDR design

– Inner most layer (b-layer) need to be as close to beam pipe as possible
  - **Challenges:** b-layer radius (11mm) is smaller compared with ALICE ITS3 (18mm)

CEPC Technical Design Report -- Reference Detector:
https://arxiv.org/abs/2510.05260

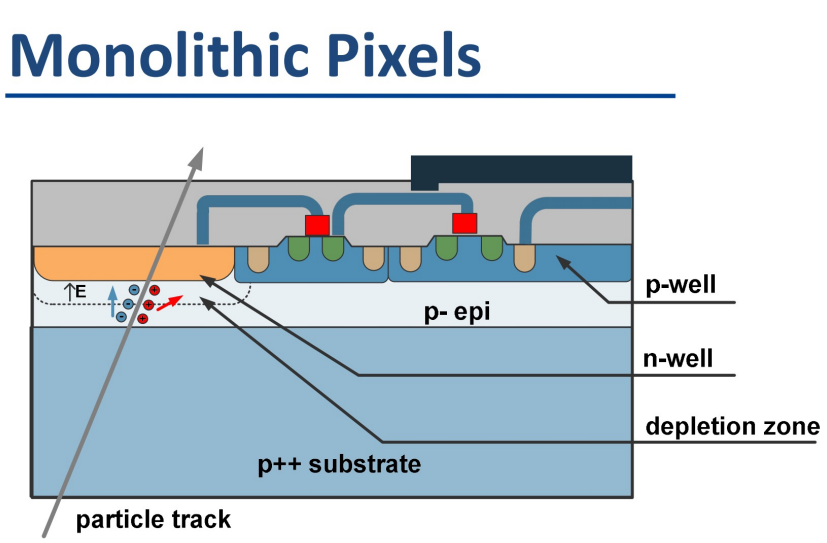
Table 4.2: Vertex Detector Design Parameters

Parameter	Design
Spatial Resolution	~ 5 μm
Detector material budget	$\sim 0.8\% X_0$
First layer radius	11.1 mm
Power Consumption	< 40 mW/cm^2 (air cooling requirement)
Time stamp precision	100 ns
Fluence	$\sim 2 \times 10^{14}$ Neq/cm^2 (for first 10 years)
Operation Temperature	~ 5 °C to 30 °C
Readout Electronics	Fast, low-noise, low-power
Mechanical Support	Ultralight structures
Angular Coverage	$\lvert\cos\theta\rvert < 0.99$

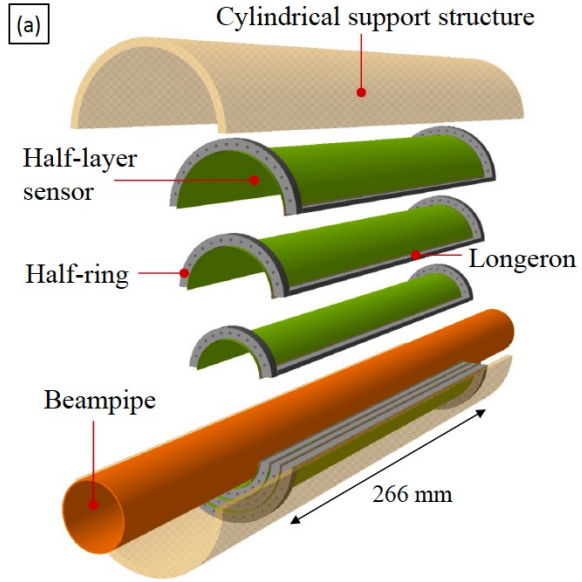
Technology for CEPC Reference TDR

- Vertex detector Technology selection
  - Baseline: based on curved CMOS MAPS (Inspired by ALICE ITS3 design [1])
    - Advantage: 2~3 times smaller material budget compared to alternative (ladder)
  - Alternative: Ladder design based on CMOS MAPS

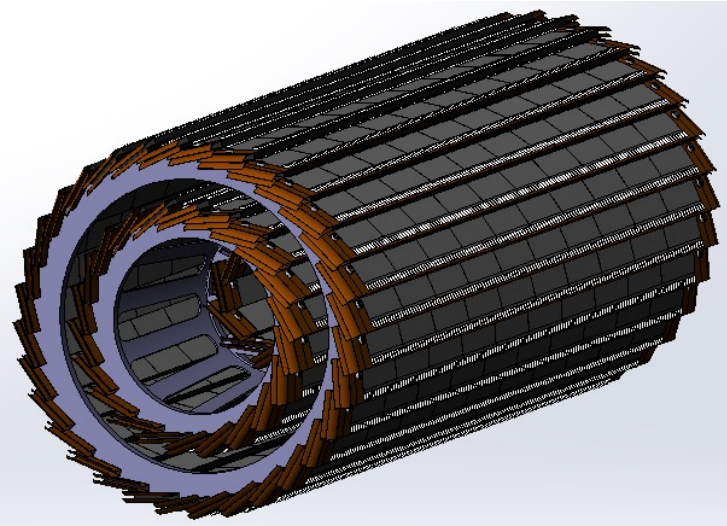
Monolithic active Pixel Sensor (MAPS)



Baseline: curved MAPS



Alternative: ladder based MAPS



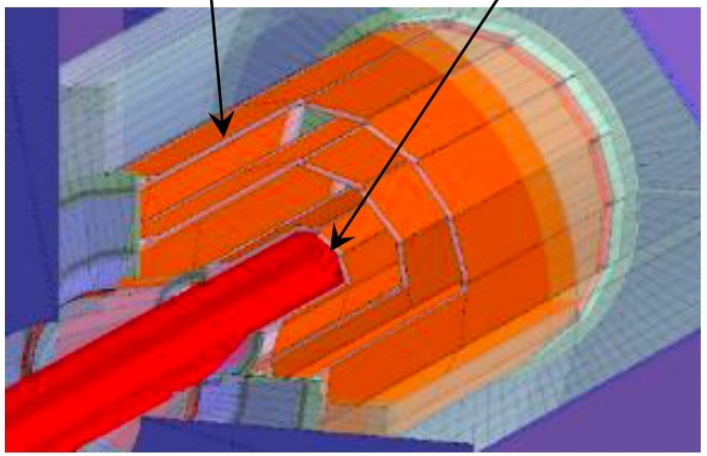
[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

R&D status and final goal

Key technology	Status	CEPC Final goal
CMOS chip technology	Full-size chip with 180 nm CIS (TaichuPix-3)	65 nm CIS
Detector integration	Detector prototype with ladder design	Detector with bent silicon design
Spatial resolution	4.9 μm	3-5 μm
Detector cooling	Air cooling with 1% channels (24 chips) on	Air cooling with full power
Bent CMOS silicon	Bent Dummy wafer radius ~12 mm	Bent final wafer with radius ~11 mm
Stitching	11×11 cm^2 stitched chip with Xfab 350 nm CIS	65 nm CIS stitched sensor

Silicon Pixel Chips for Vertex Detector

2 layers / ladder R_{in}~16 mm



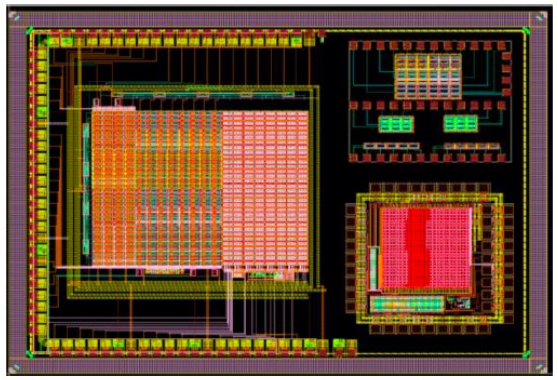
Goal: σ(IP) ~ 5 μm for high P track

CDR design specifications

- **Single point resolution ~ 3μm**
- **Low material (0.15% X_0 / layer)**
- **Low power (< 50 mW/cm²)**
- **Radiation hard (1 Mrad/year)**

Silicon pixel sensor develops in 5 series: JadePix, TaichuPix, CPV, Arcadia, COFFEE

Develop **COFFEE** for a CEPC tracker using SMIC 55nm HV-CMOS process

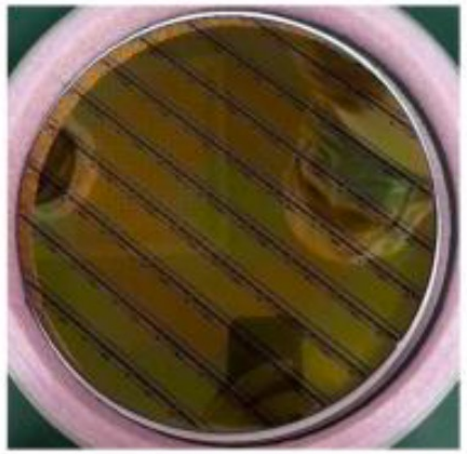


JadePix-3 Pixel size ~16×23 μm²

Tower-Jazz 180nm CiS process
Resolution 5 microns, 53mW/cm²

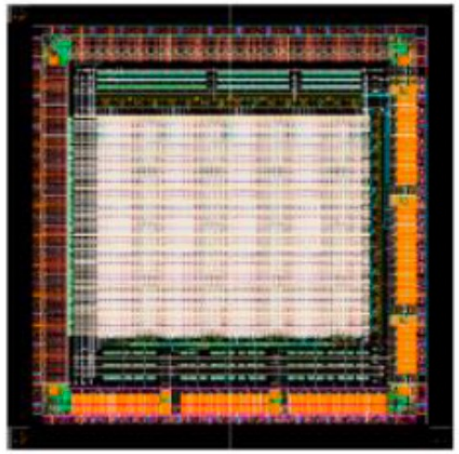
MOST 1

TaichuPix-3, FS 2.5x1.5 cm²
25×25 μm² pixel size

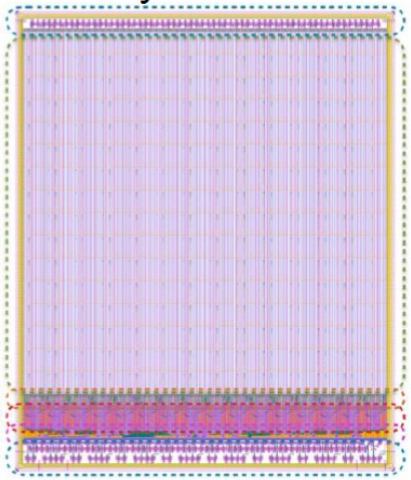


MOST 2

CPV4 (SOI-3D), 64×64 array
~21×17 μm² pixel size

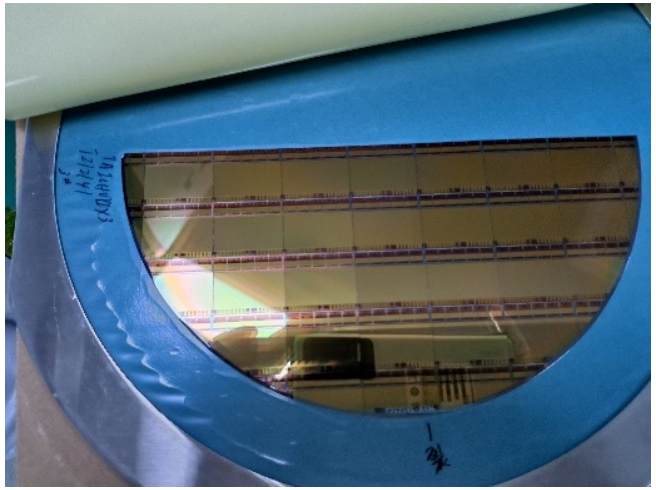


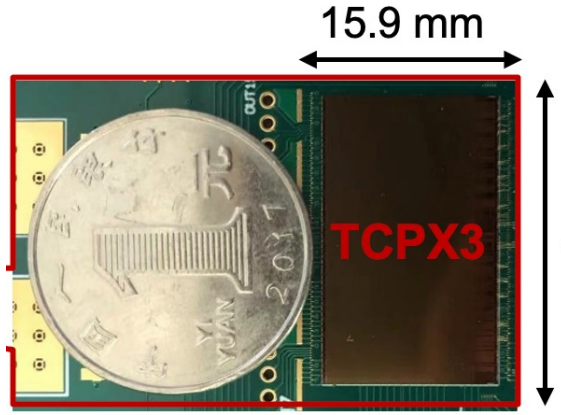
Arcadia by Italian groups for IDEA vertex detector
LFoundry 110 nm CMOS



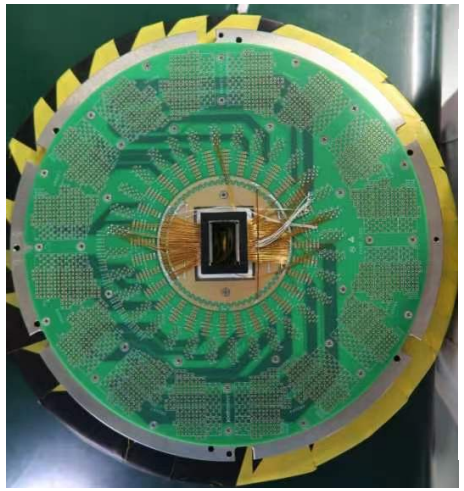
R&D efforts: Full-size TaichuPix3

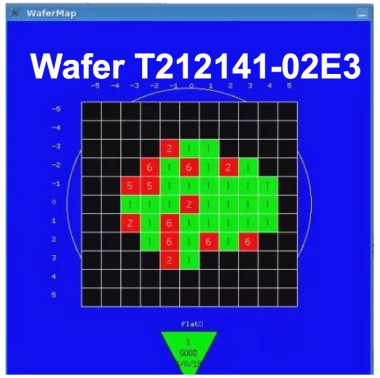
- Full size CMOS chip developed, 1st engineering run
  - 1024×512 Pixel array, Chip Size：15.9×25.7mm
  - 25μm×25μm pixel size with high spatial resolution
  - Process: Towerjazz 180nm CIS process
  - Fast digital readout to cope with ZH and Z runs (support 40MHz clock)





TaichuPix-3 chip vs. coin

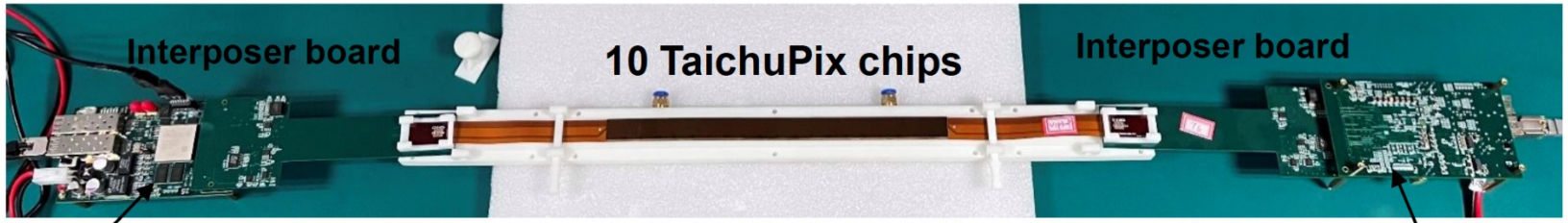




An example of wafer test result

	Status	CEPC Final goal
CMOS chip technology	Full-size chip with TJ 180nm CIS	65nm CIS

R&D effort: vertex detector prototype

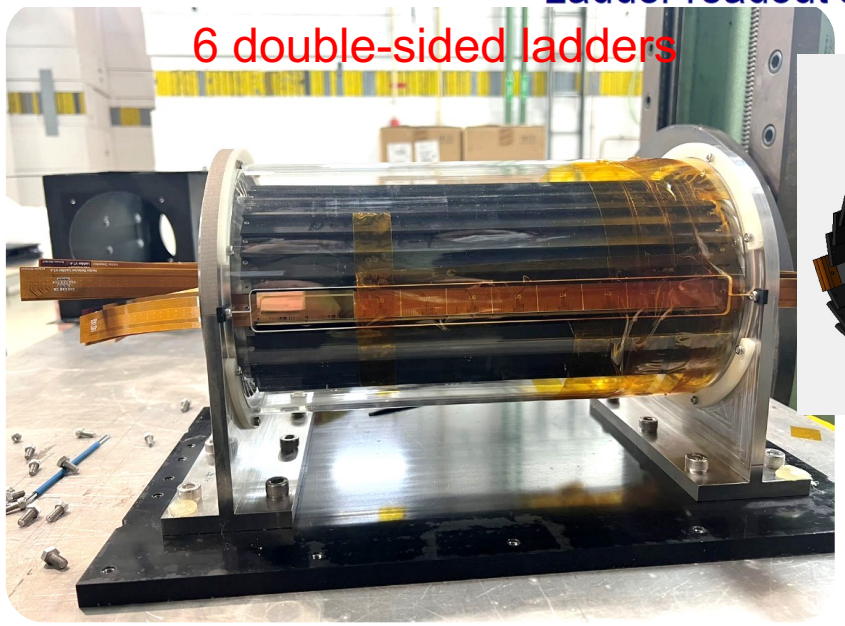


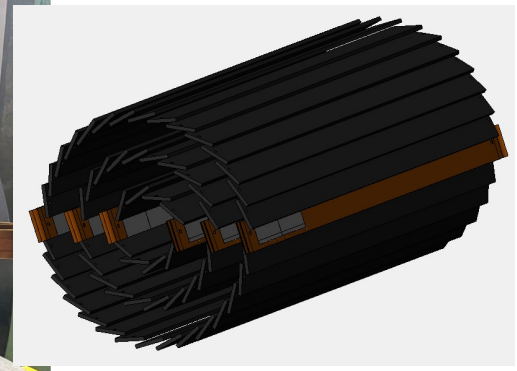
TaichuPix-based prototype detector tested at DESY in April 2023

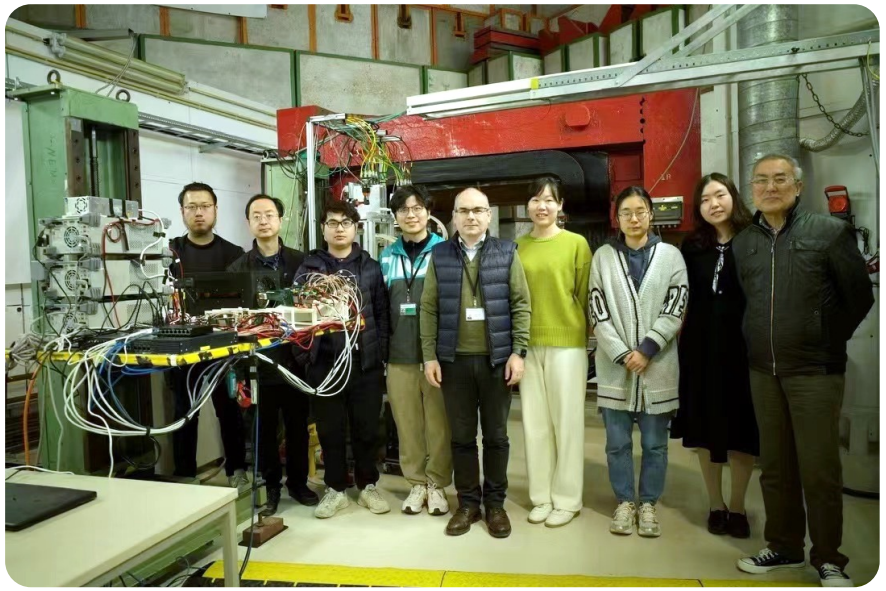
Spatial resolution ~ **4.9 μm**

Ladder readout system

6 double-sided ladders

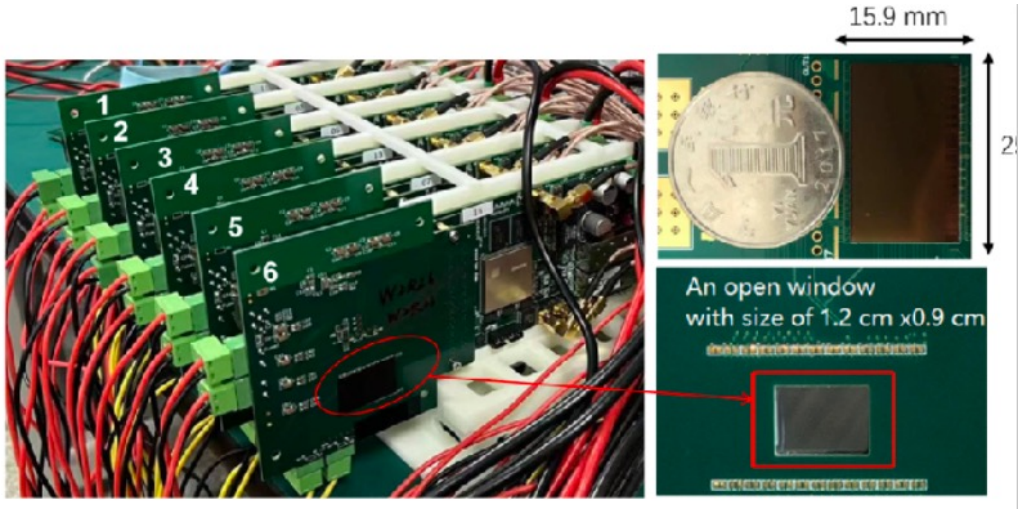


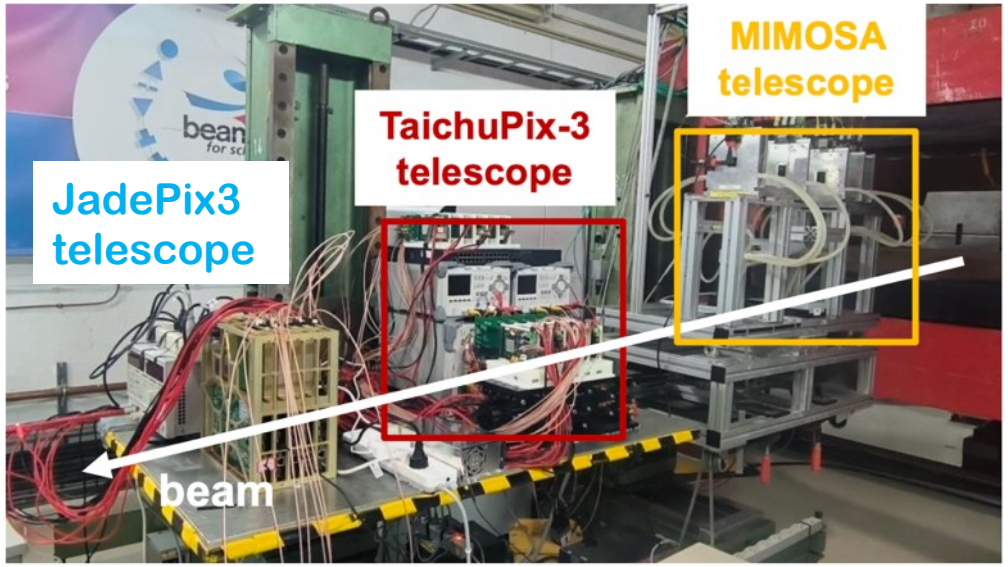




	Status	CEPC Final goal
Detector integration	Detector prototype with ladder design	Detector with bent silicon design

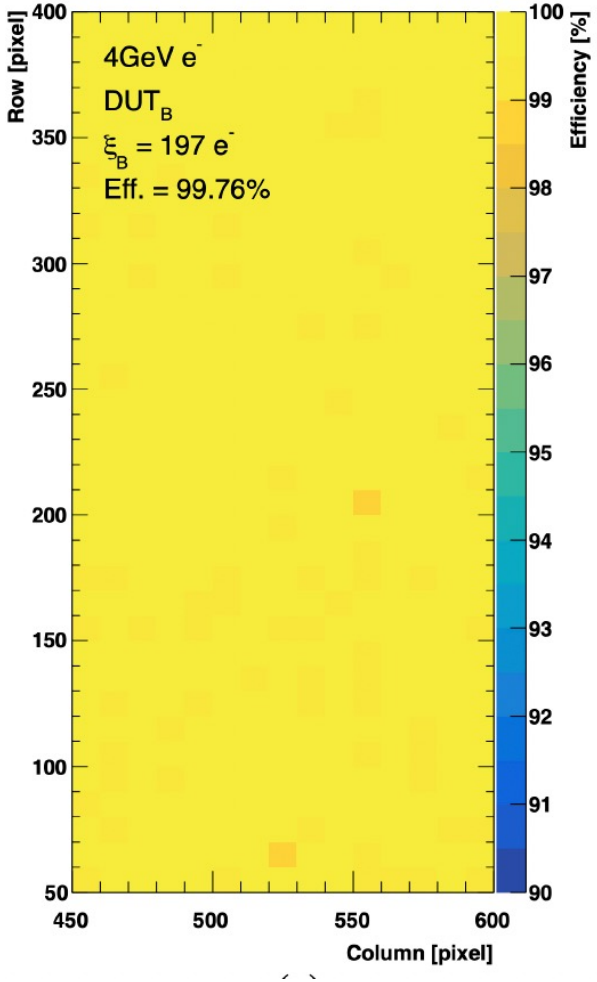
R&D efforts and results: Jadepix3/TaichuPix3 beam test @ DESY



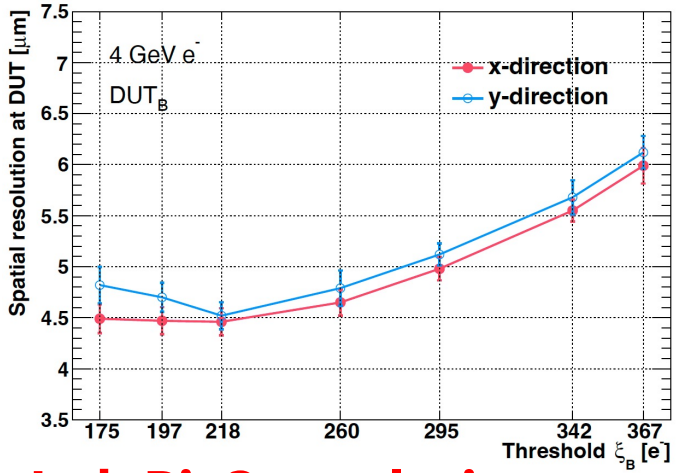


Spatial resolution 4~5um, Efficiency >99%

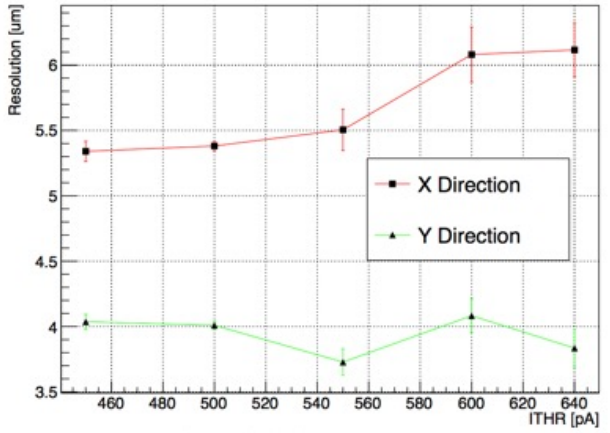
TaichuPix3 efficiency



TaichuPix3 resolution



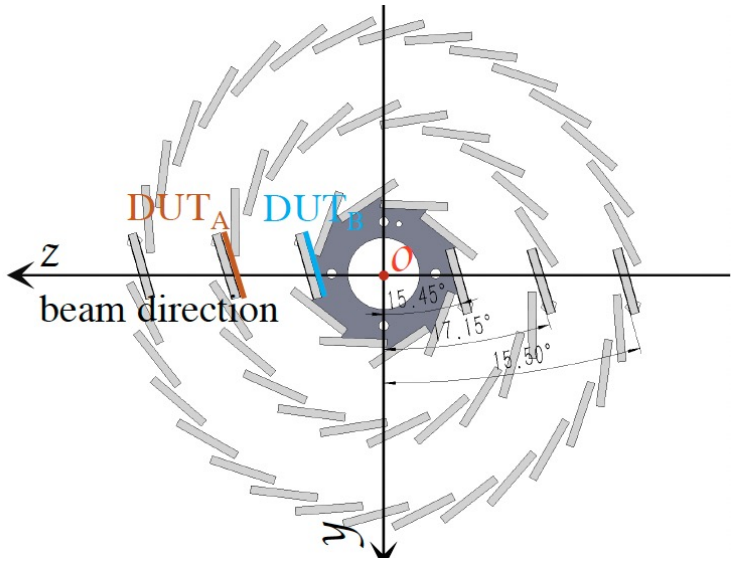
JadePix3 resolution

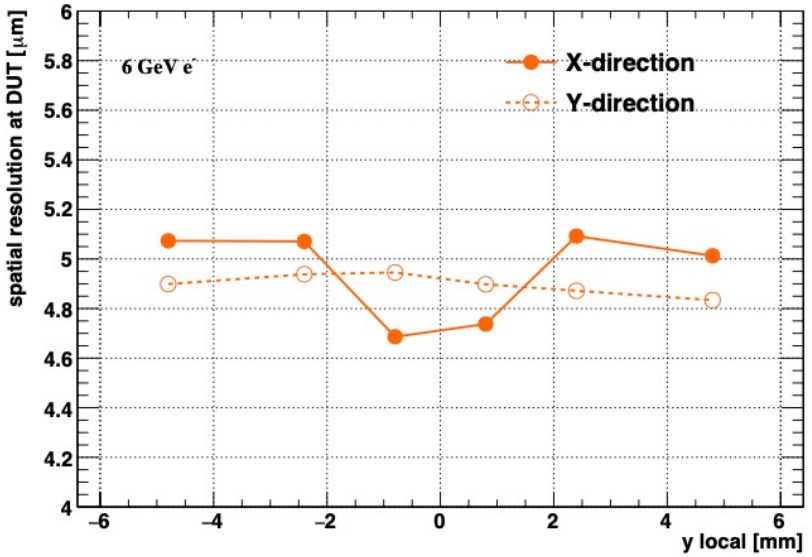


Collaboration with CNRS and IFAE in Jadepix/TaichuPix R & D

R&D efforts and results: vertex detector prototype beam test

Spatial resolution ~ **5 μm**

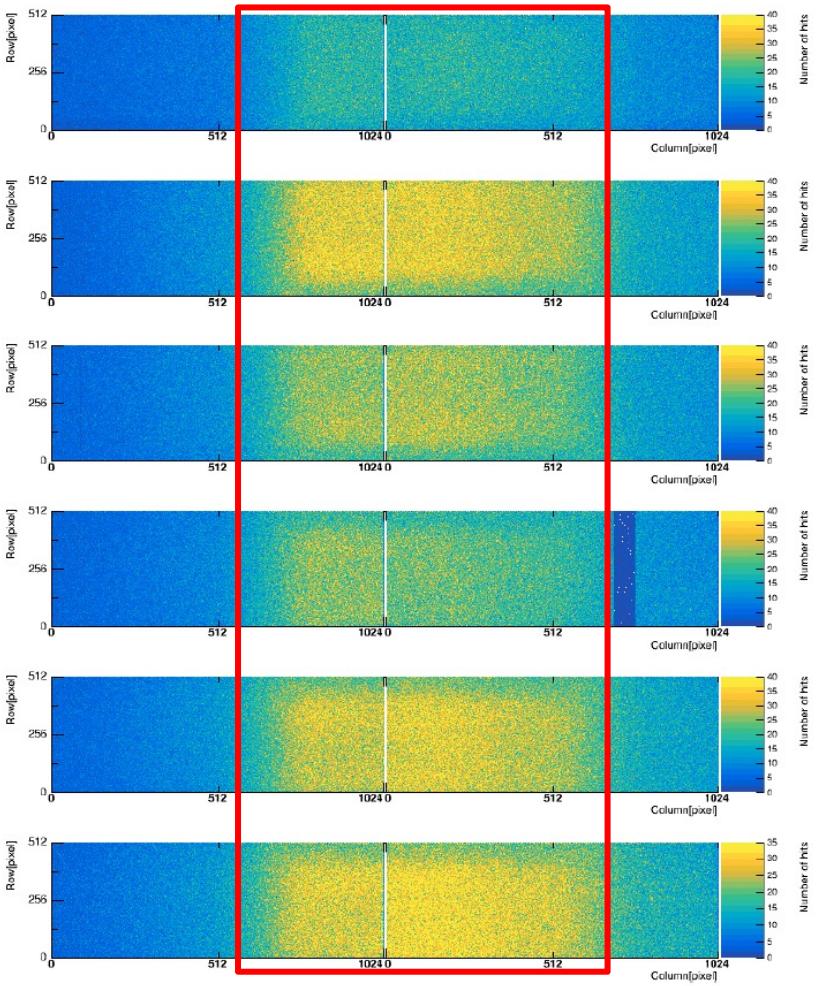




	Status	CEPC Final goal
Spatial resolution	4.9 μm	3-5 μm

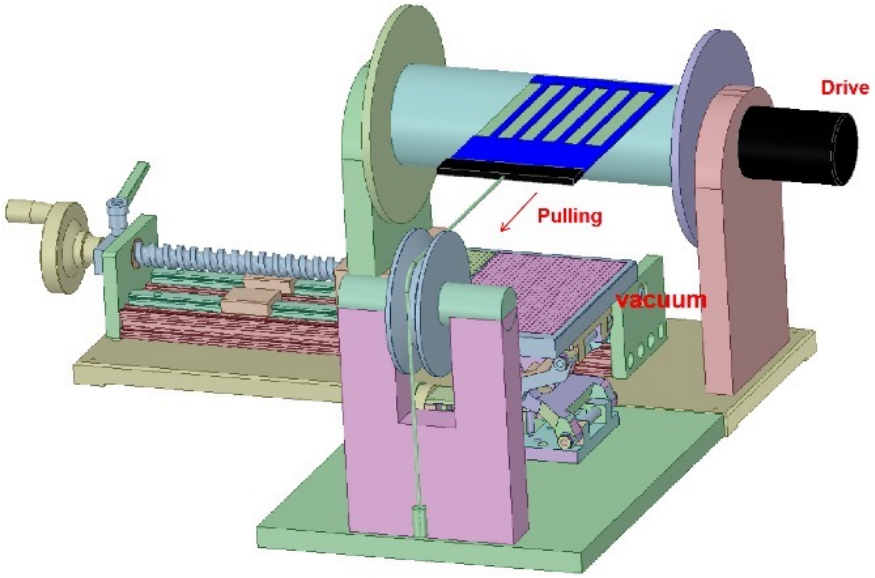
Hit maps of multiple layers of vertex detector

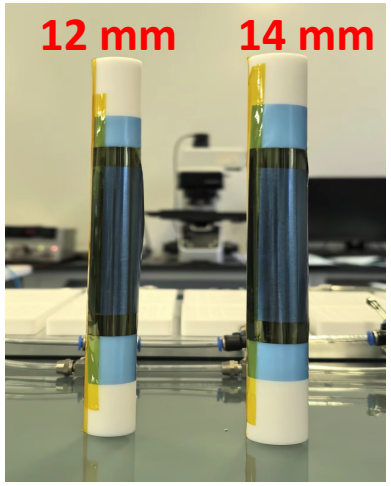
Beam spot



R&D efforts curved MAPS

- CEPC b-layer radius (11 mm) smaller compared with ALICE ITS3 (radius = 18 mm)
- Feasibility : Mechanical prototype with dummy wafer can curved to a radius of 12 mm
  - The dummy wafer has been thinned to 40 µm





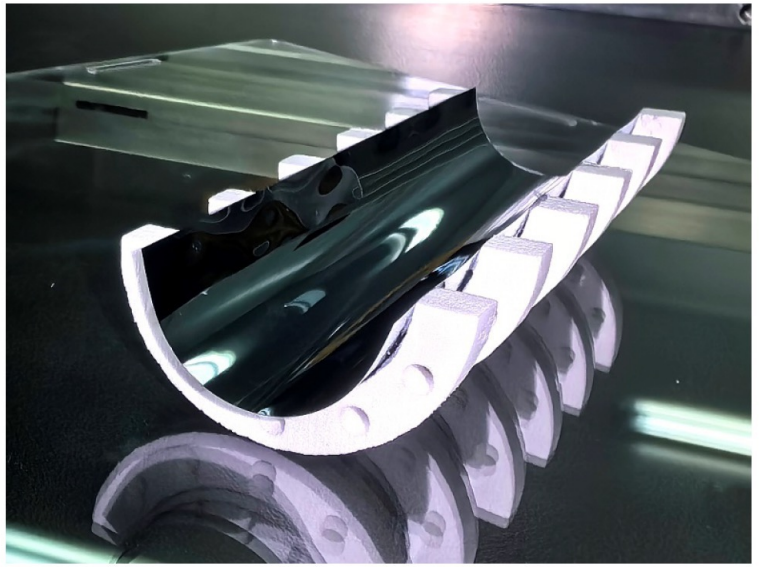
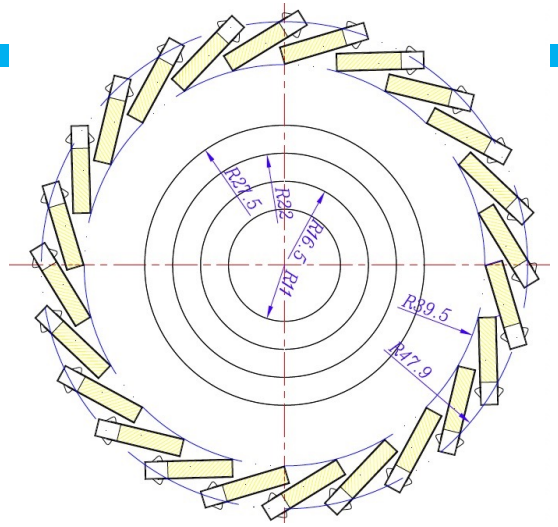


Figure 4.26: 12 mm bending radius.

	Status	CEPC Final goal
Bent silicon with radius	Bent Dummy wafer radius ~12 mm	Bent final wafer with radius ~11 mm

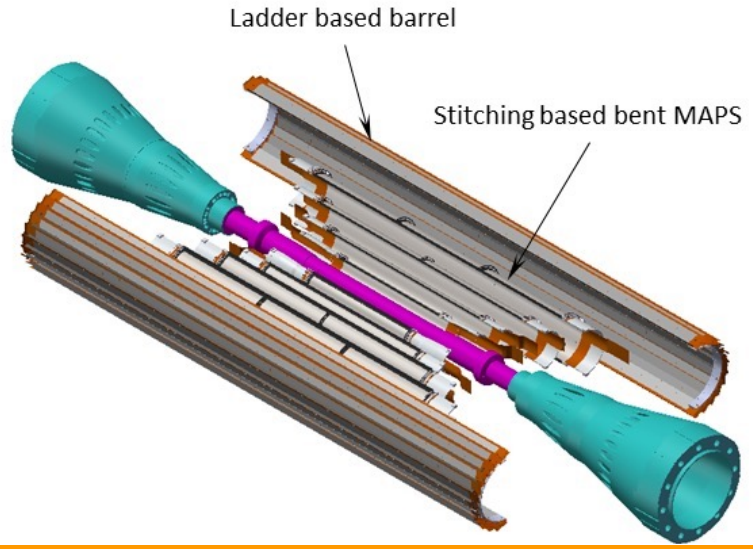
Baseline layout in CEPC Ref-TDR

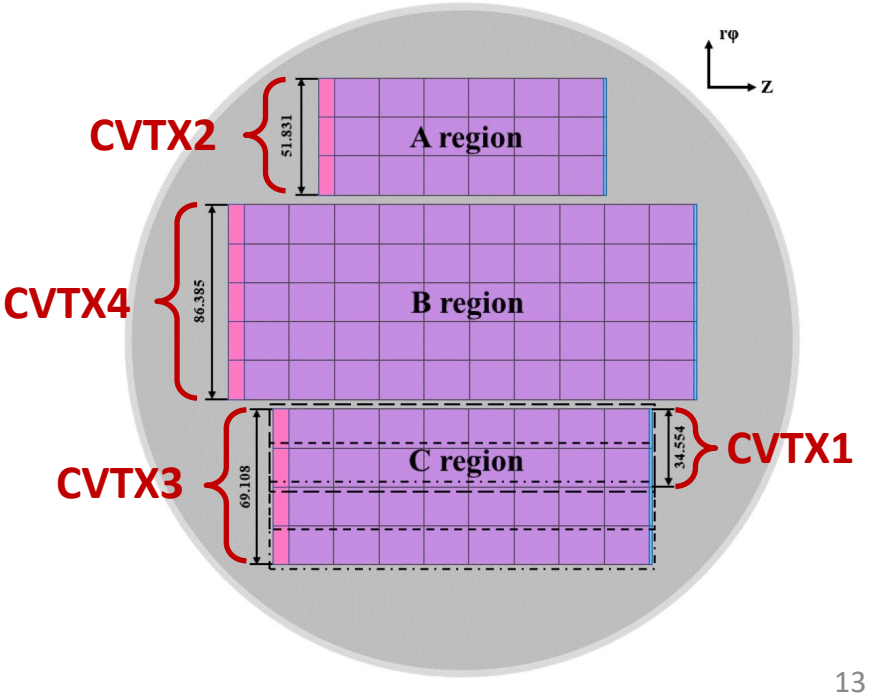
- Baseline: 4 single layer of bent MAPS + 1 double layer ladders
  - Alternative option: 3 double layer ladders
- Inner layer: using single bent MAPS (~0.15 m^2)
  - Low material budget 0.06% X_0 per layer
  - Different rotation angle in each layer to reduce dead area
- Outer layer: using double layer ladder (~0.3% X_0/layer)



CVTX/ PVTX X	radius mm	length mm
CVTX 1	11.1	161.4
CVTX 2	16.6	242.2
CVTX 3	22.1	323.0
CVTX 4	27.6	403.8
PVTX 5	39.5	682.0
PVTX 6	47.9	682.0

Long barrel layout (no endcap disk)





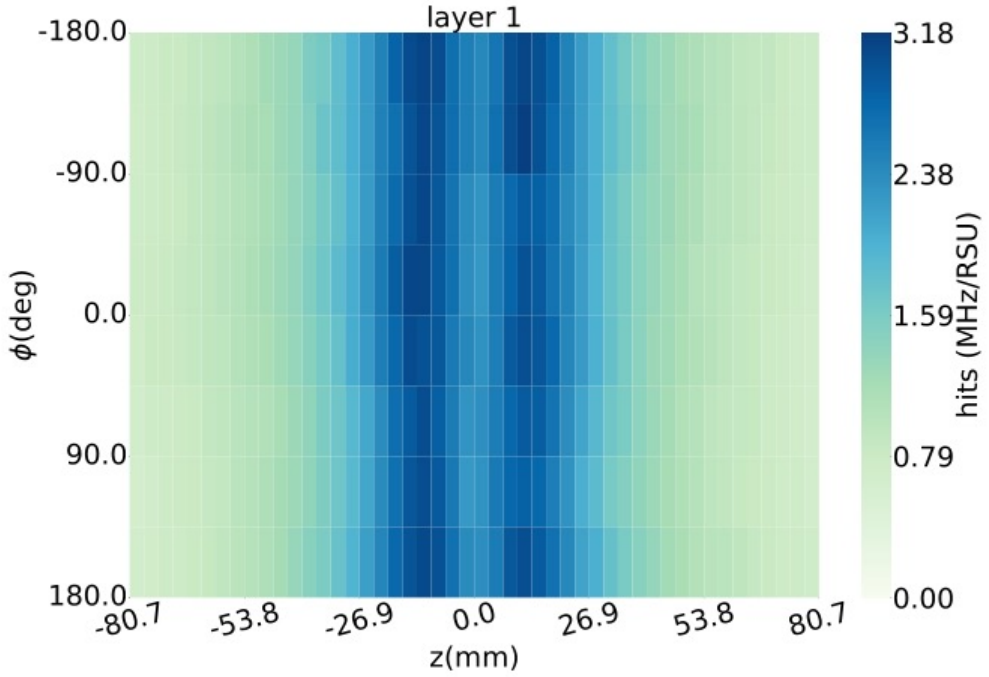
Background estimation

- The various sources of beam-induced backgrounds are simulated
  - The data rate at low-lumi Z pole is about ~Gbps level in b-layer

Background rate for Higgs and low-lumi Z runs

Layer	Ave. Hit Rate (MHz/cm^2)	Max. Hit Rate (MHz/cm^2)	Ave. Data Rate (Mbps/cm^2)	Max. Data Rate (Mbps/cm^2)
Higgs mode: Bunch Spacing: 277 ns, 63% Gap				
1	6.2	12	760	1500
2	0.84	1.6	87	160
3	0.17	0.36	19	38
4	0.067	0.16	8.4	19
5	0.017	0.037	2.1	4.2
6	0.013	0.026	1.6	3.7
Low-luminosity Z mode: Bunch Spacing: 69 ns, 17% Gap				
1	15	39	2700	8100
2	1.7	2.6	240	400
3	0.72	1.2	110	240
4	0.43	0.94	70	210
5	0.10	0.19	14	31
6	0.078	0.15	11	23

Hit rate map for 1st layer @ Higgs mode



Electronics

- Inner layer (L1-L4): stitching and RDL metal layers on wafer to transfer signal and power
  - Flexible Printed Circuit (FPC) connecting stitched sensors and Front-end Electronics Board (FEE)
  - FEE is installed in the service area outside of fast-LumiCal
- Outer layer (L5-L6): ladder on FPCs (also used in alternative layout)
  - Signal, clock, control, power, ground will be handled by control board through FPCs

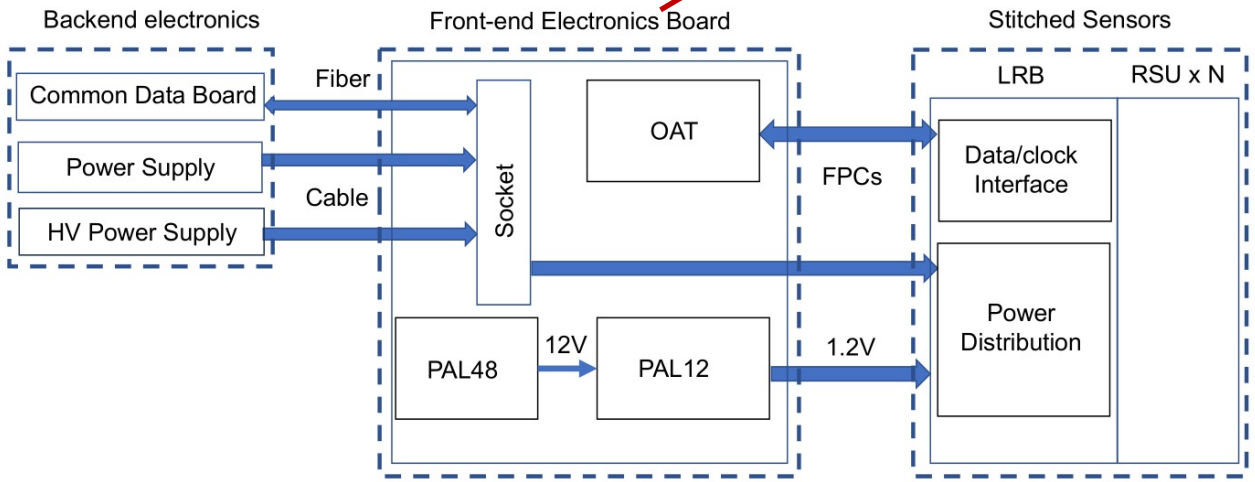
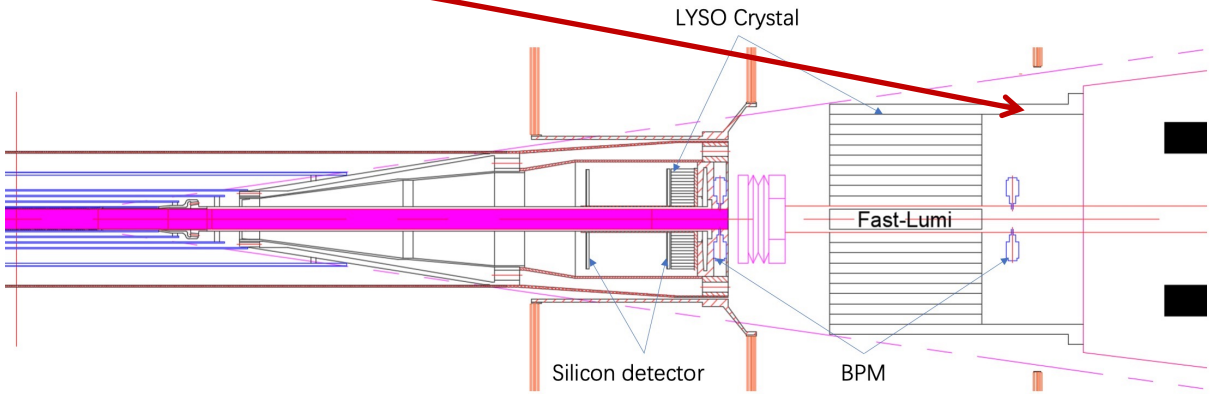


Diagram of the VTX readout electronics



Location of the VTX service area

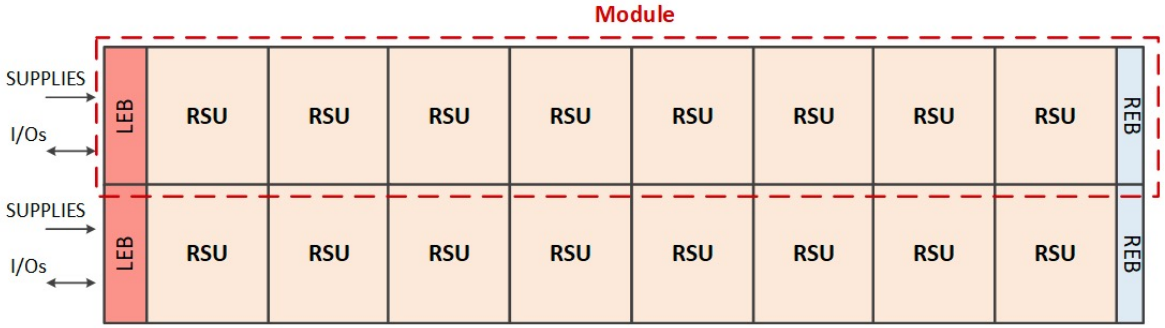
Electronics (2)

– Stitching layer : Stitching on MAPS wafer to replace PCB

– Outer layer (L5/L6) : flexible PCB （ also used in alternative layout)

- Signal, clock, control, power, ground will be handled by control board through flexible PCB

Stitching layers



Outer layer (layer 5/6,) : flexible PCB

Ladder readout system

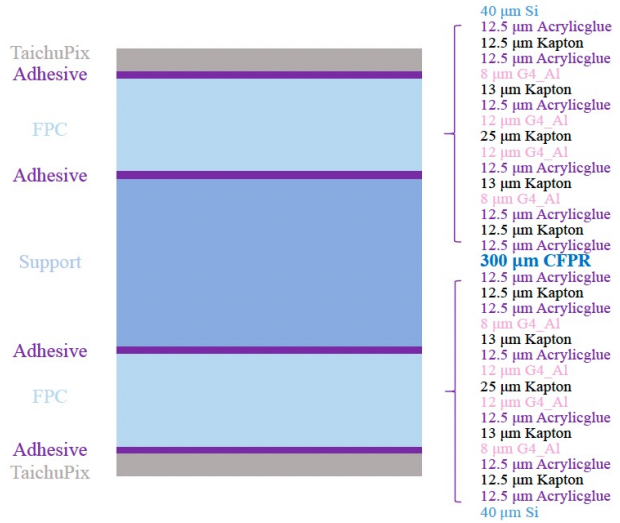
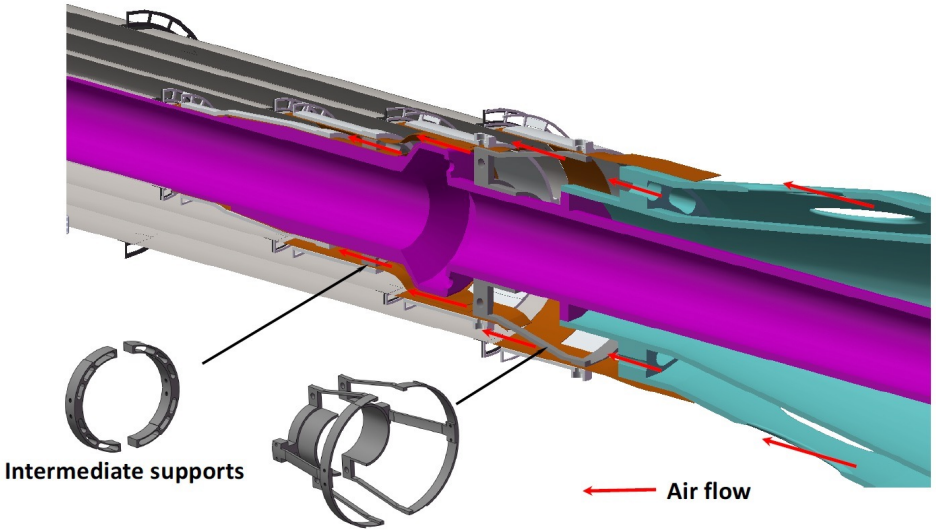


Table 4.12, Estimates of average power dissipation per unit area

	Power density [mW/cm^2]
Repeated Sensor Unit	38
Left-End Block	485

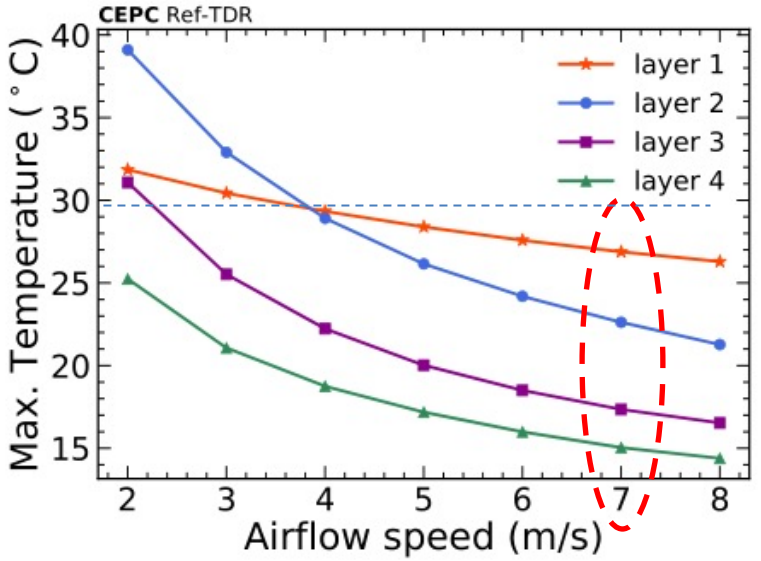
Mechanics and cooling

- Benefitted from 65 nm technology, power consumption can be reduced to ~40 mW/cm^2
- Air cooling feasibility study
  - Effective airflow cross section of 12.6 cm^2
  - can be cooled down below 30 ℃ with 7 m/s air speed, Temperature gradient is within 10 ℃

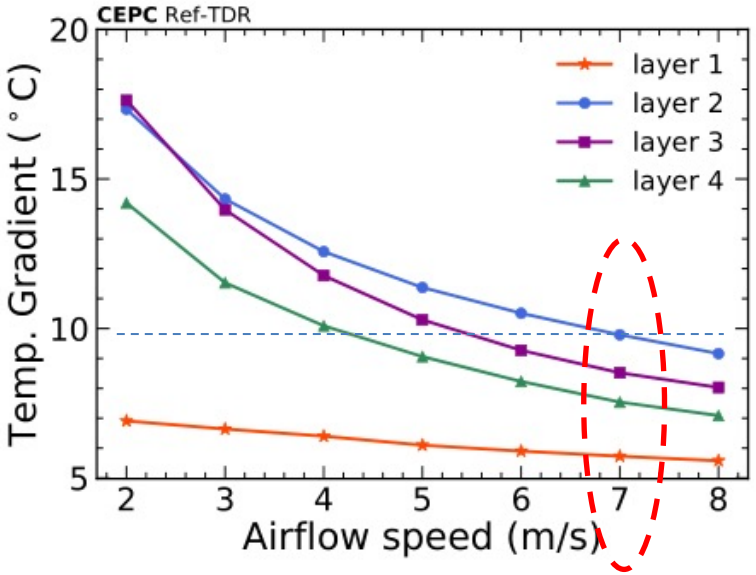


Installation of the half layers and intermediate support

Maximum temperature in stitching layers



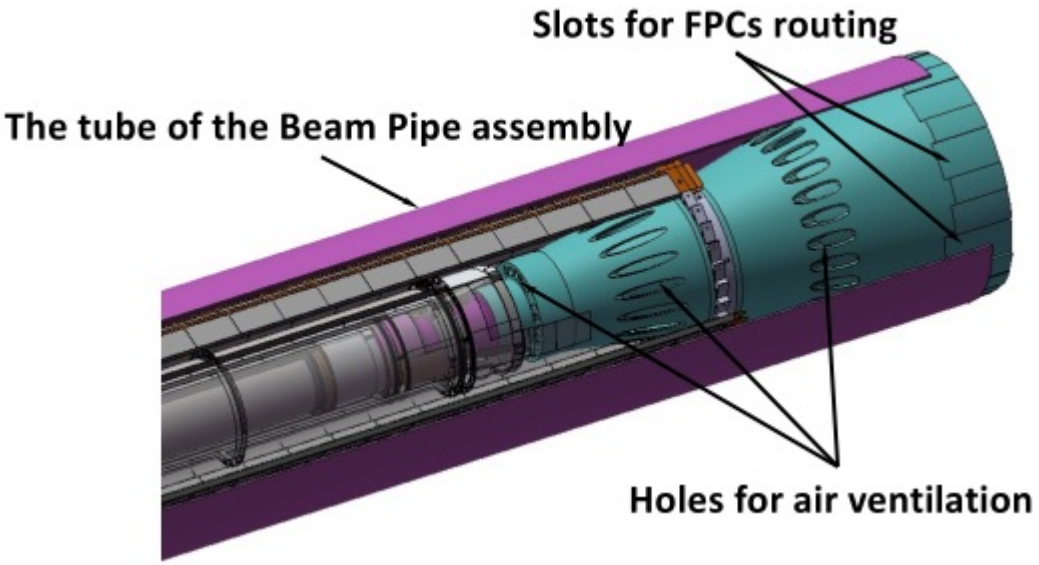
Temp. Gradient in stitching layers



Thermal simulation results for the curved layers

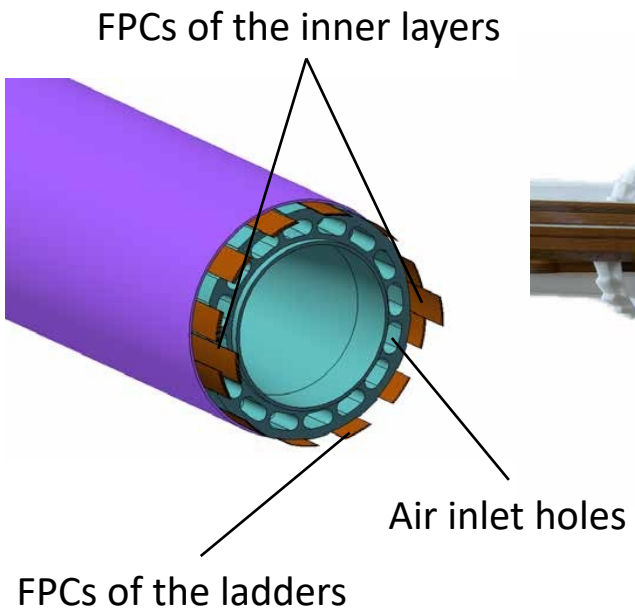
Vertex technologies: Cables and services

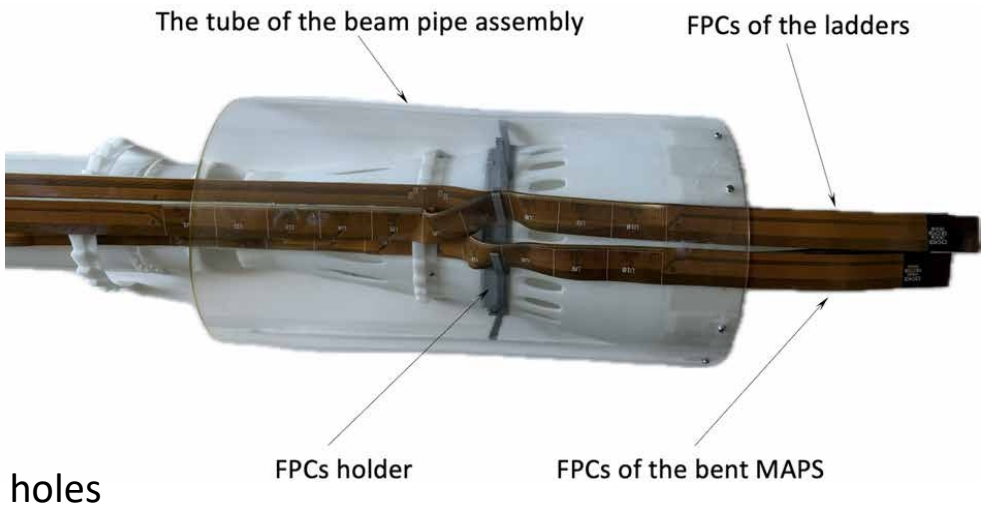
- A hollow conical structure integrated into the beam pipe assembly to serves as air distributor.
- A half-dummy 3D printed mechanical mockup was constructed
  - Validated there is enough space for cable routing and air cooling channel
  - The effective area for air cooling is 12.6 cm^2 (stitching layers)+ 28 cm^2 (between L4/L5)



Cross-sectional view of the full assembly

Dummy mockup of the VTX structure





Alignment in stitching layer

- Deformation mode simulated by FEA.

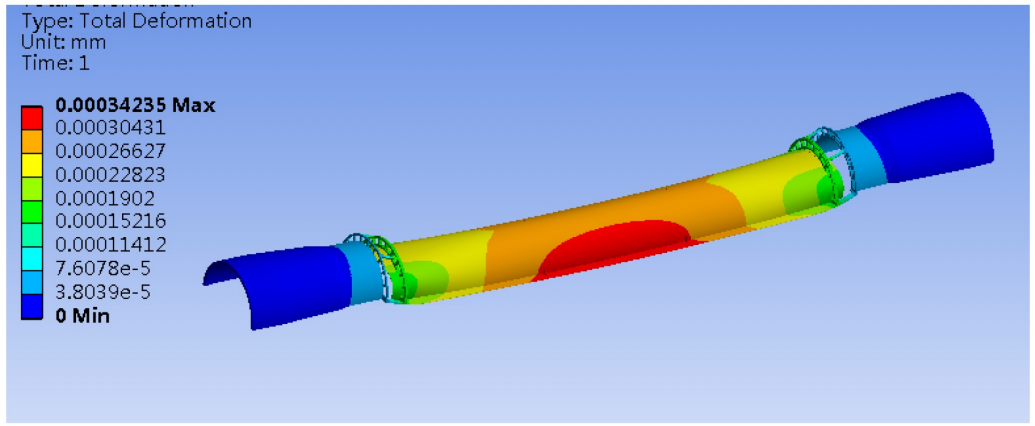
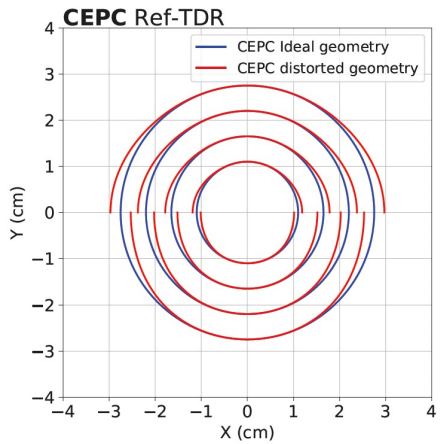
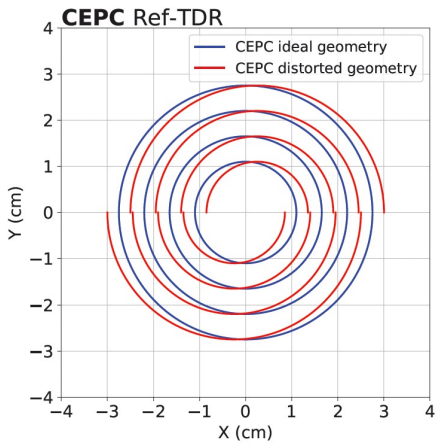
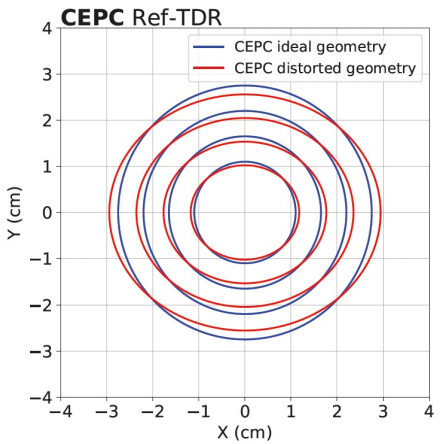


Figure 4.71: The simulated defromation of the inner layer bent MAPS half cylinder.

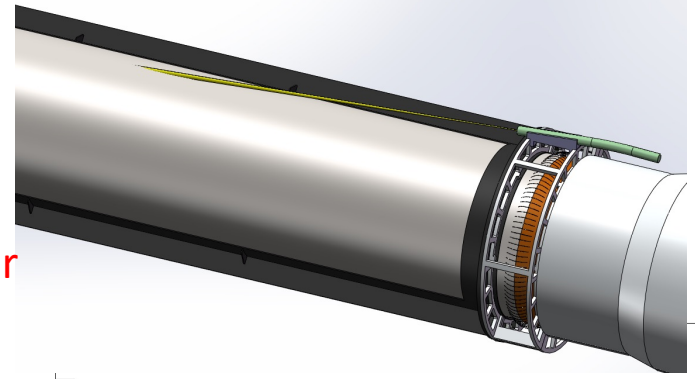




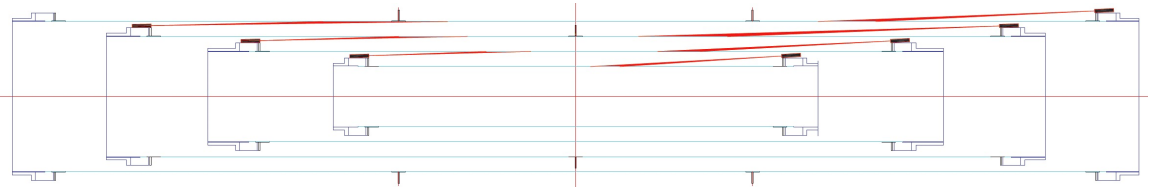


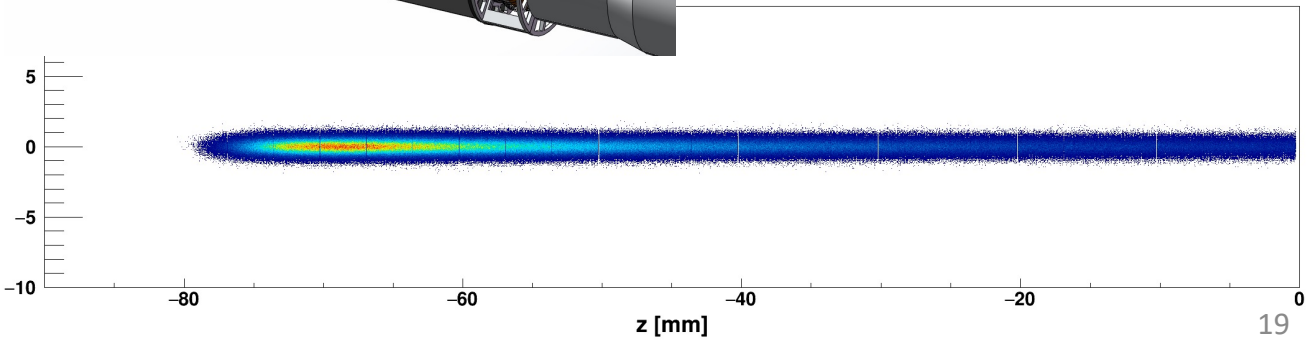
- Real time Deformation monitoring by infra-red laser alignment system

2D and 3D model on laser alignment system on vertex detector (inspired by CMS tracker laser alignment)



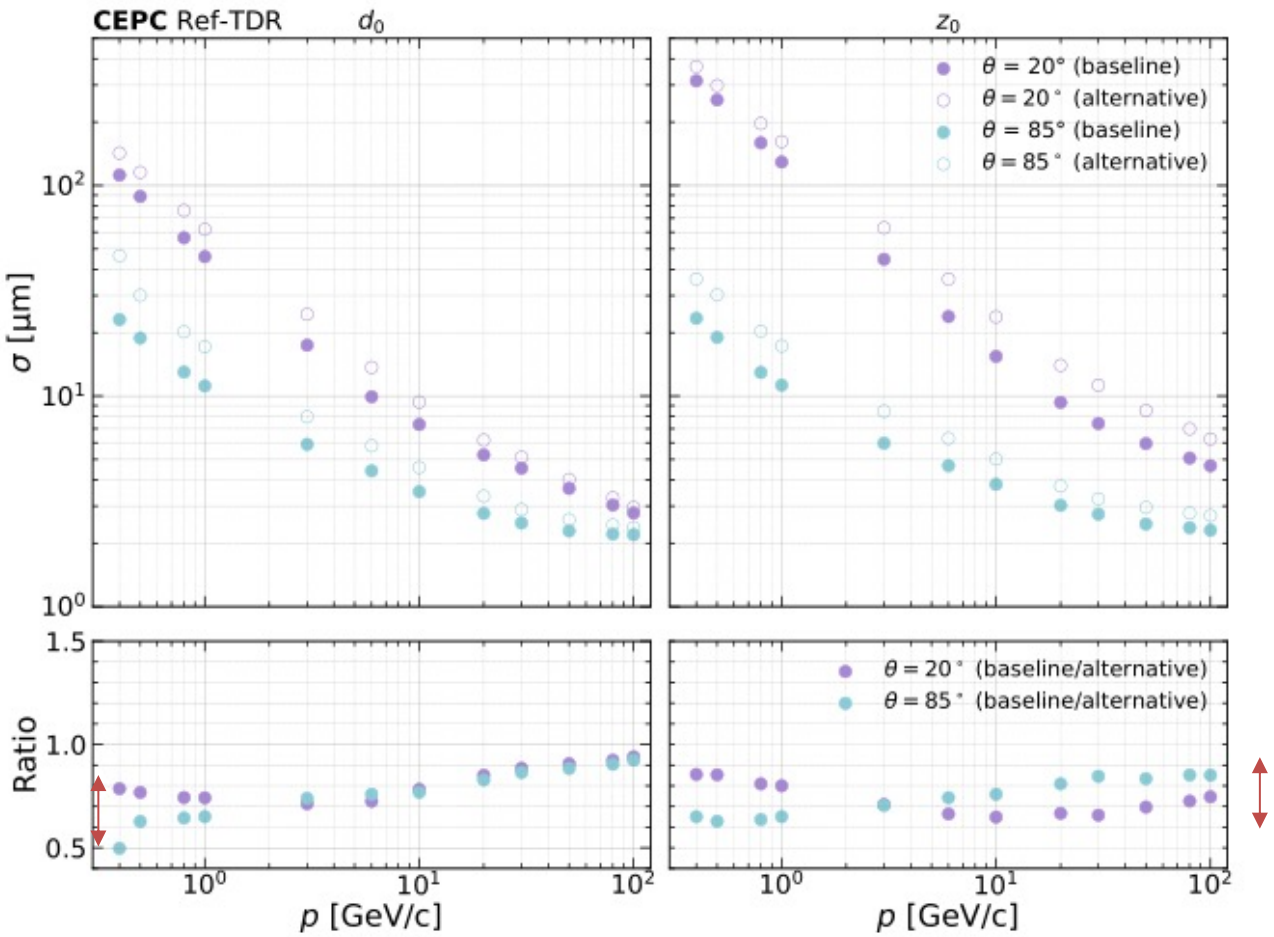
laser beamspot on bent-MAPS



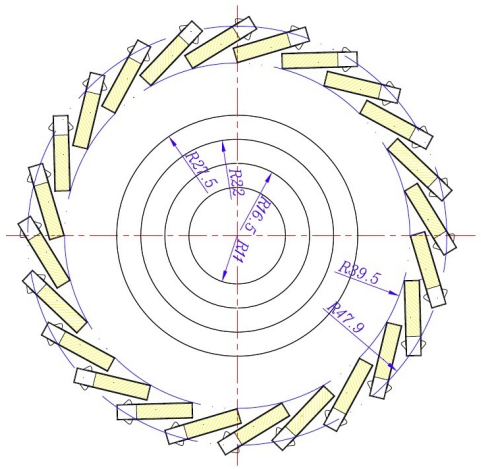


Performance: impact parameter resolution

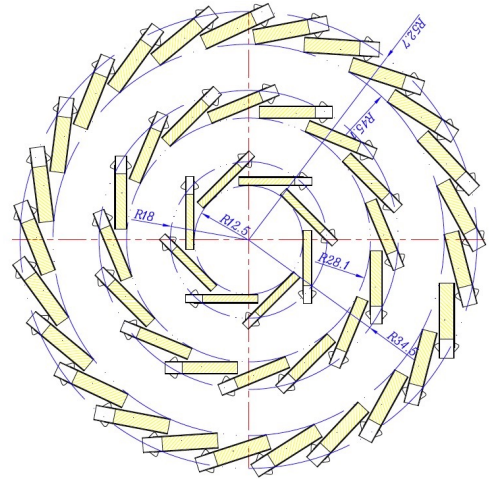
- Baseline has better resolution than alternative (ladder) (10-40%) in 0.4 GeV to 100 GeV



Baseline scheme
4 stitched curved sensor +
1 double layer ladders



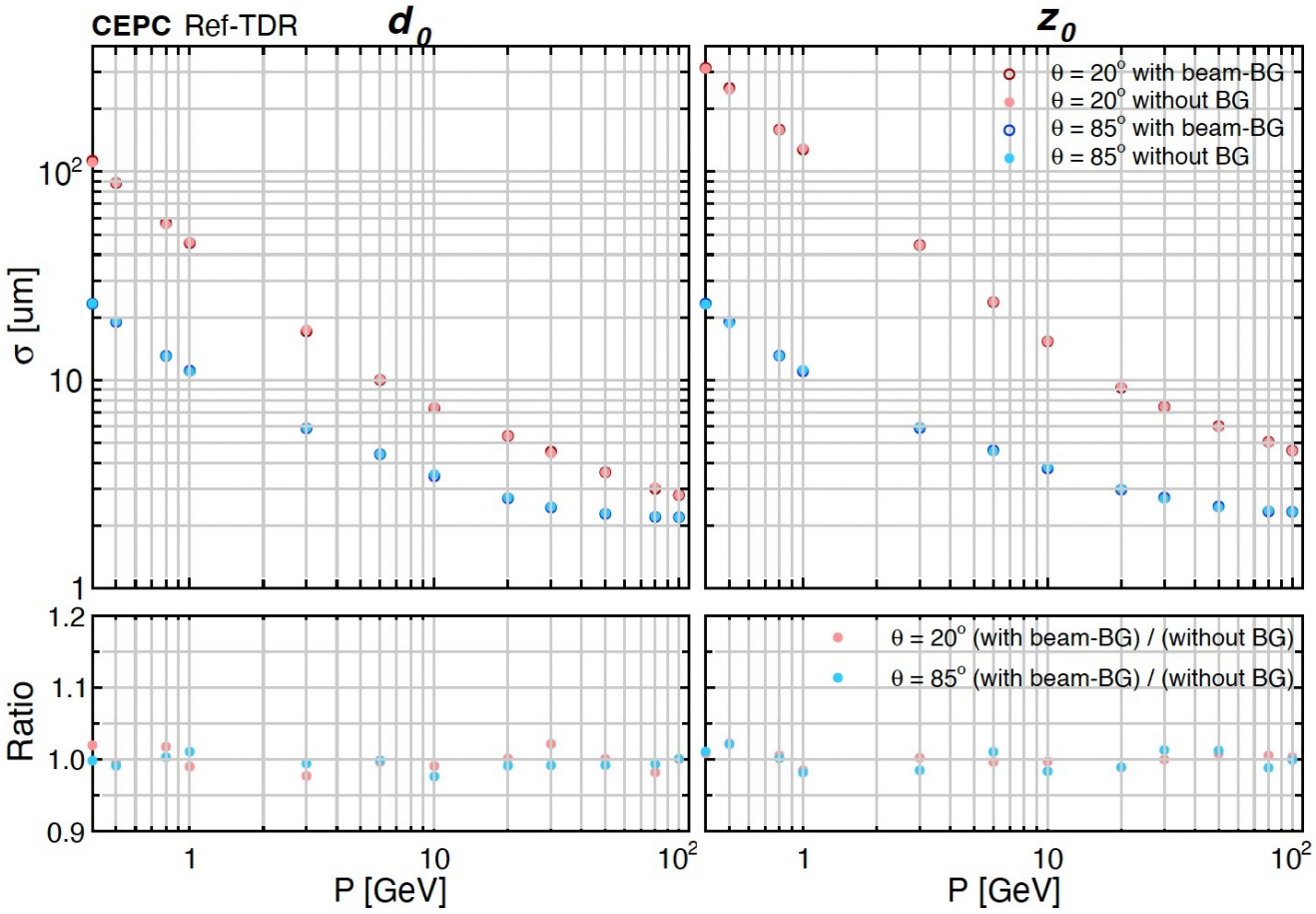
Alternative scheme
3 double layer ladders



Impact parameter resolutions of d_0 and z_0 for the baseline and alternative

Performance with beam background

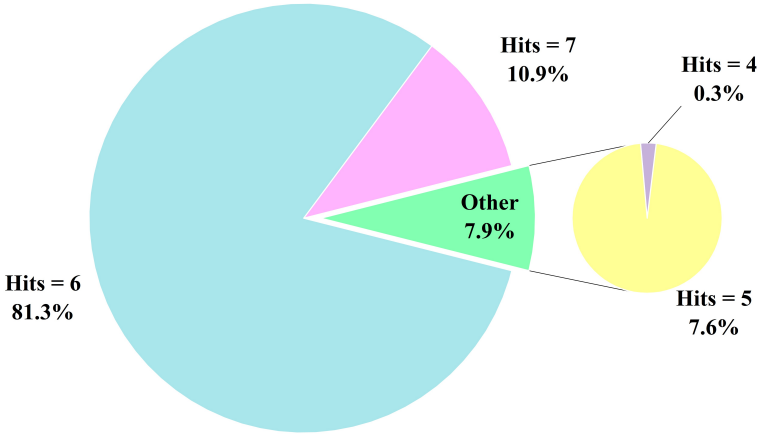
- The impact of beam background to performance has been studied.
  - Beam background rate is order of magnitude higher than signal
    - No visible impact to performance
    - Tracking time increased with Bkg



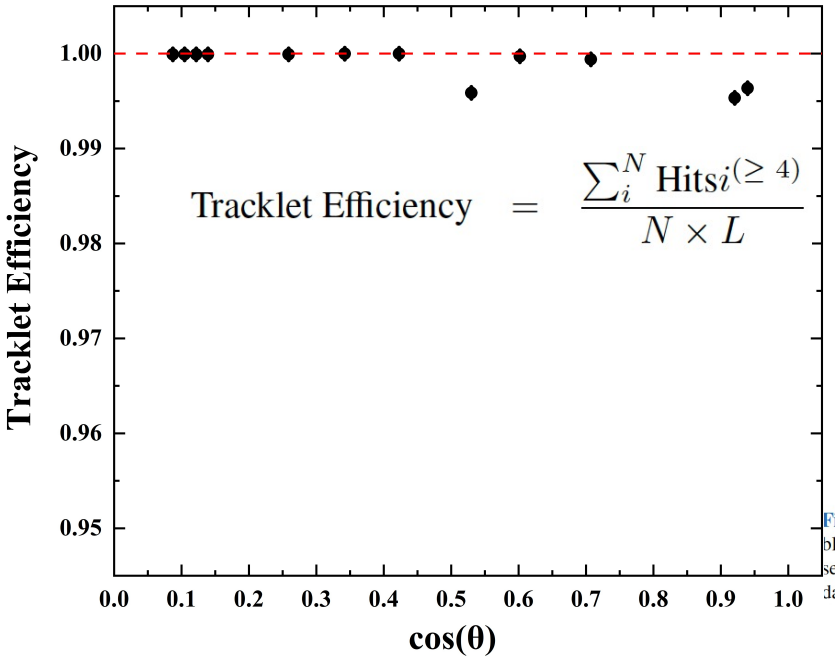
Performance: Efficiency

- A few percent Inefficiency expected in stitching layer
- Sensor (RSU) has inefficiency region in power stitch
- 99.7% of the track with >=4 hits (6 hits expected)

Number of hits



Tracklet efficiency



RSU design

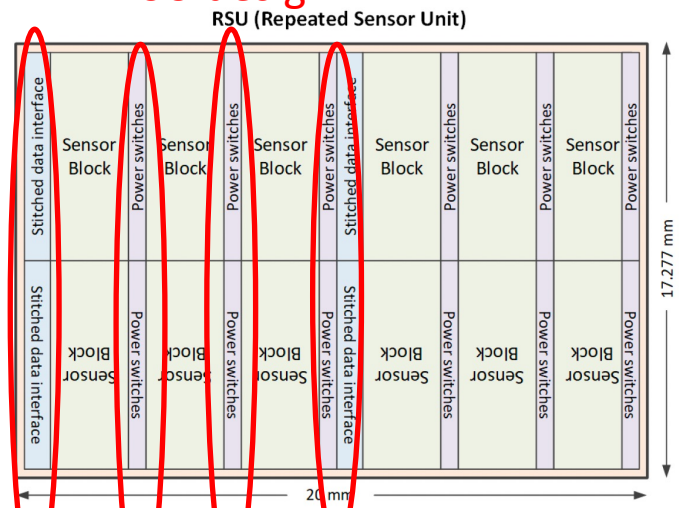


Figure 4.50: Proposed floor-plan for a repeated sensor unit (RSU) (not to scale). It contains several identical senso blocks. Each of them has a pixel matrix with its own biasing generator, slow control and periphery readout circuit. Each sensor block can be selectively switched on/off. The stitched data interface blocks are used to transmit control signals and data to the edge of the stitching sensor.

Research team

- IHEP: Chip design, detector assembly
- IPHC/CNRS: chip design, Christine Hu et al: Collaboration in FCPPL and DRD3 framework
- IFAE: Chip design , Sebastian Grinstein et al
- ShanDong U.: Stitching chip design
- CCNU: chip design, ladder assembly
- Northwestern Polytechnical U. : Chip design
- Nanchang U. : Chip design
- Nanjing U.: irradiation study, chip design
- NanKai U. : physics performance
- Recent developing R & D collaboration with CERN in HLMC 55nm aiming for ALICE3 upgrade

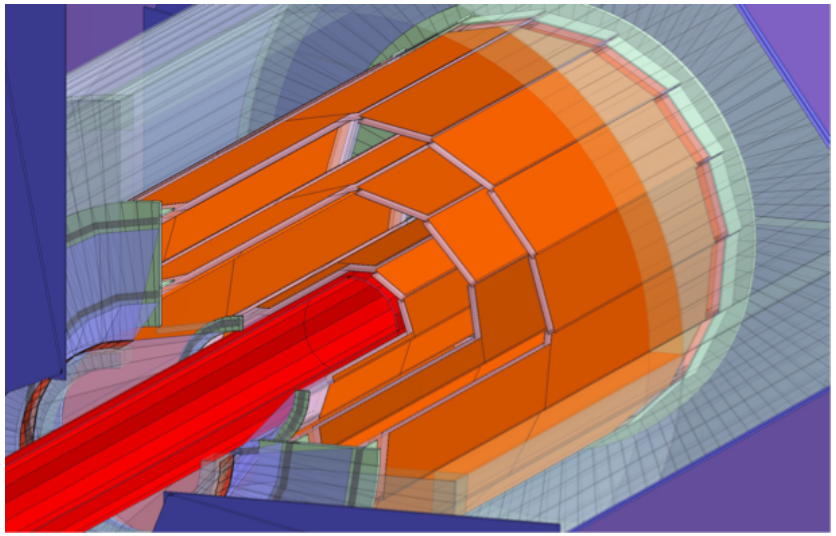
Working plan

- Development of wafer-scale stitched MAPSs.
  - Develop wafer-scale stitching with 180nm technology
  - The second-generation stitching chip will transition to 65 nm/55 nm
    - Baseline: TPSCo's 65 nm technology
    - Alternative: Shanghai HLMC's 55 nm technology
- Ultra-thin mechanical supports and low-mass integration techniques.
  - Start with prototype with dummy silicon wafer
- Construction of a full-scale VTX prototype to address challenges in mechanical precision, cooling performance, laser alignment, and system-level integration.

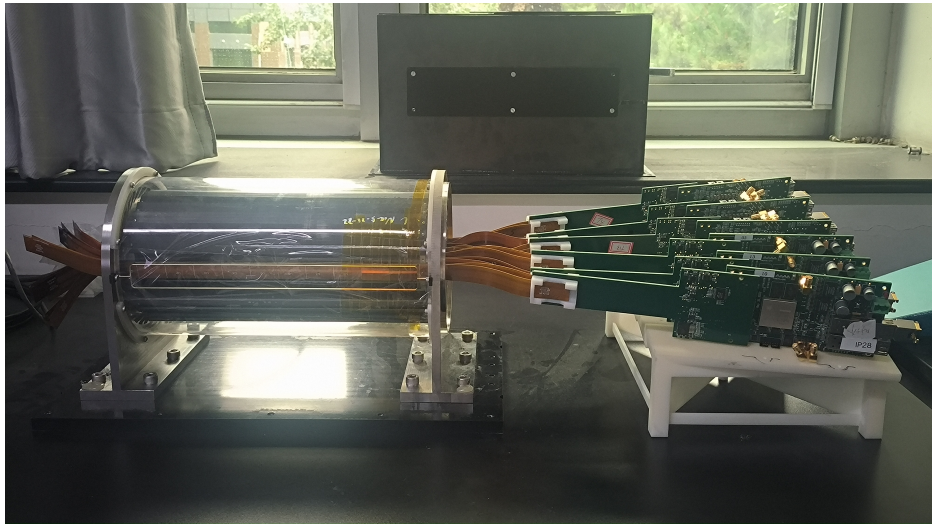
Summary

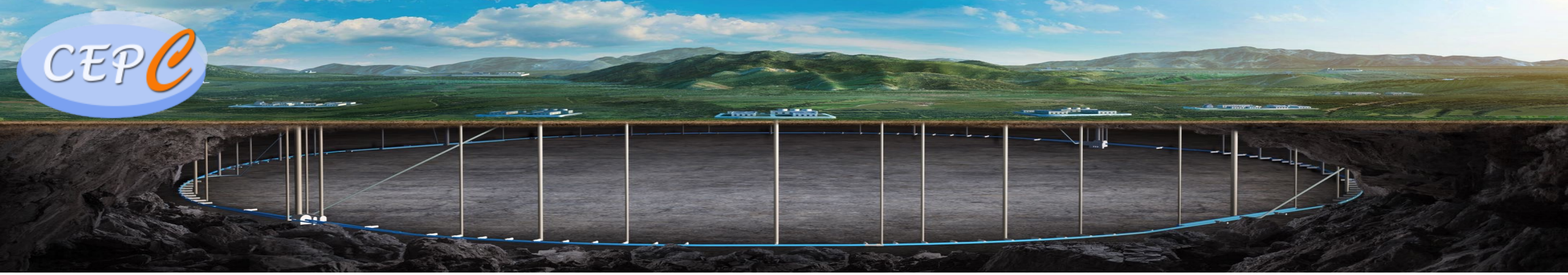
- Completed reference TDR for CECP vertex detector
  - Aiming for stitching technology as baseline design for reference TDR
- We active expanding international collaboration and explore synergies with other projects
  - We are members of ECFA DRD3 collaboration

CEPC vertex conceptional design (2016)



CEPC vertex prototype (2023)





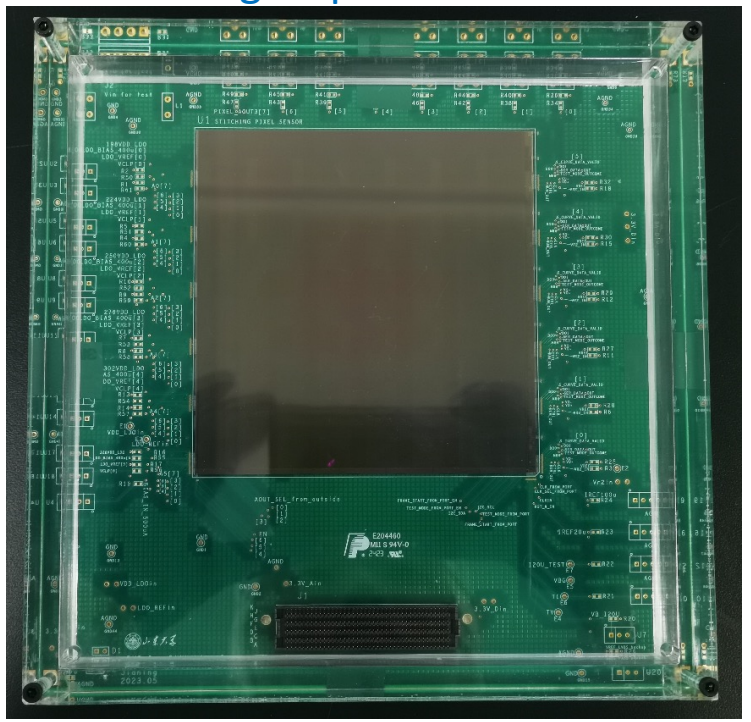
Thank you for your attention!

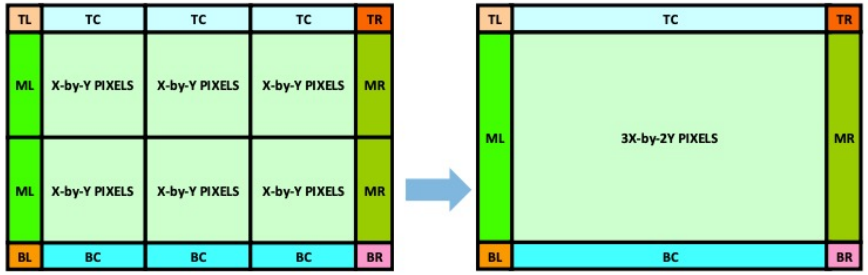
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

R&D efforts and results: R & D for curved MAPS

- Stitching chip design (by ShanDong U.)
  - 350nm CIS technology Xfabs
  - Wafer level size after stitching ~11 ×11 cm^2
  - reticle size ~2 ×2 cm^2
  - 2D stitching
  - Engineering run, chip under testing

Stitching chip : 11 ×11 cm^2

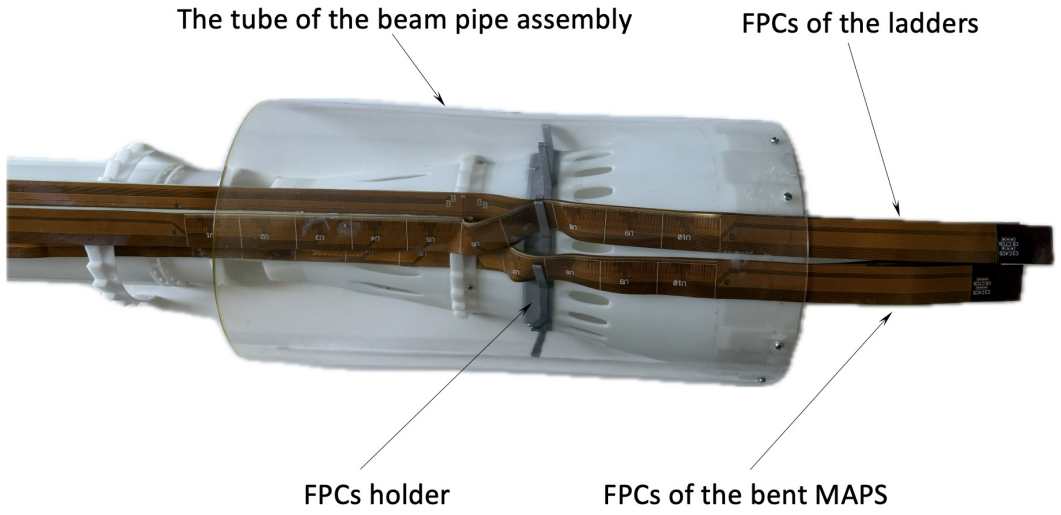




Key technology	Status	CEPC Final goal
Stitching	11*11cm stitched chip with Xfab 350nm CIS	65nm CIS stitched sensor

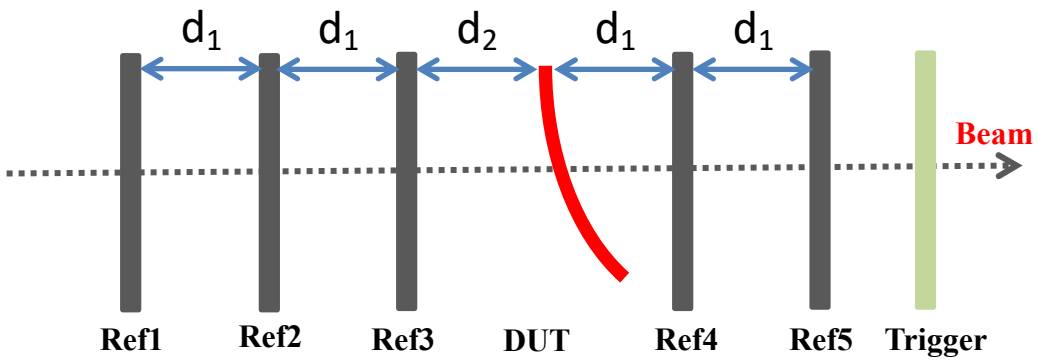
Vertex detector Mockup: Cable routing

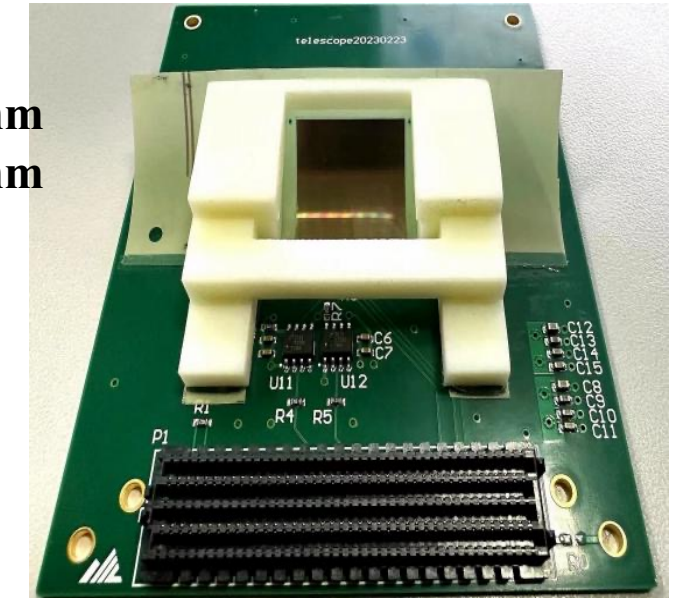
- Full-size 3D printed vertex detector and beam-pipe mockup
  - Validate there is enough space for cable routing and air cooling channel
  - The total cross-sectional area available for air cooling in the inner four layers is 12.6 cm^2

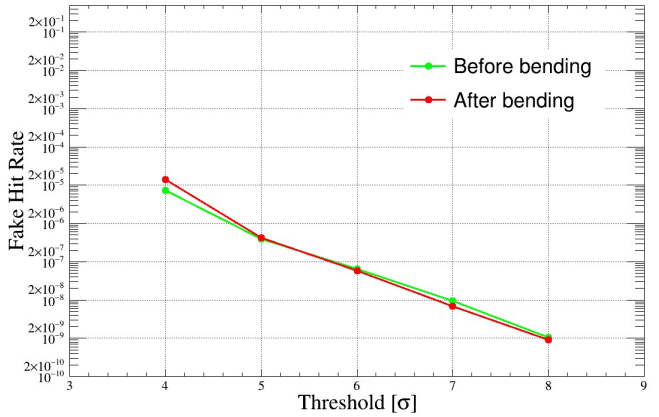


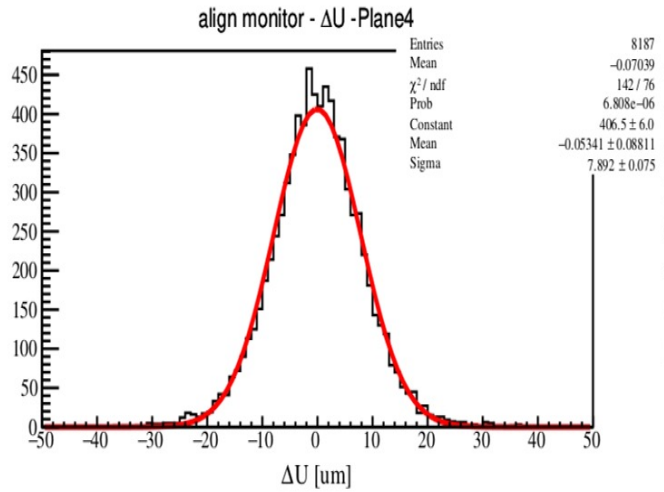
R&D efforts : Curved MAPS testbeam

- R & D of curved maps with MIMOSA28 chip
  - No visible difference in noise level or spatial resolution before/after bending

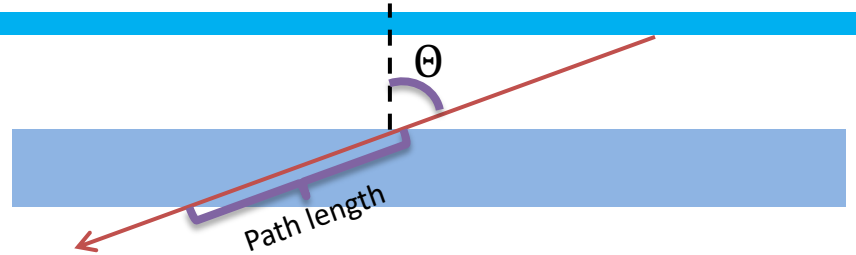




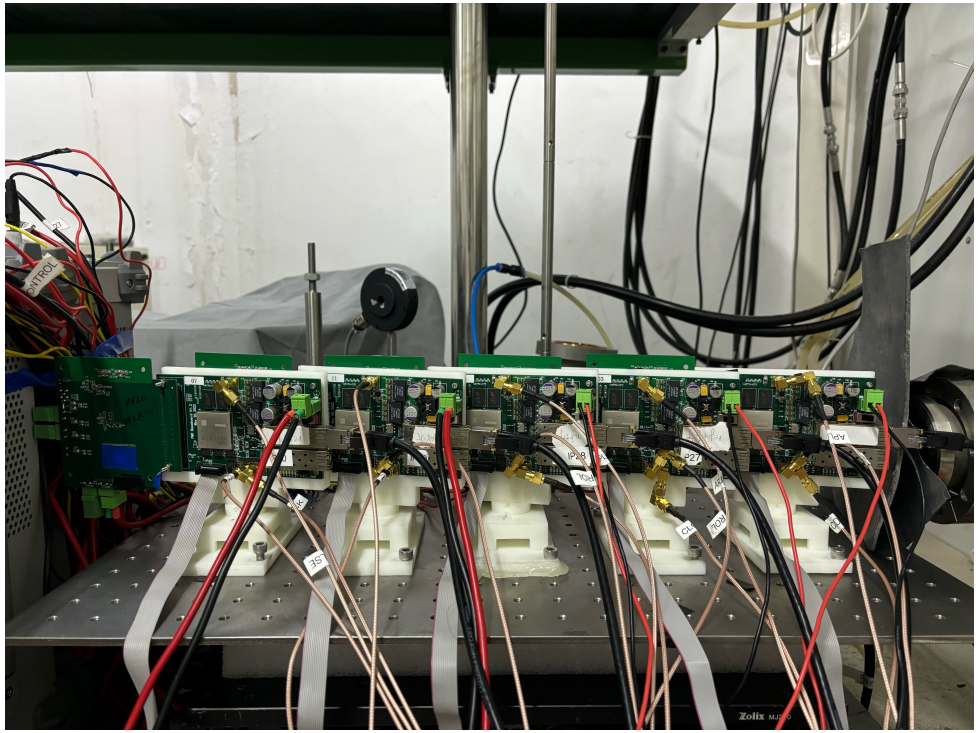


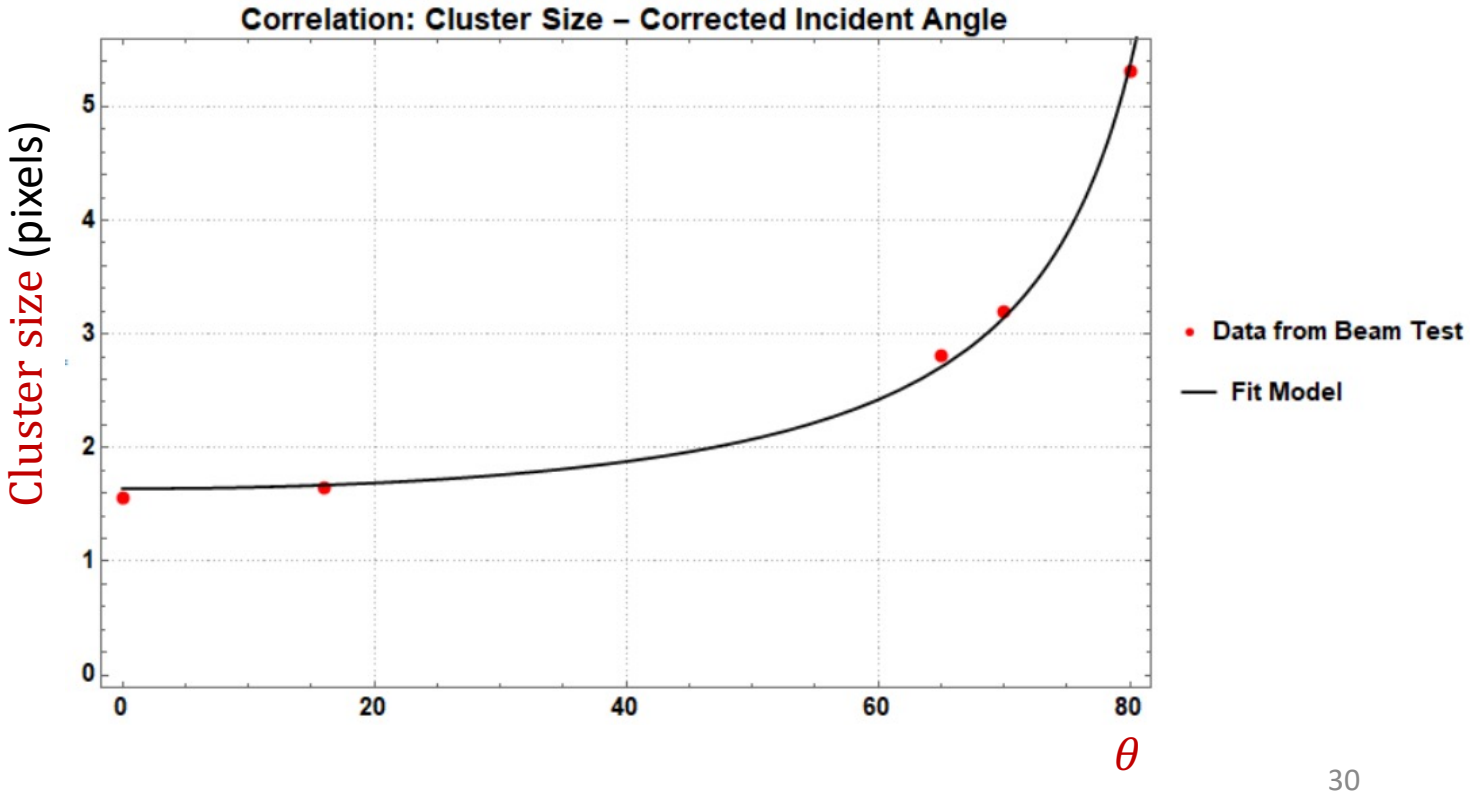


Long barrel : cluster size vs incident angle



Cluster size $= a \times sec\theta + b$

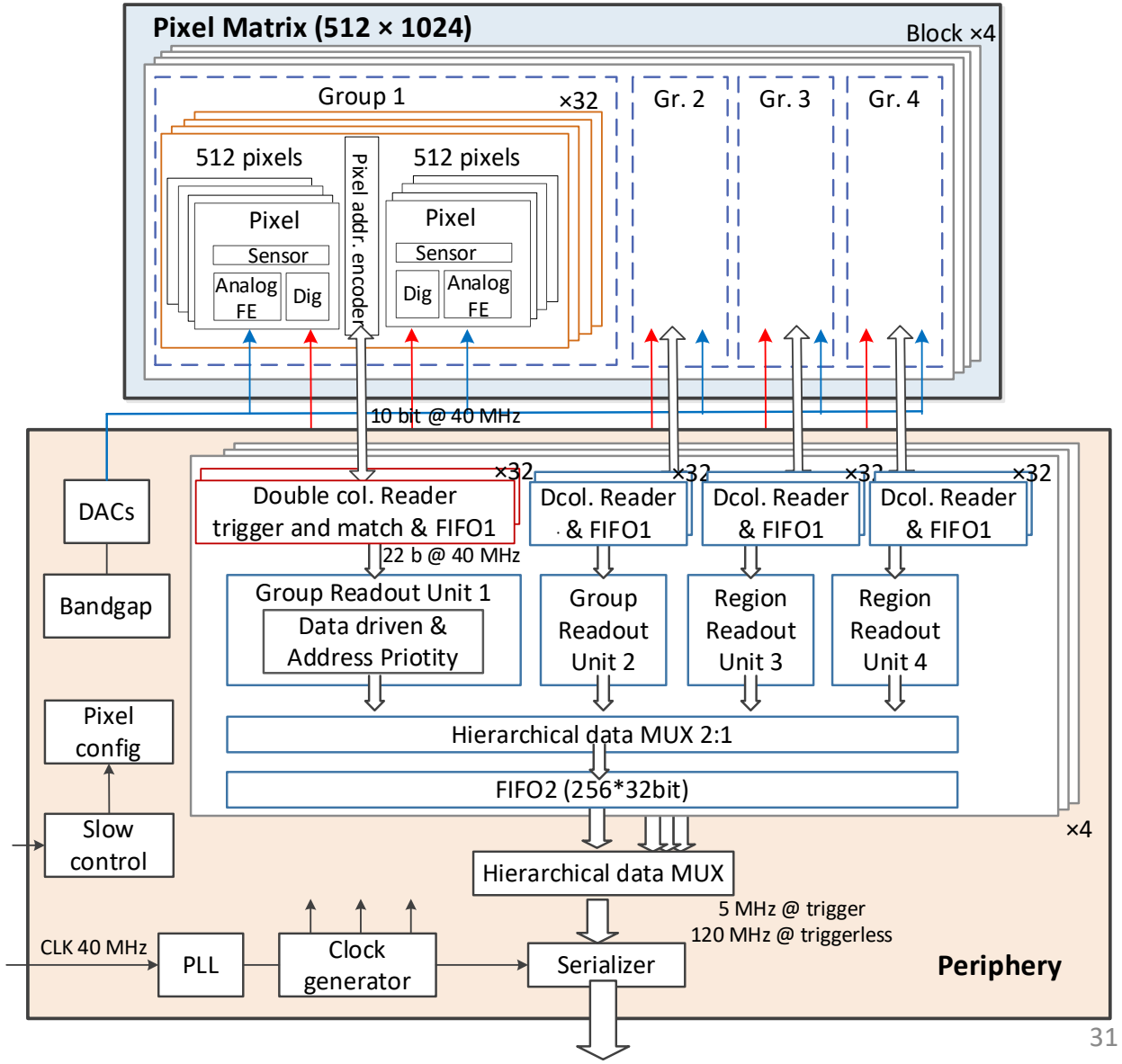




TaichuPix design

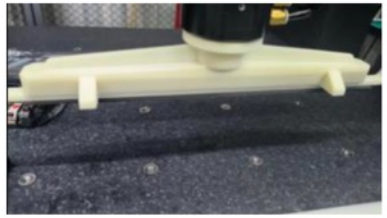
- Pixel design: 25 μm × 25 μm
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- Column-drain readout for pixel matrix
  - Priority based data-driven readout
  - Readout time: 50-100 ns for each pixel
- 2-level FIFO architecture
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate
  - between core and interface
- Trigger-less & Trigger mode compatible
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp

  only matched event will be readout
- Features standalone operation
  - On-chip bias generation, LDO, slow control, etc

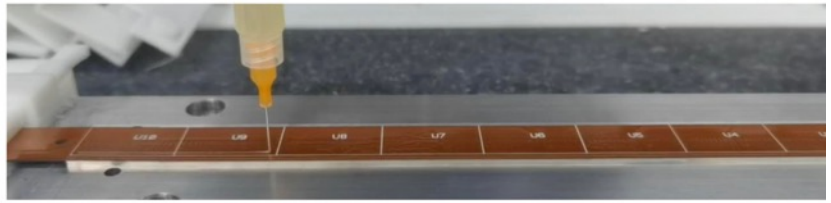


TaichuPix3 vertex detector prototype

New pickup tools

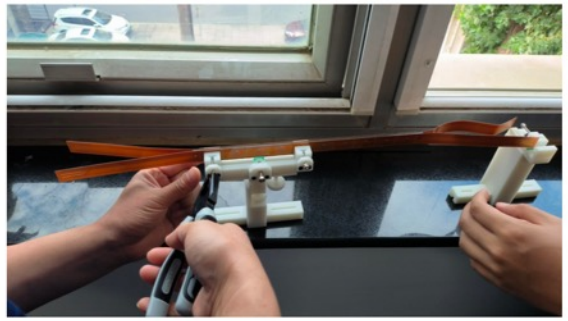


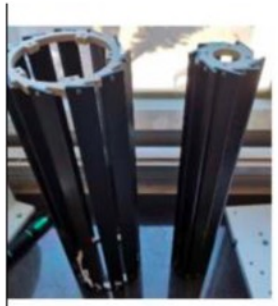
Dummy ladder glue automatic dispensing using gantry

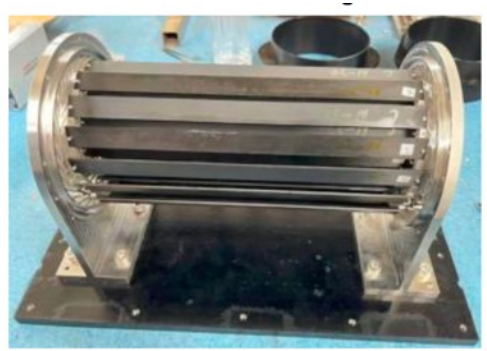


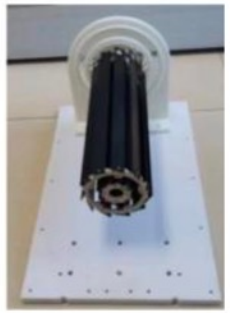
Ladder on wire bonding machine

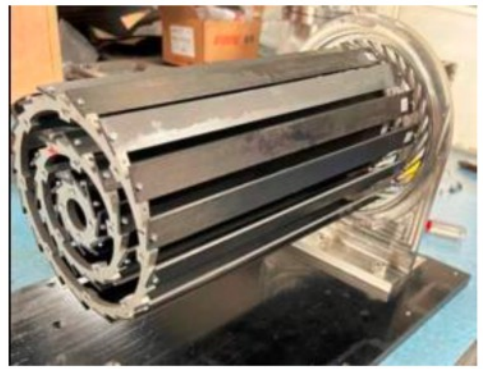
Dummy Ladder on holder



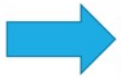








Ladder support tools



Ladder loaded on vertex detector

The first vertex detector (prototype) ever built in China