A large dynamic range front-end readout circuit based on first-order Delta-Sigma modulation for Calorimeters

Lanzhou Heavy Ion Accelerator (LHIA) is the highest energy heavy ion accelerator in China. The instrument is equipped with a variety of detectors to minimize systematic errors in external target experiments, among which the zero-angle Calorimeter is one of the most important sub-detectors to accurately measure the arrival time, energy and position information of the particles.

The readout systems of the Calorimeter are confronted with the dual challenges of unpredictable particle responses and nanosecond-scale signal fluctuations. Attaining a resolution below 5%, a dynamic range of 60 dB with low power consumption continues to pose significant technical challenges. This study is grounded in the architecture of first-order Delta-Sigma Modulation (DSM), including an integrator, a comparator, a latch and a Time to Digital Convertor (TDC), realizing real-time readout of charge signals with a dynamic range of 160 fC-160 pC. To enhance the time resolution， energy resolution and low power, a two-step TDC has been developed to achieve a better compromise between resolution and dynamic range. It comprises a counter-type TDC and a delay chain TDC circuit as coarse and fine counts separately. The dynamic range of the TDC is about 640 ns with a LSB of 70 ps, and a measurement error of less than 1.3 LSB, with an rms value of about 3 ps. The preliminary test results show that the total energy nonlinear error is less than 3.81% which is encouraging. The total power consumption is about 6.12 mW using 180nm CMOS process.

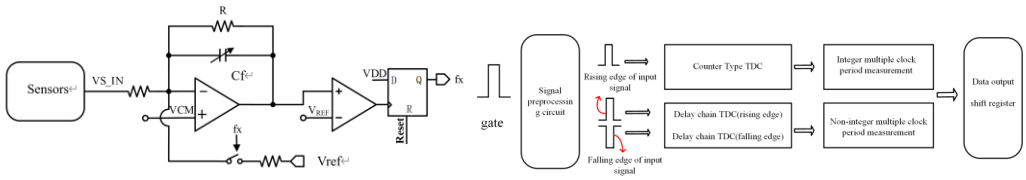

Figure 1 Left：the Front-end readout circuit including an integrator, a comparator and a latch, feedback capacitor Cf adjusts the amplification factor to expand the dynamic range, and the Vref is used to adjust whether positive or negative pulses are received. Right：diagram of the two-step TDC circuit.

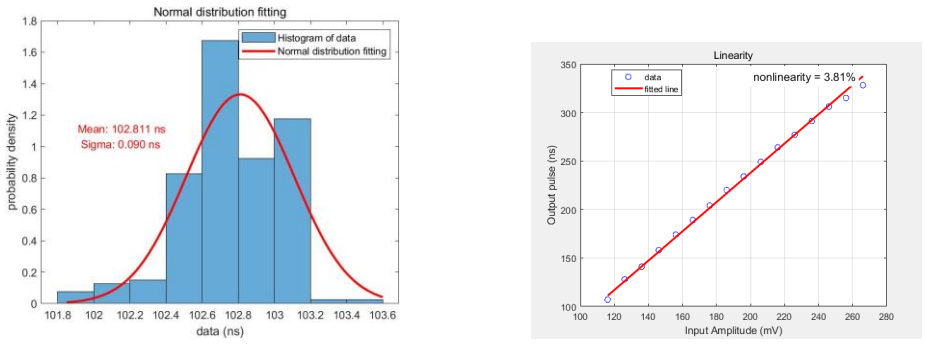

Figure 2 Test results. Left：resolution of the TDC circuit which is about 90ps. Right：the total nonlinear error is less than 3.81%, including the integrator, comparator, latch and TDC.