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Evaluation of Radiation-Tolerant Photodiodes for CMOS Image Sensors

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Motivation and Challenge

浙江大学 ZHEJIANG UNIVERSITY

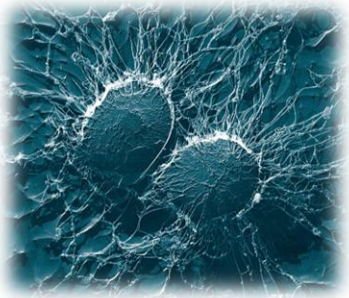
Medical **Space** **Biology** **Particle Physics** **Nuclear Power Plant**

Medical CT

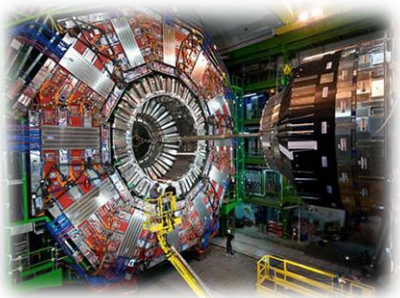
Space Station

Mars Rover

Electron Microscope



Particle Collider



Thermonuclear Fusion Reactor

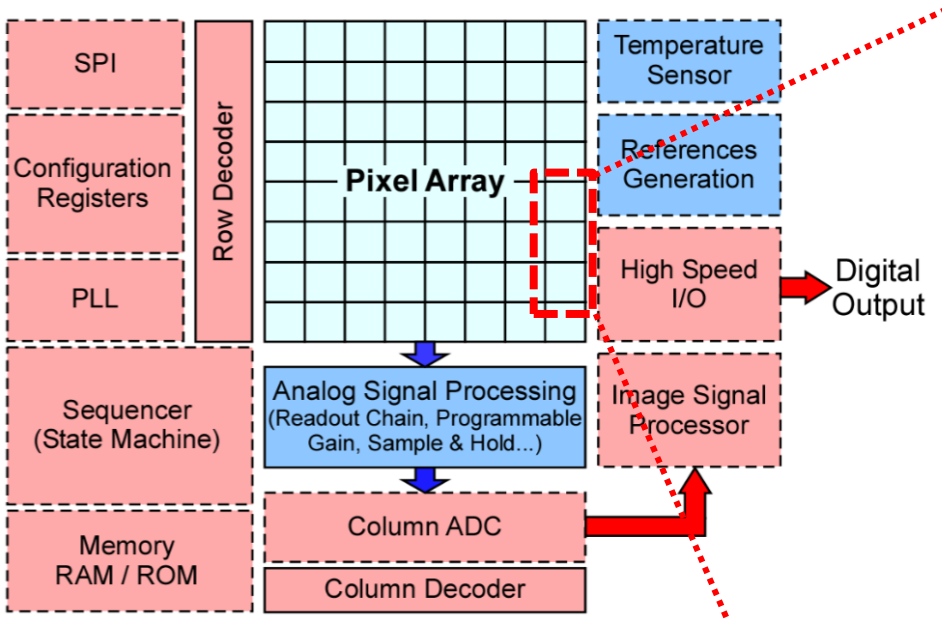
10rad **1krad** **10krad** **100krad** **1Mrad** **10Mrad** **100Mrad** **1Grad**

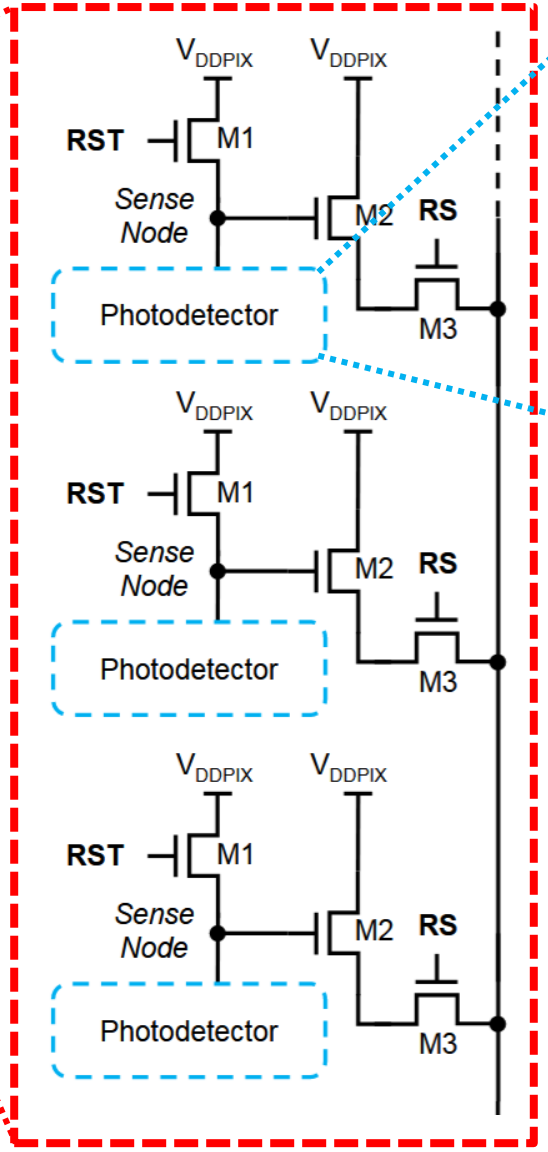
Safe to humans

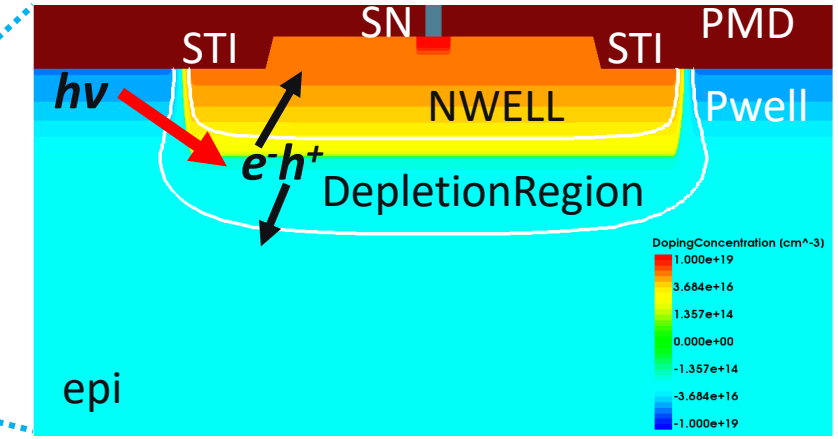
Commercial Camera

Radiation-hardened CMOS Image Sensors are critical for applications where humans cannot safely go!

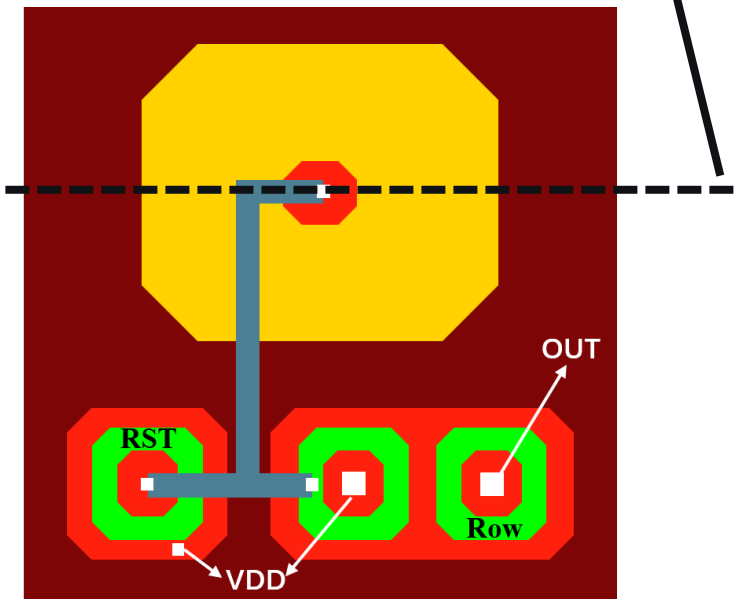
Typical CIS architecture[1-2]







PD Cross Section

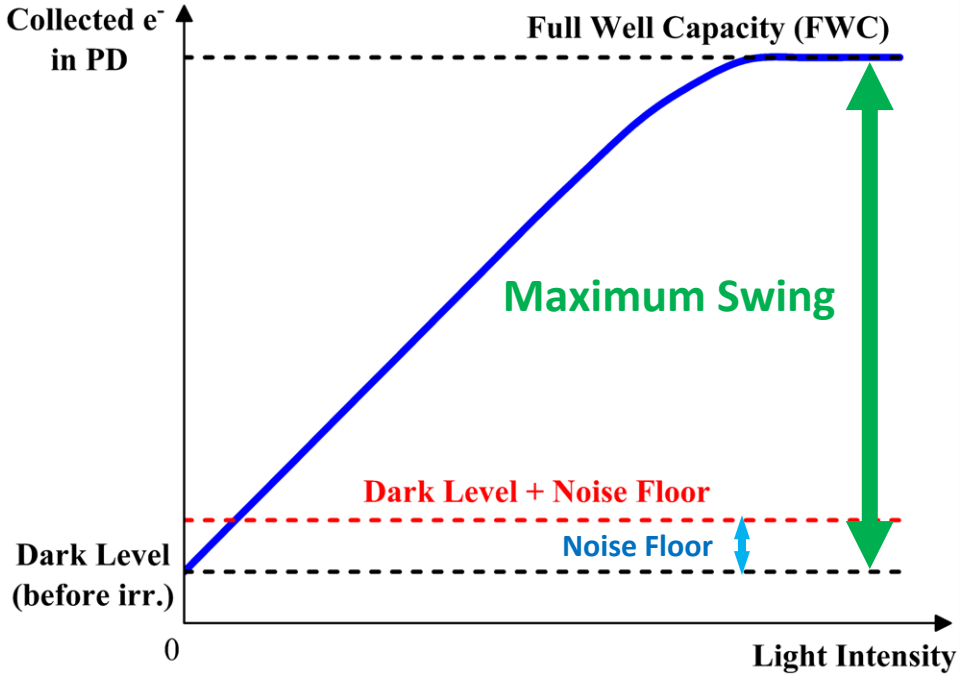


Top View

- Photon-to-Charge, Charge-to-Voltage Conversion
- Signal Readout
- Analog-to-Digital Conversion
- Data Processing and Transmission

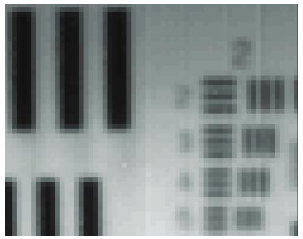
Photodiode Performance Degradation

Dynamic Range: Ratio of the maximum to the minimum measurable light intensities

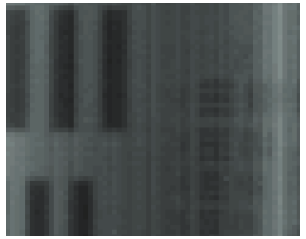


$$DR = 20\log\left(\frac{\text{Maximum Signal}}{\text{Noise Floor}}\right)$$

$$= 20\log\left(\frac{\text{Maximum Swing}}{\sqrt{\sigma^2_{readout} + \sigma^2_{darkCurrent}}}\right)$$

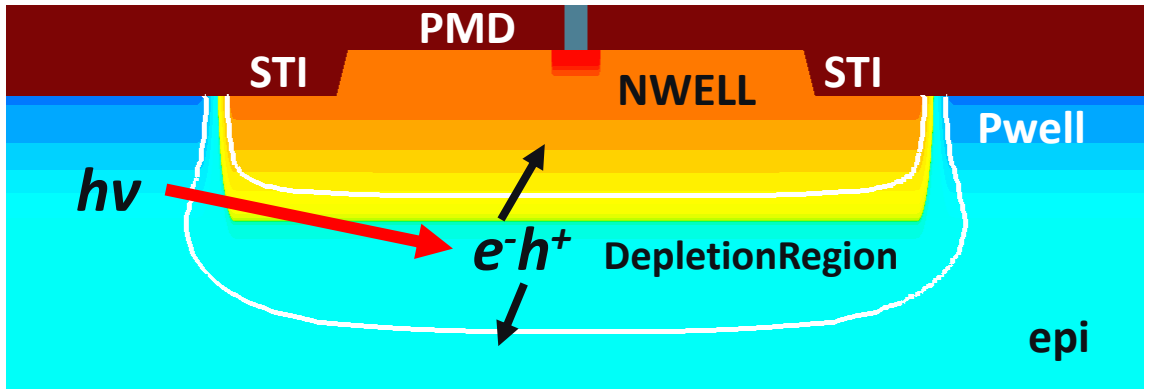


Pre rad



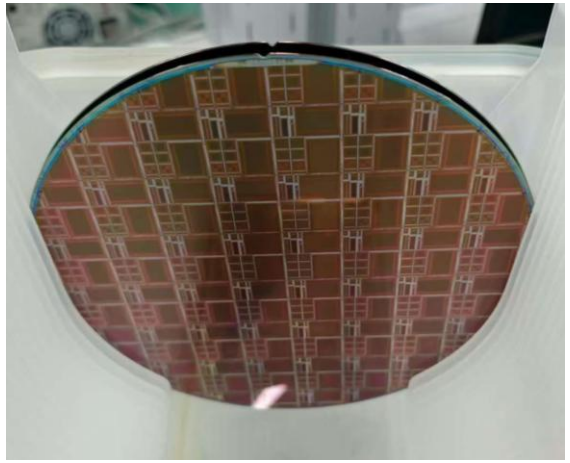
100 Mrad (SiO2)

PD Degradation Caused by TID[3]

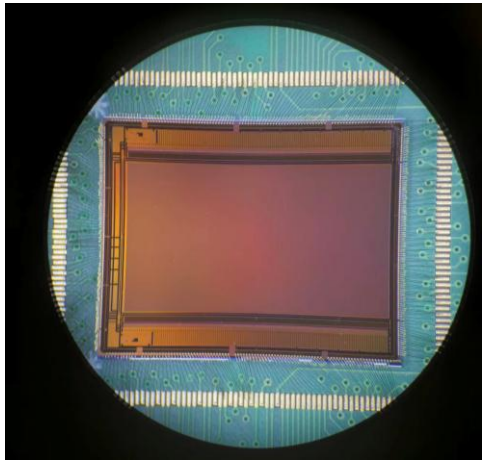


- **Total Ionizing Dose** — **Inducing high dark current!**
- Displacement Damage Effects
- Single Event Effects

Overview of the Engineering Sample Chip



Silicon Wafer



Full-sized sensor

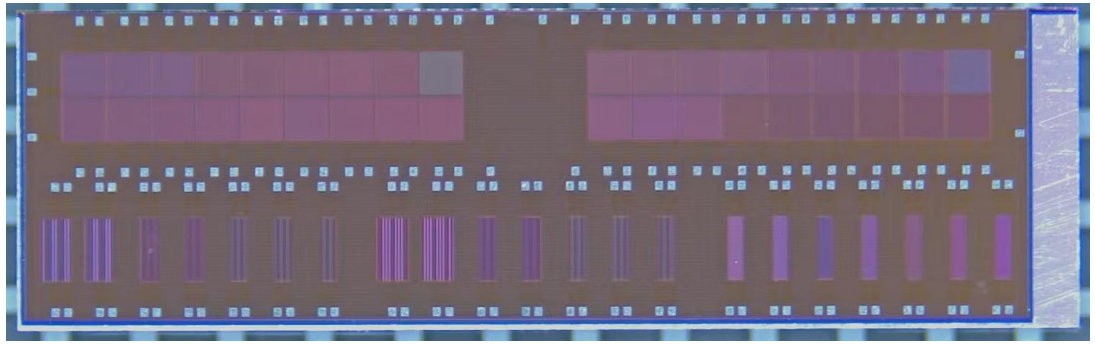


Photo of the passive arrays (2.5 mm × 8 mm)

RadHard sensor fabricated with a 180 nm CIS process, include:

- Two 1280×720 full-sized sensor designs

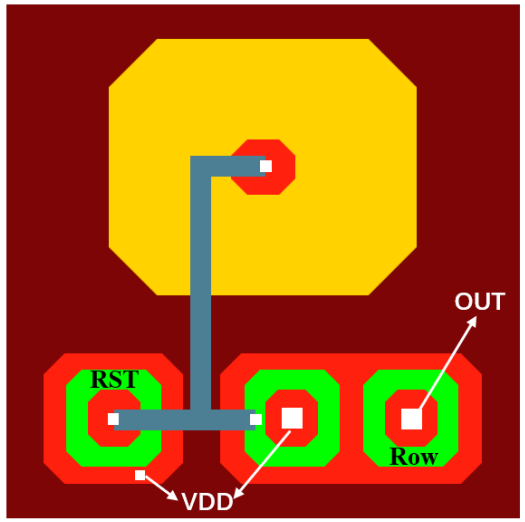
  See Pengxu Li's talk

- Six 256×256 test pixel arrays
- Passive photodiode arrays

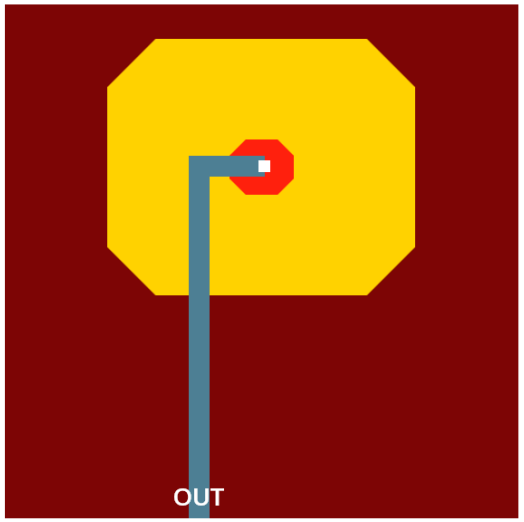
  Main foucs of today's talk

Several PD structures are inspired by the pioneering work[2-8] of V. Goiffon et al.

Passive Arrays



Active pixel



Passive pixel (10 µm × 10 µm)

- Designed dedicated passive photodiode arrays for **direct assessment of the induced dark current** after being exposed to different TID radiation levels

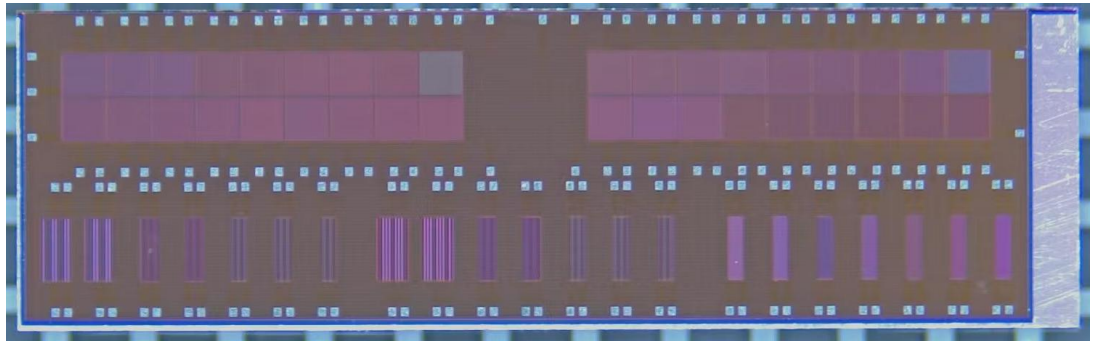
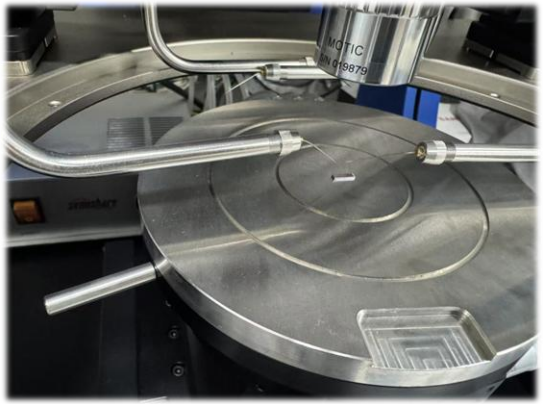
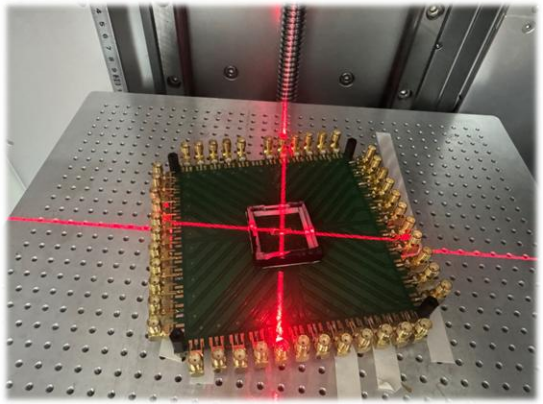


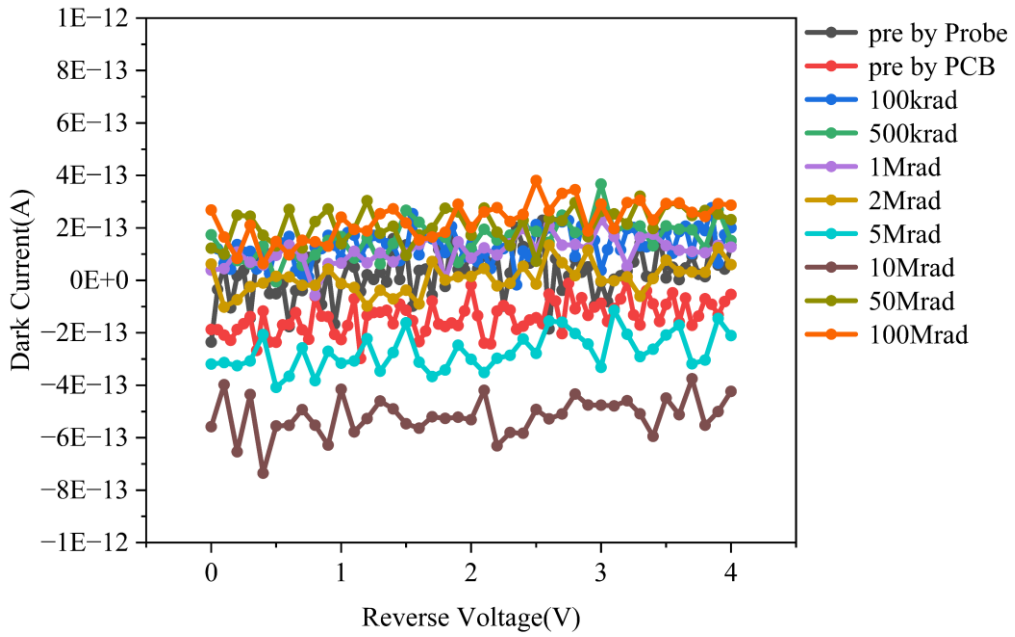
Photo of the passive arrays (2.5 mm × 8 mm)

- Each individual photodiode array consisting of **1024 (32×32)** pixels, they are read out in parallel

Experimental Setup



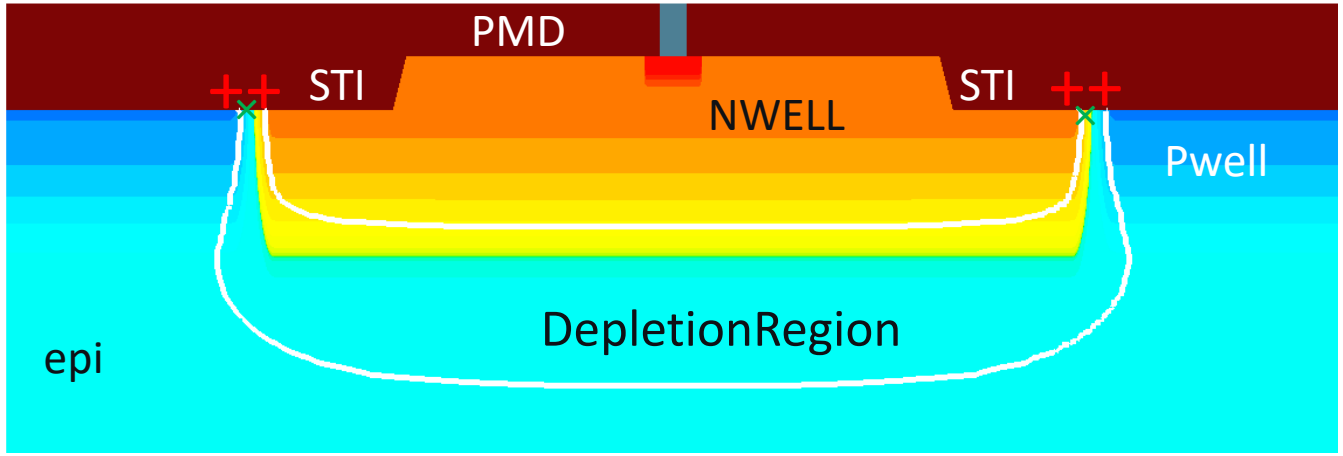




Background bias current

- Dark current measured with bare chips using a probe station and also with chips wire-bonded to PCB with low leakage design; consistent results obtained for chips before irradiation
- Measurements repeated for bonded chips (powered off) after irradiation with **X-ray** machine up to **100 Mrad (SiO2)**
- Subsequent measurements **normalized by 1024** to represent the dark current of single photodiode

Dark Current in Photodiode



*STI = Shallow Trench Isolation
*PMD = Pre-Metal Dielectric

+: Oxide Positive Trapped Charge(N_{ot})
×: Interface Trap (N_{it})

Increases with TID

Surface as the dominant source of dark current, explainned by the **SRH mechanism**[1-2]:

$$I_{dark} \approx K \times N_{it} \times A_{dep} \times exp(E^{\alpha}) \times T^3 exp\left(\frac{-E_g}{kT}\right)$$

Constant

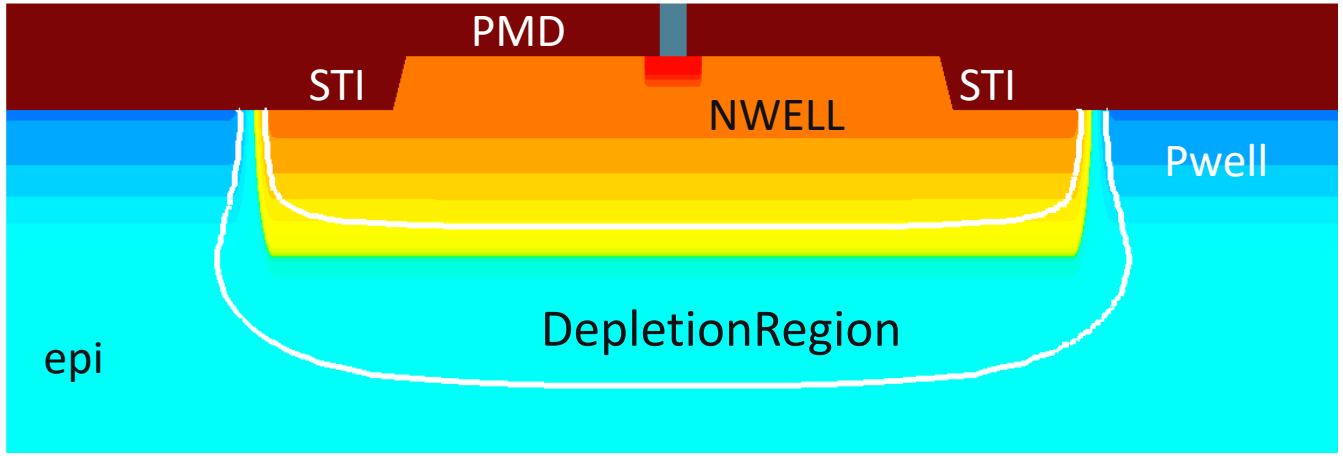
Interface trap density in SiO2/Si: **Replace it!**

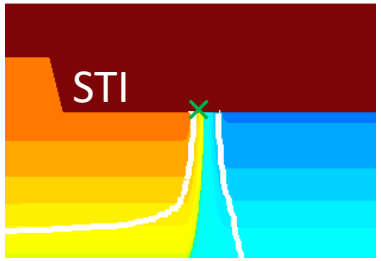
Depleted interface area: **Reduce it!**

Electric field enhancement factor: **Avoid it!**

T dependence:
≈ 2x increase per 8°C

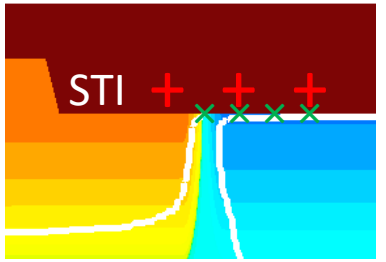
Standard Photodiode





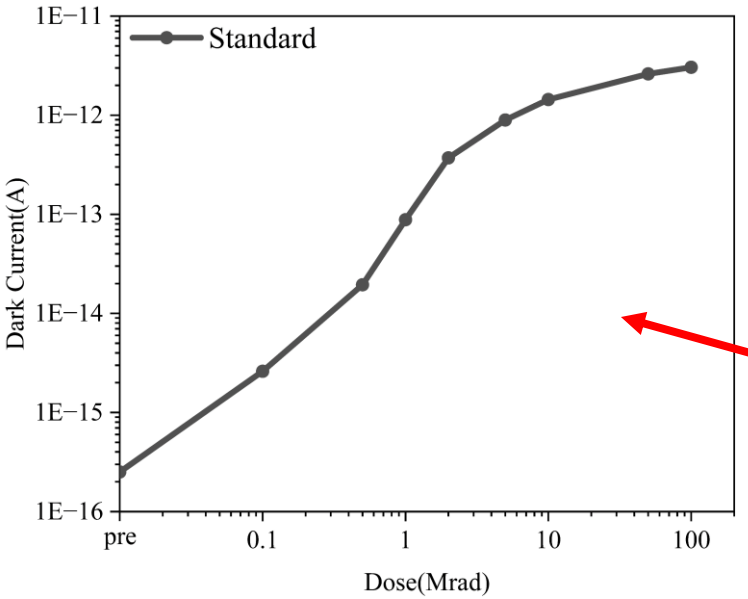
0 ~ 0.1Mrad

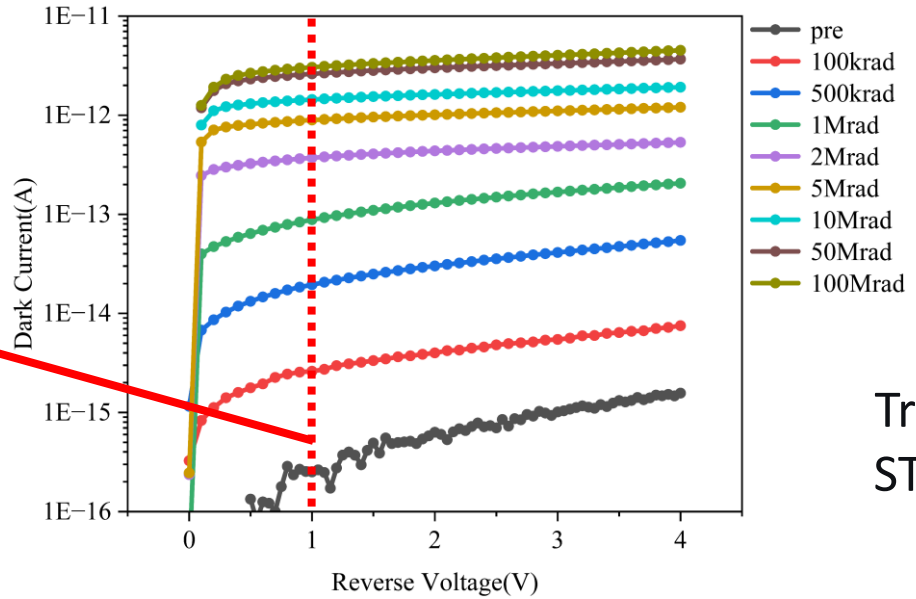
DC ∝ N_{it}

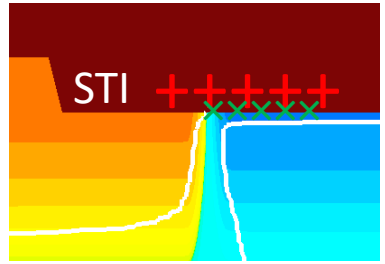


0.1 ~ 5Mrad

DC ∝ $N_{it} \times A_{dep}$





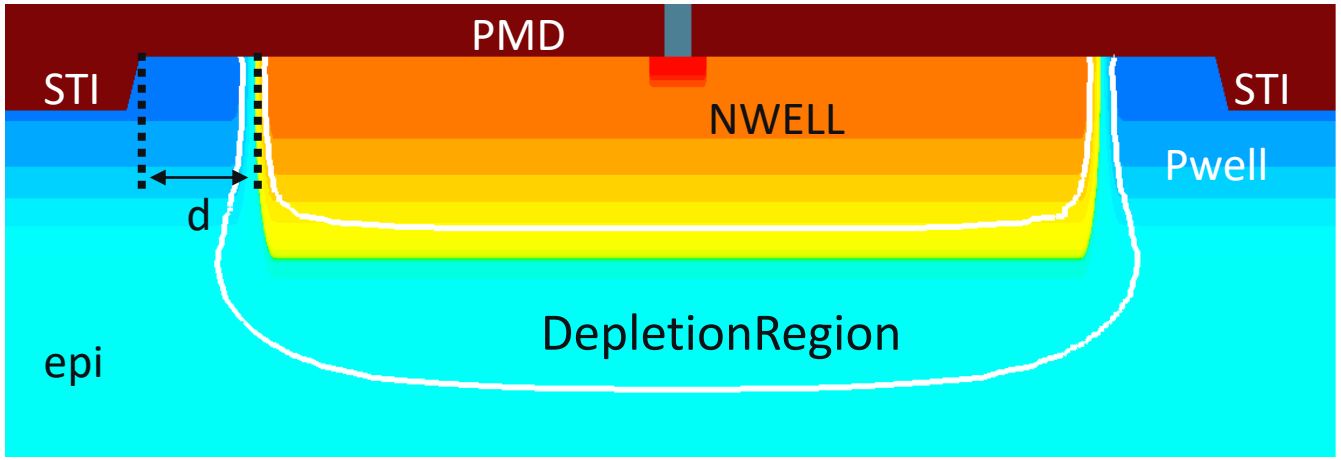


5 ~ 100Mrad

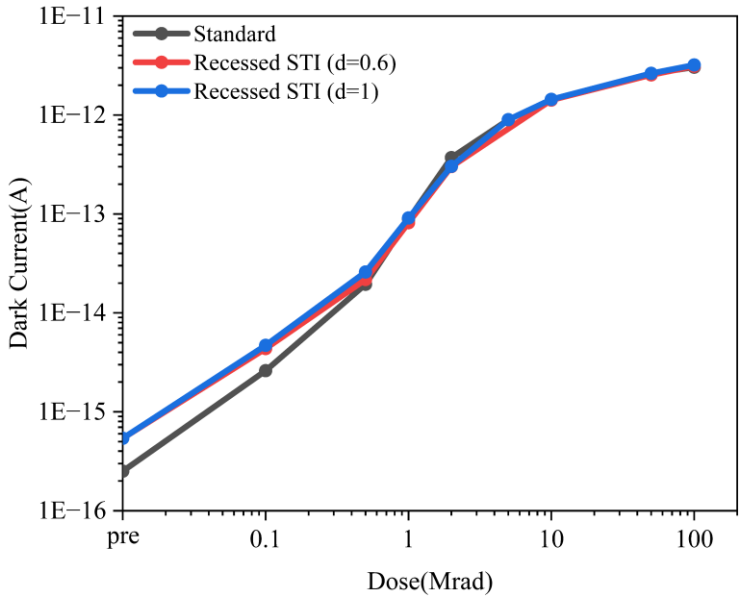
Trap density approaches saturation;

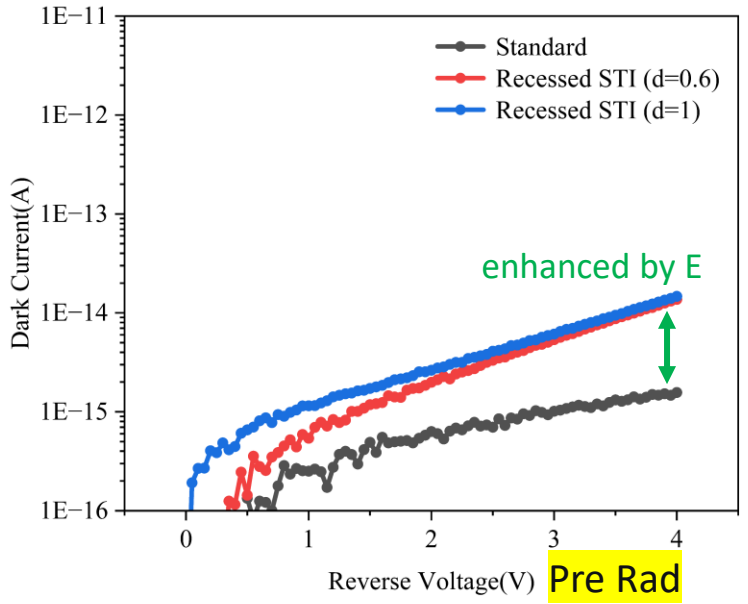
STI (N_{ot}) may lead to Pwell inversion and short-circuit

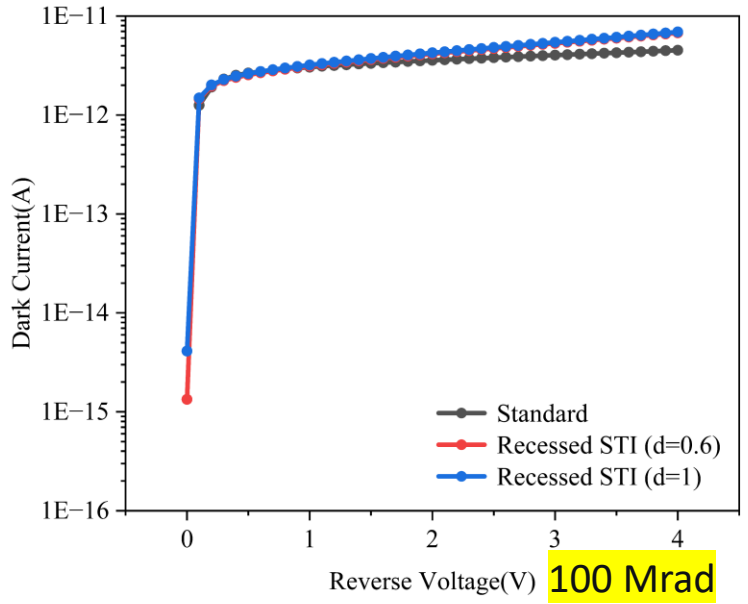
Recessed STI



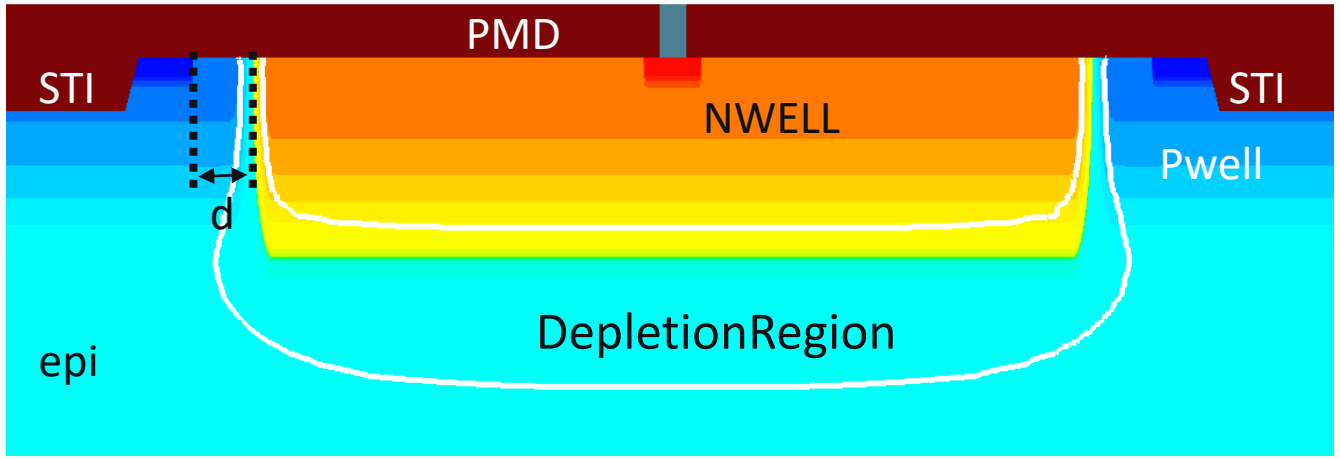
- **Replace** the Oxide in the depleted interface from STI to PMD
- The interface of PMD as dirty as the STI
- High E-field between the Nwell and surface Pwell



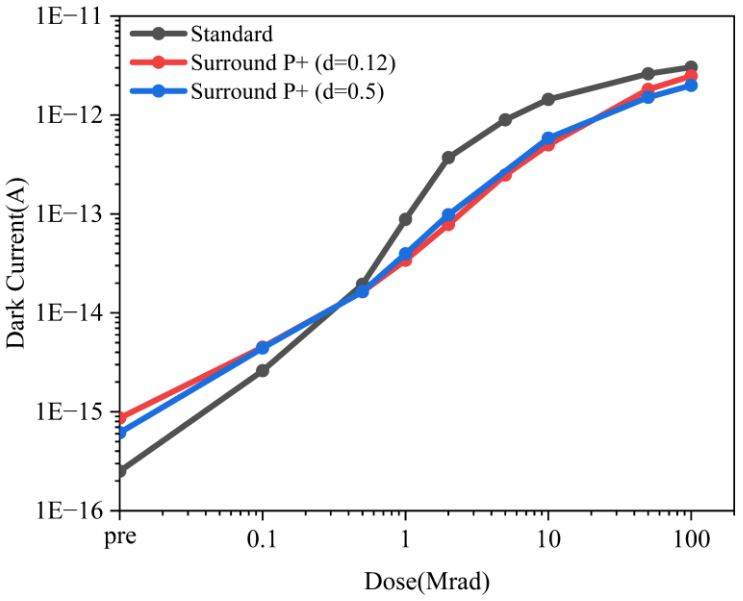


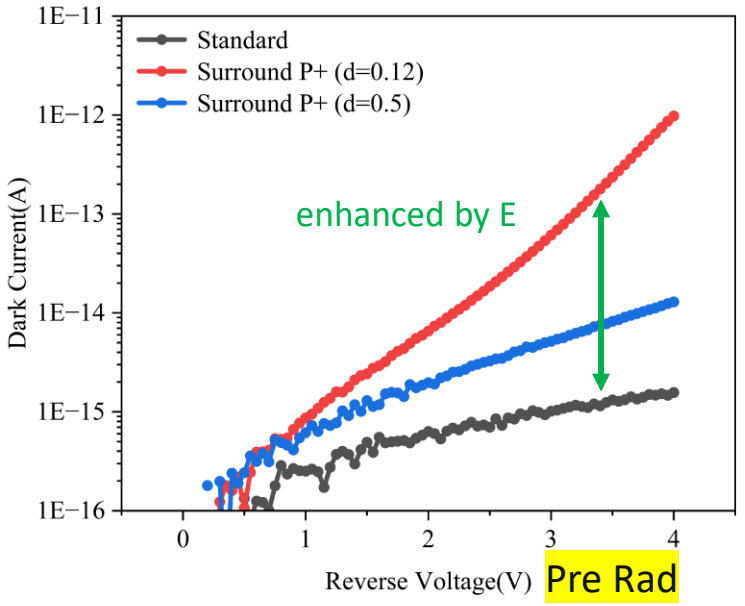


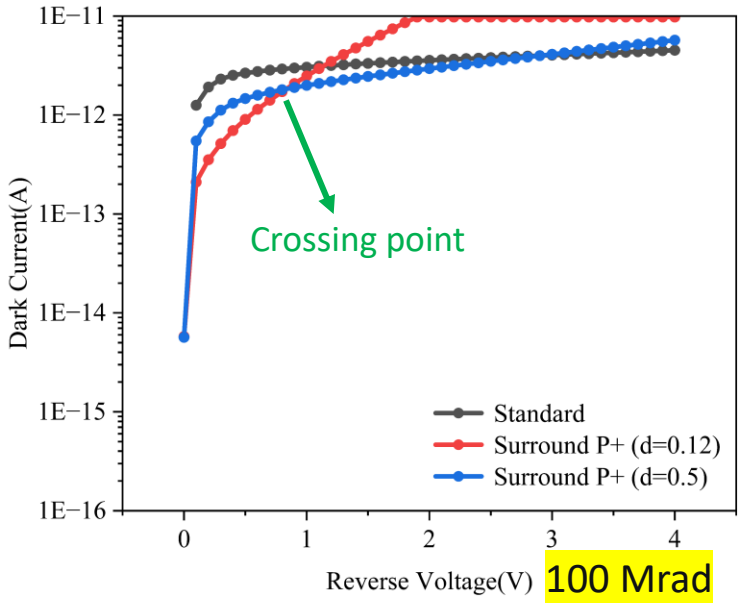
Surrounding Nwell by a P+ Ring



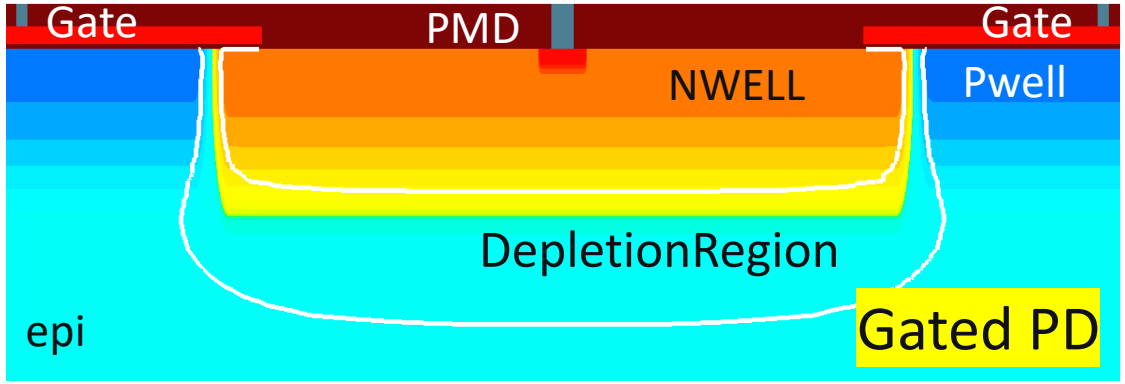
- **Reduce the A_{dep}** by P+ ring to prevent the depletion region from extending
- High E-field between the Nwell and surface P+

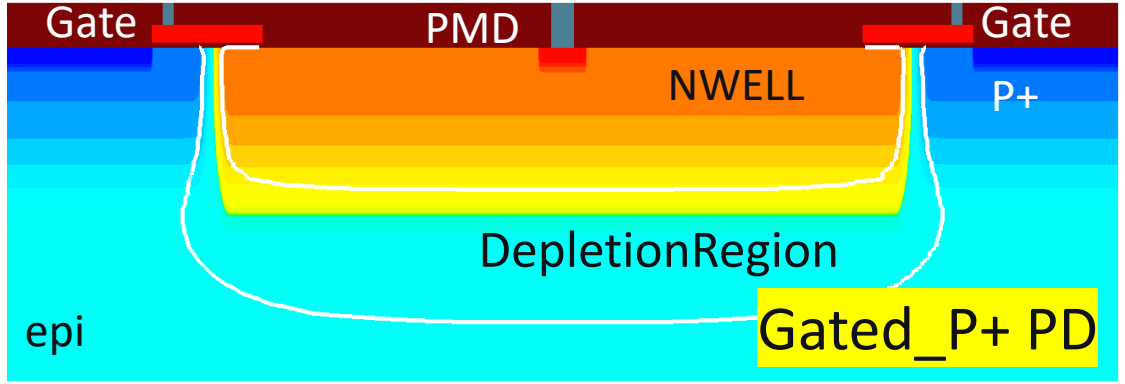


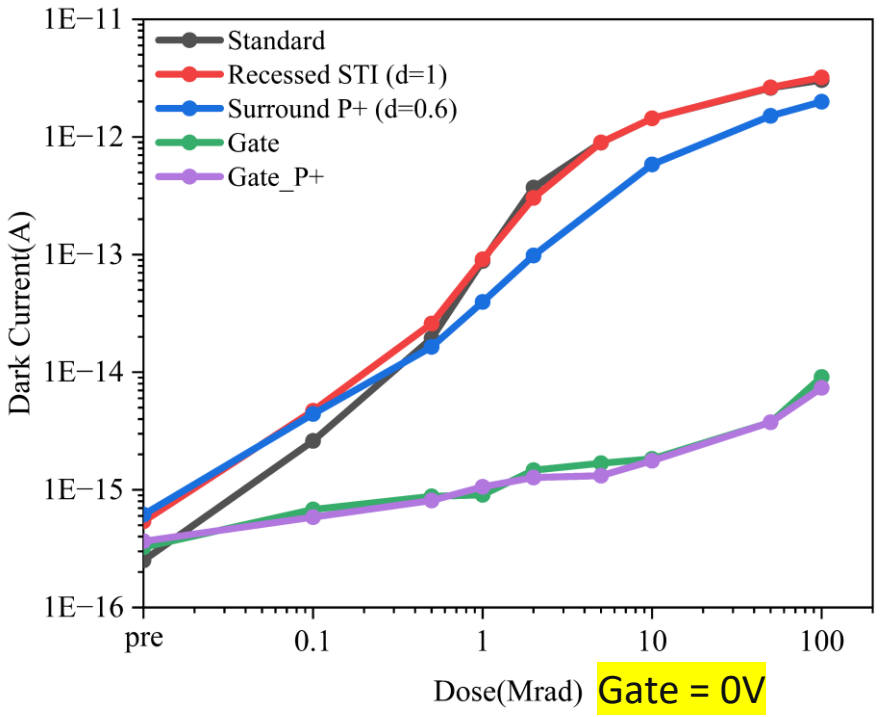




Gated Photodiode



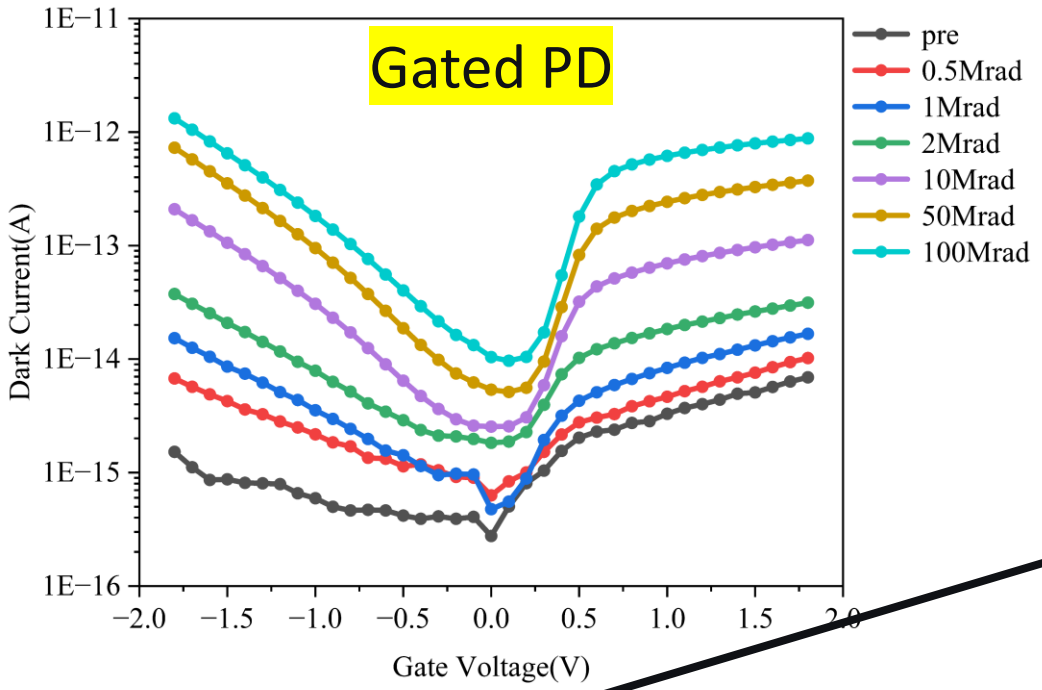


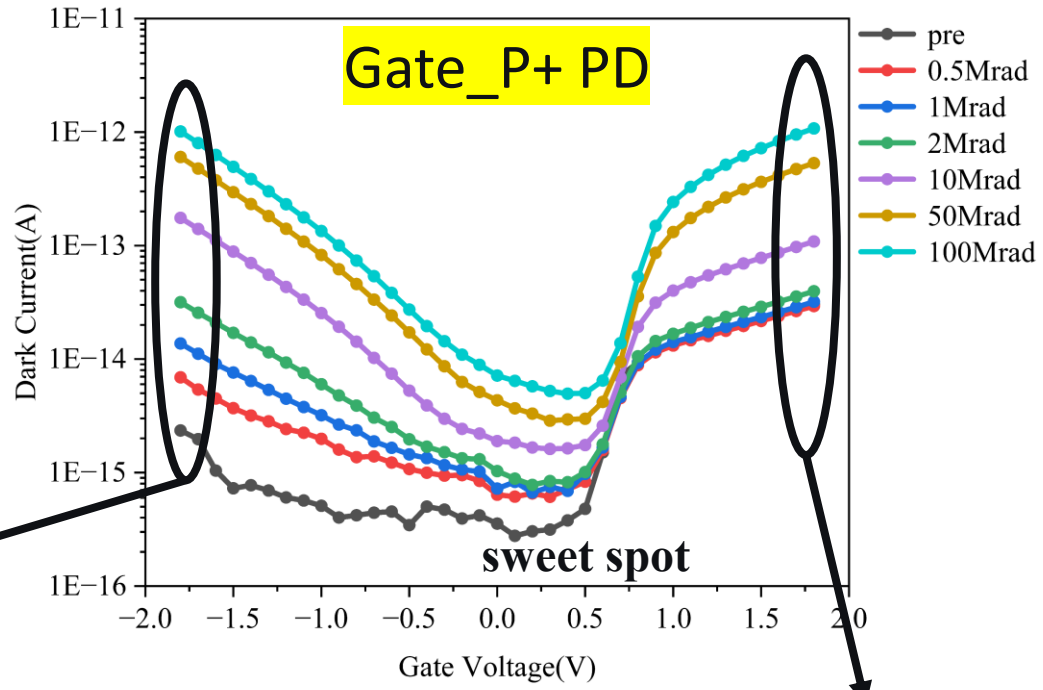


- Gate oxide: a much high purity oxide compared with STI and PMD
- The addition of a pure gate fully covers the depleted interface area A_{dep}, resulting in a significantly reduced N_{it} and little N_{ot}

A highly effective radiation-tolerant Photodiode at 100 Mrad

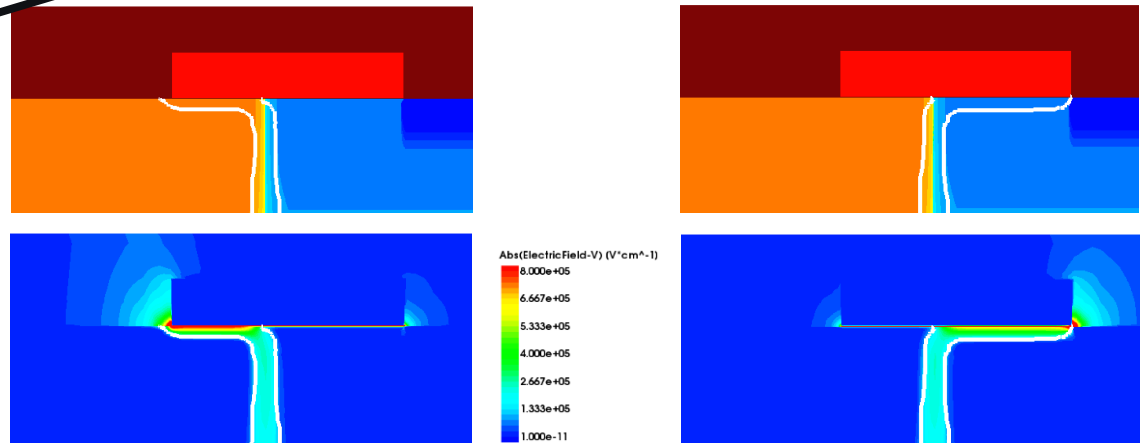
"U-Shaped" DC-Vg Curve





Gate = -2V

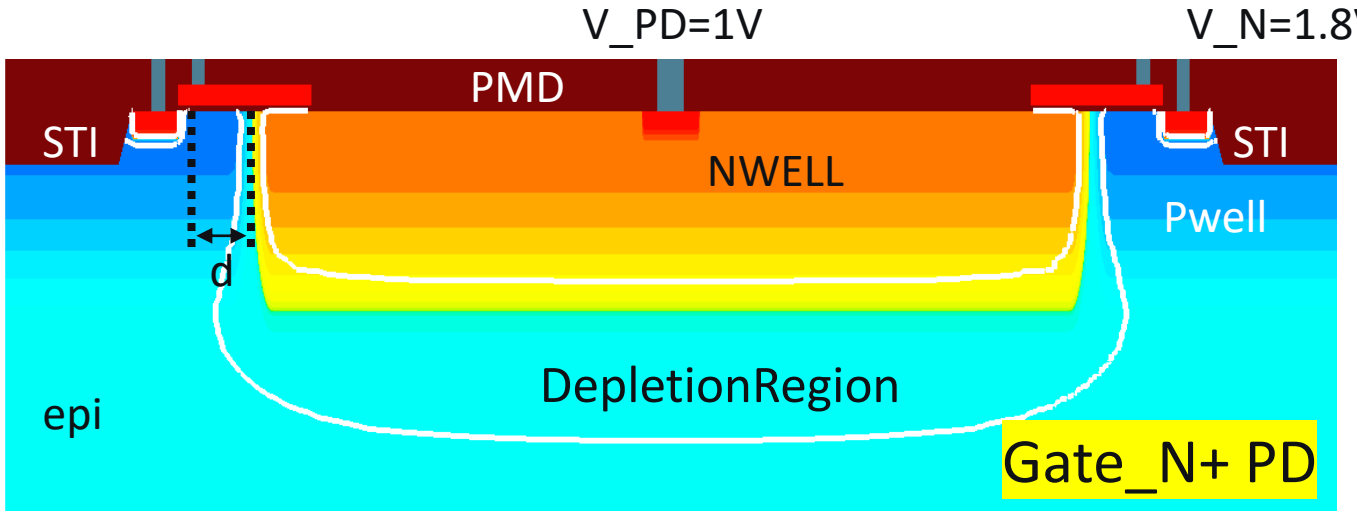
Trap assisted tunneling due to the band bending called **GIDL** (gate-induced drain leakage)



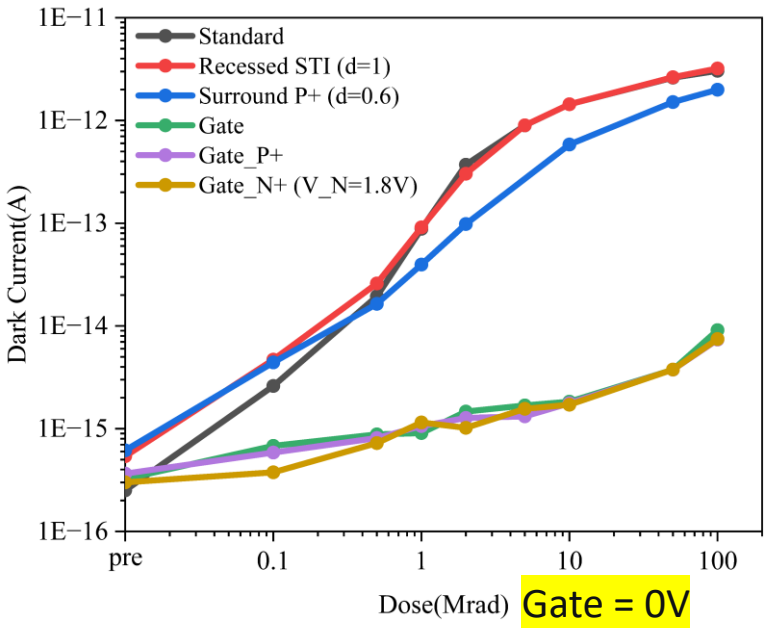
Gate = 2V

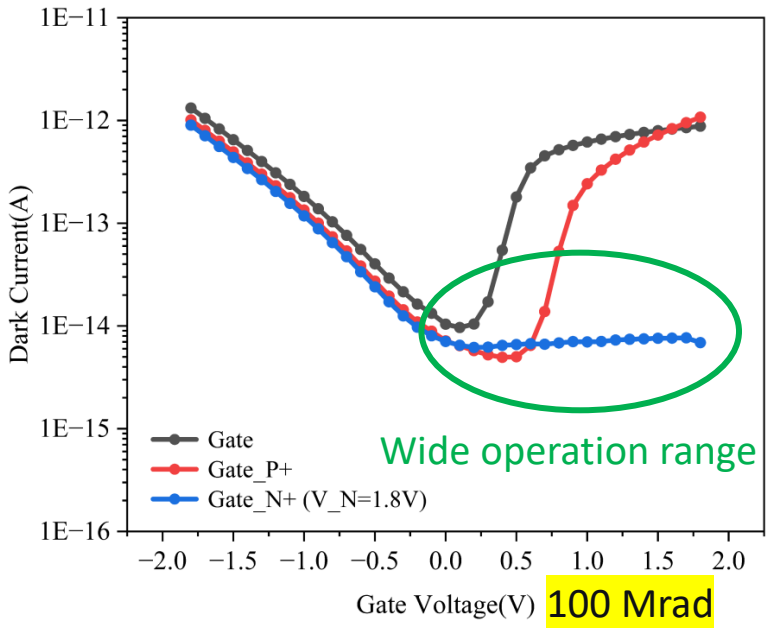
Enhancement of the **trap assisted generation** due to the high electric field region.

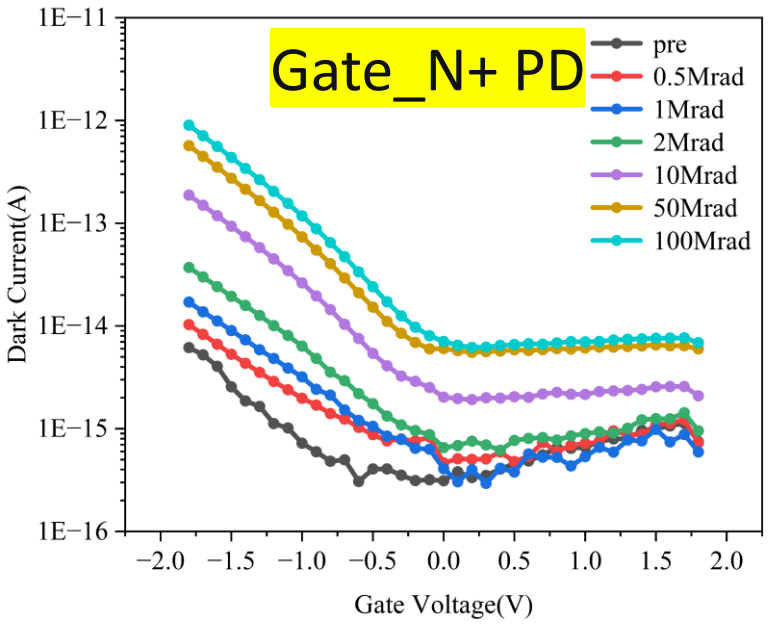
Replacing P+ with N+



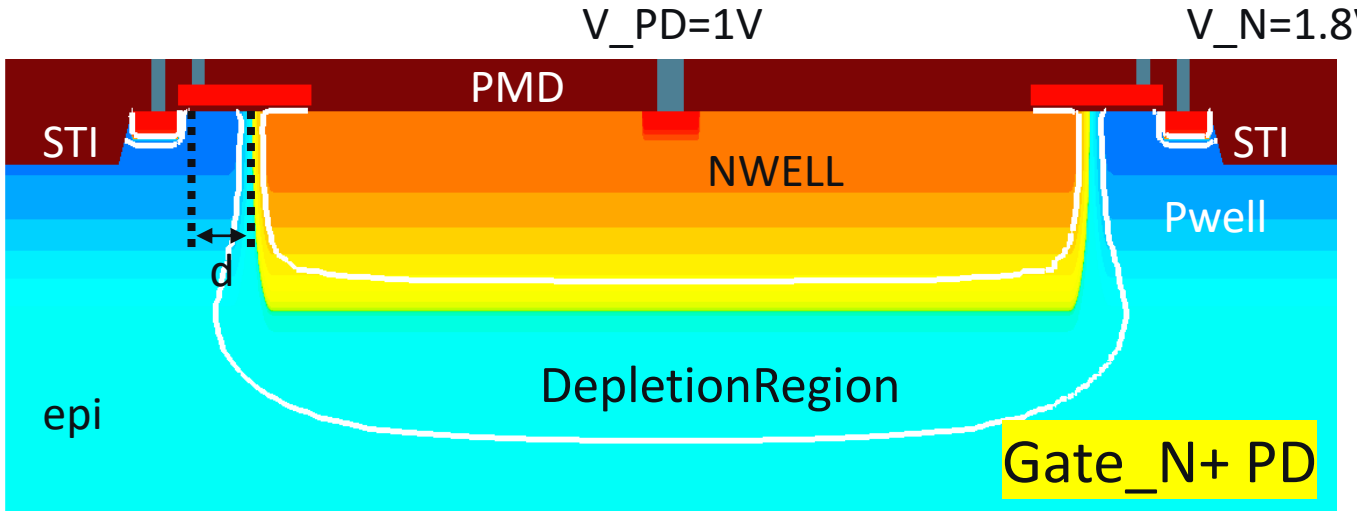
- Consistent trend across three gate structures: dark current maintaining a value around **10 fA** up to **100 Mrad**
- dark current of the Gate_N+ remains stable under positive gate bias at high TID level

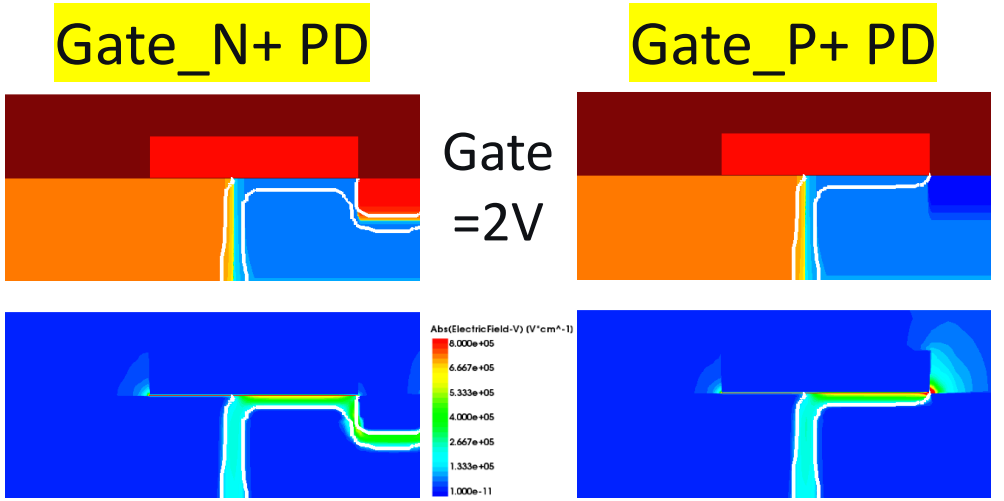


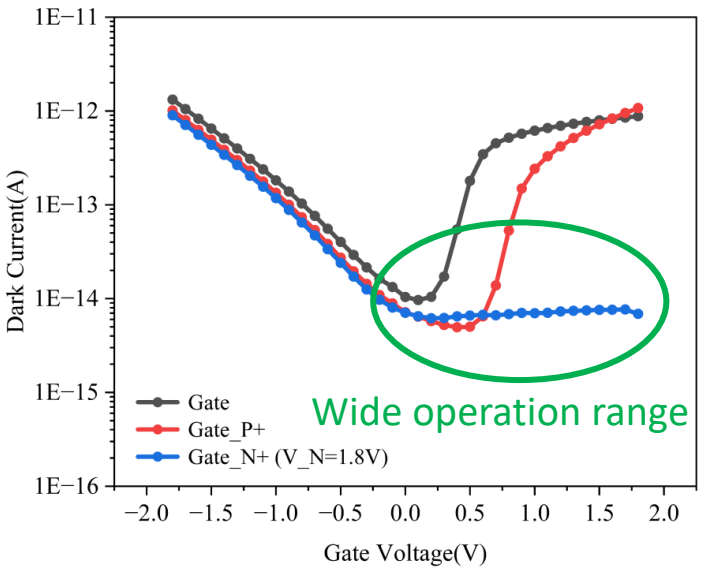




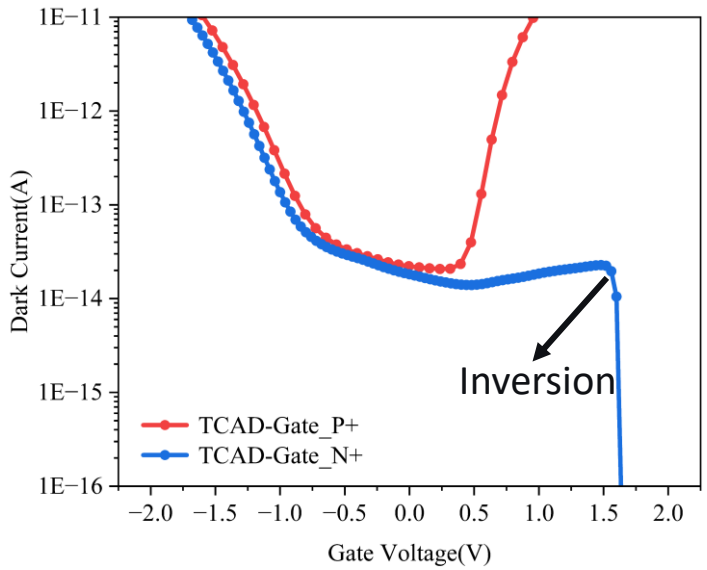
Mitigation of High E-Field







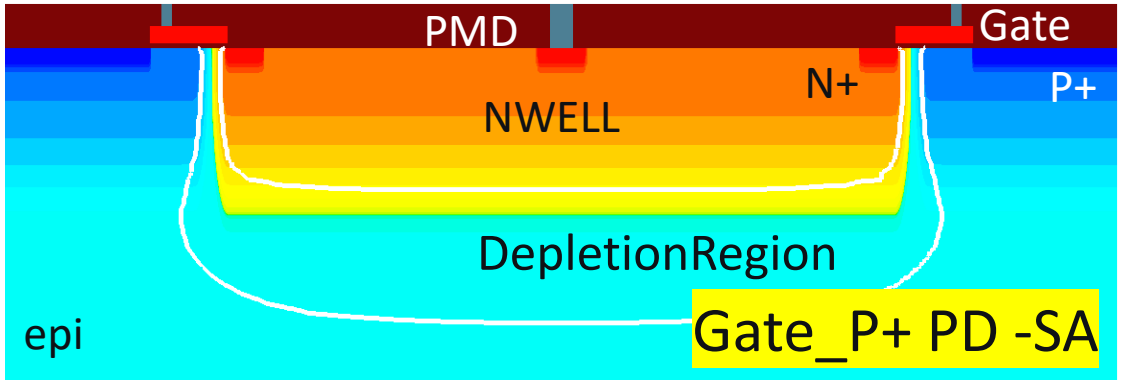
100 Mrad Experimental data

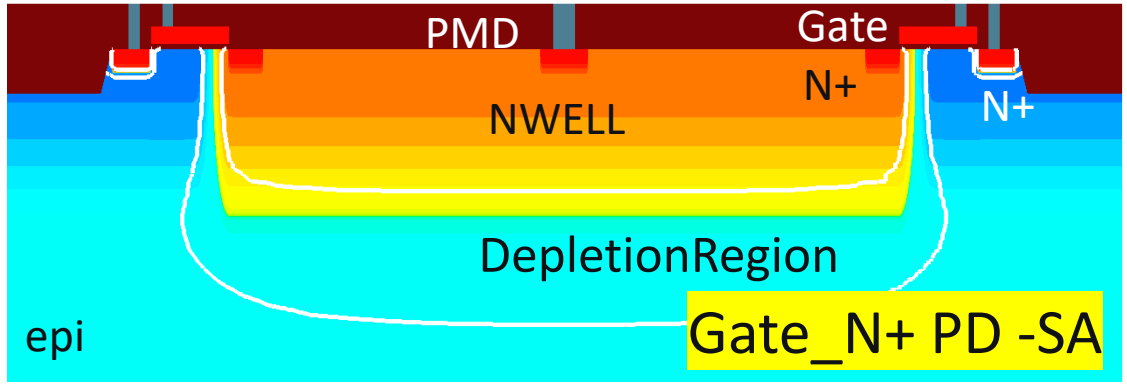


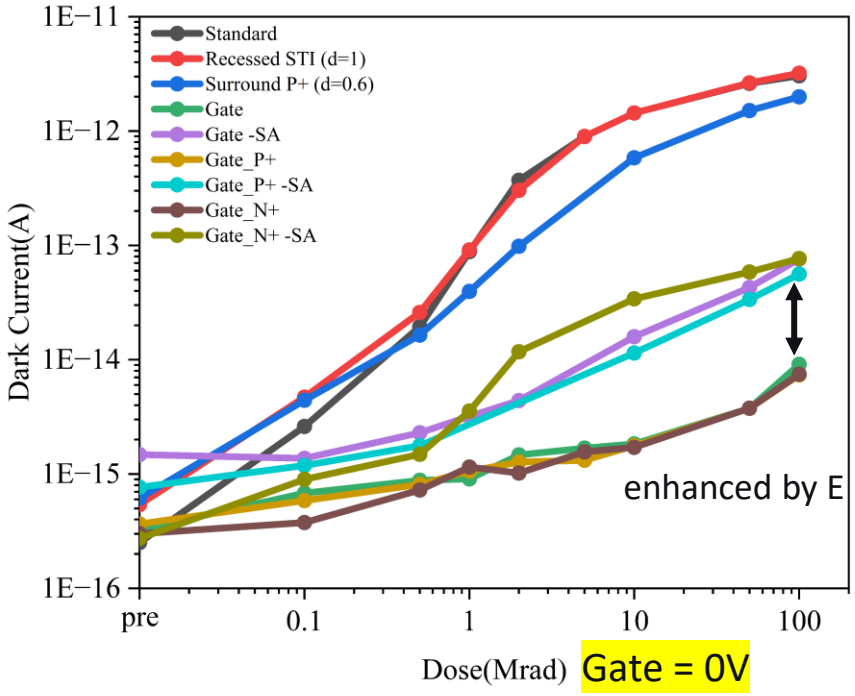
TCAD Simulation

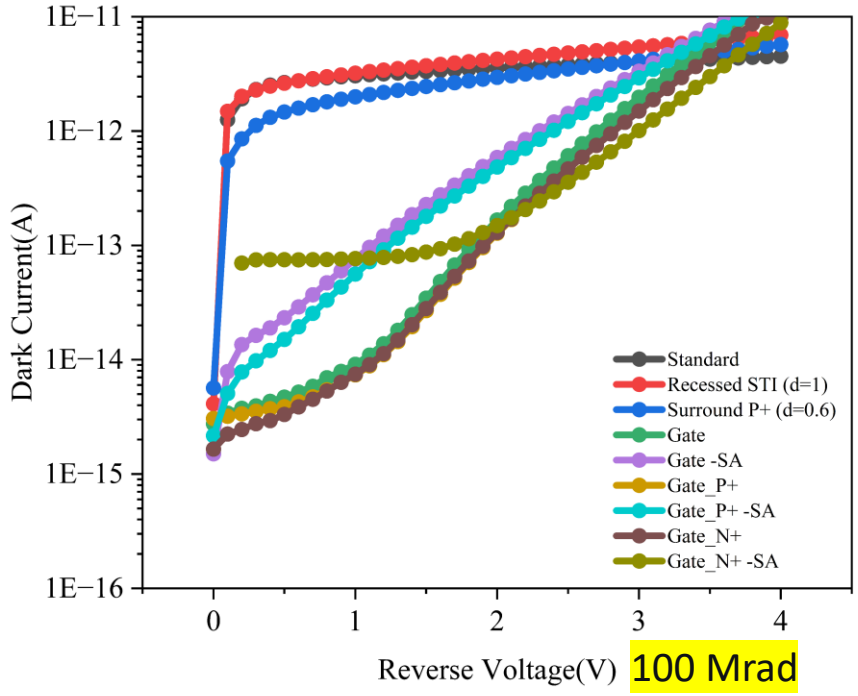
- The Gate_N+ PD structure capable of **suppressing local high E-fields** during positive gate bias
- Key optimization of "d": avoid premature P-well inversion

Manual or Self-Alignment?



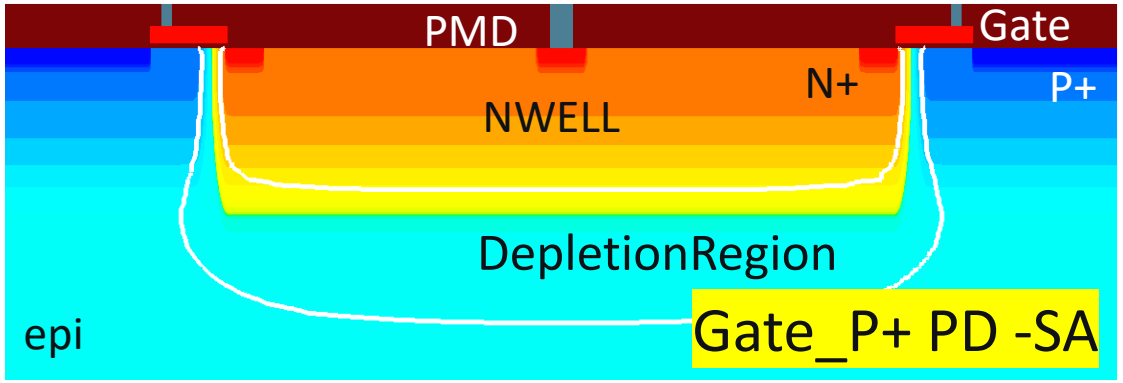


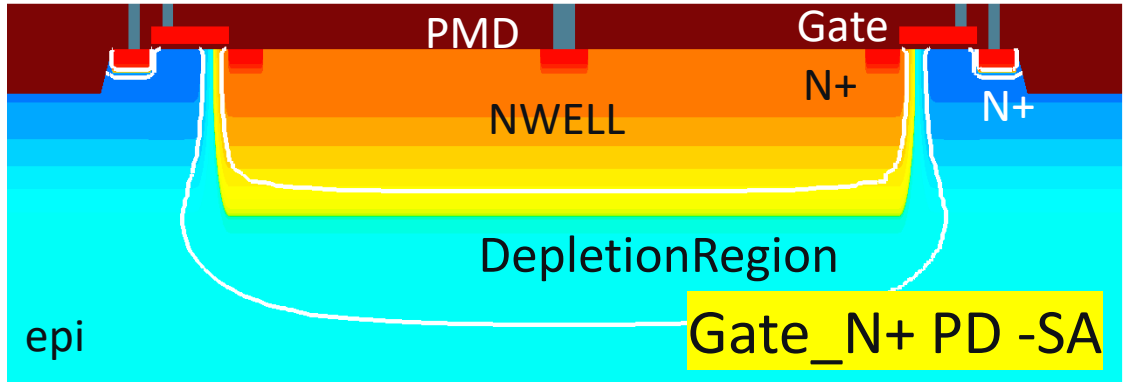


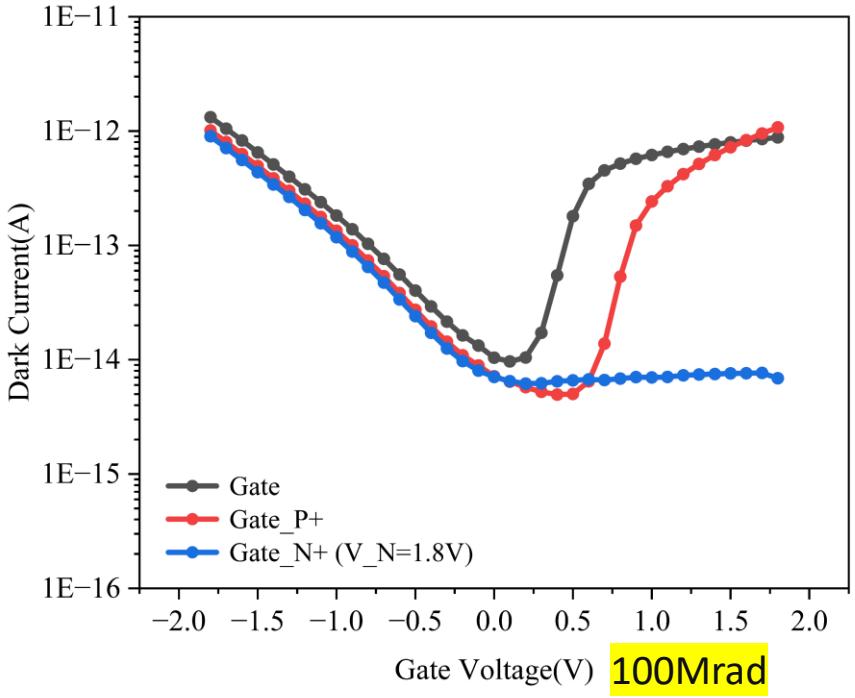


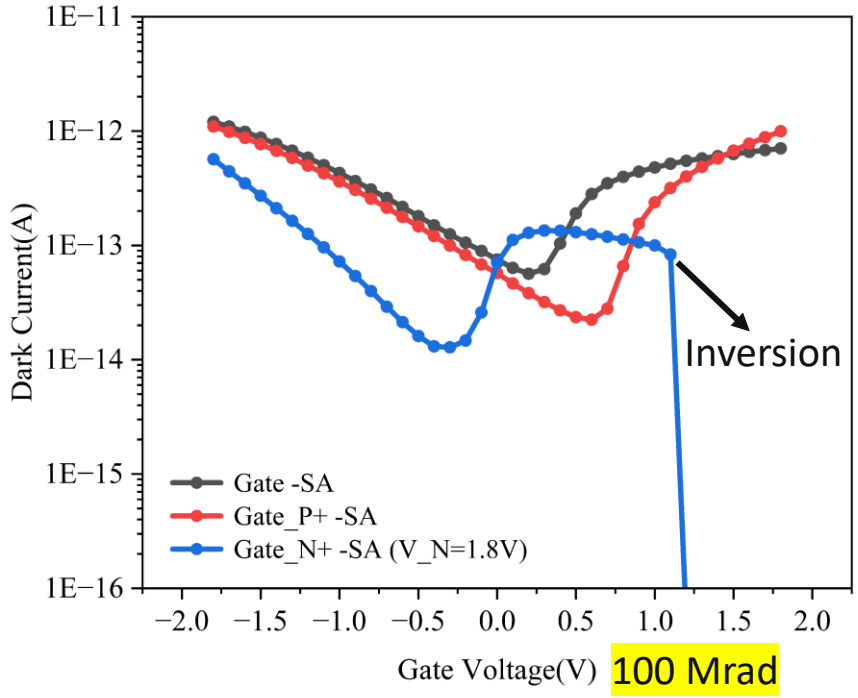
- The Self-aligned structure **ensures gate oxide coverage** of the surface depletion region (standard process), but at the cost of an enhanced electric field

Manual or Self-Alignment?









- Self-Aligned Gated PDs with still higher dark current than Manual Overlap at optimal operating voltage

Summary

- Evaluation of different Radiation-Tolerant Photodiodes:
  Gate > Gate-SA > Surround P+ > Recessed STI = Standard

- Gate_N+ Photodiode demonstrates the highest radiation tolerance (~10 fA at 100 Mrad) and remains stable under positive gate bias

- Future plan:
  - Perform irradiation testing up to 1 Grad (SiO2)
  - Extract the oxide charge and interface state densities at different dose levels, and establish a reliable model to assisit future designs

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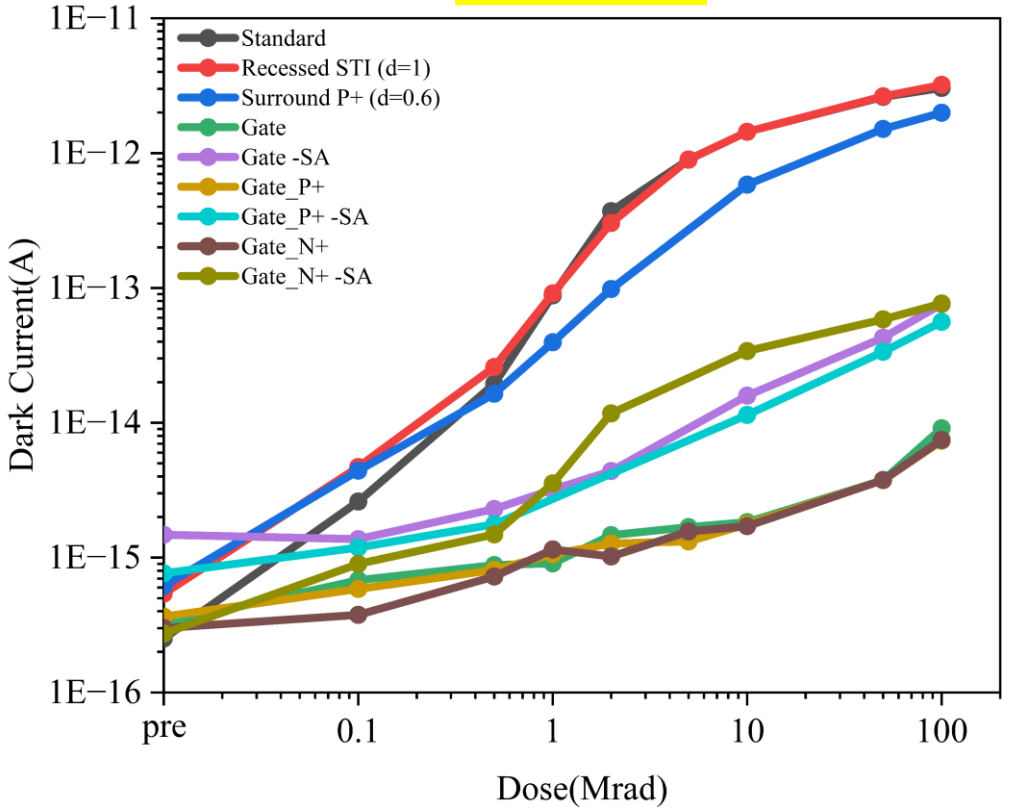
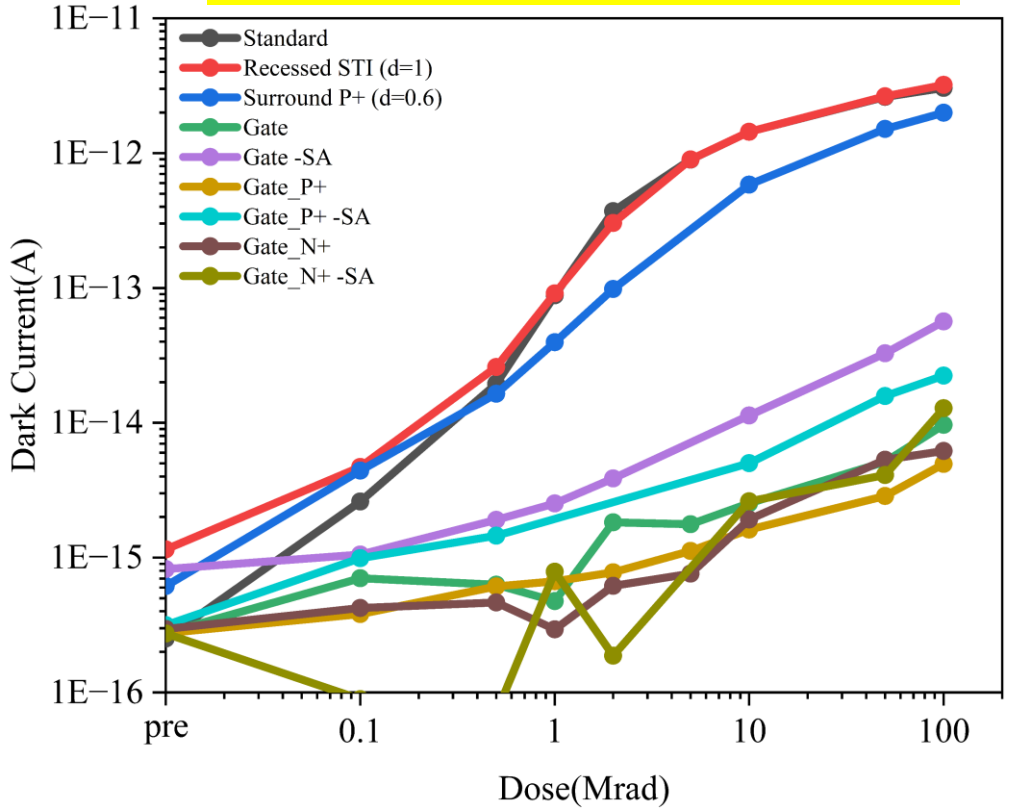
Back up

Comparison of Different Structures

Gate = 0V



At the optimum Gate voltage



Gate > Gate-SA > Surround P+ > Recessed STI = Standard