Silicon Detector R&D's in China For Major Particle Physics Experiments

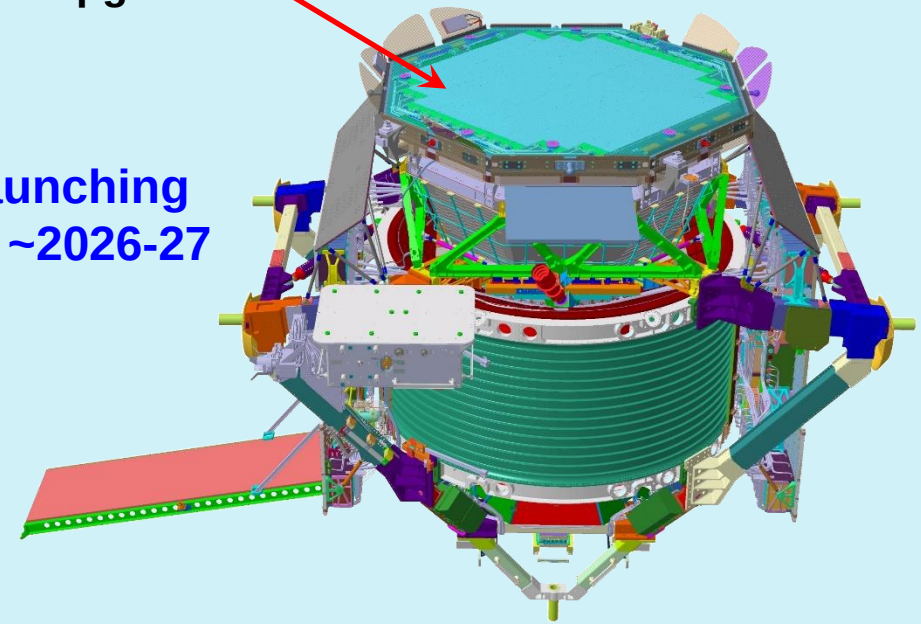
Jianchun Wang (IHEP)

HSTD14, Nov 16-21, 2025, Taipei

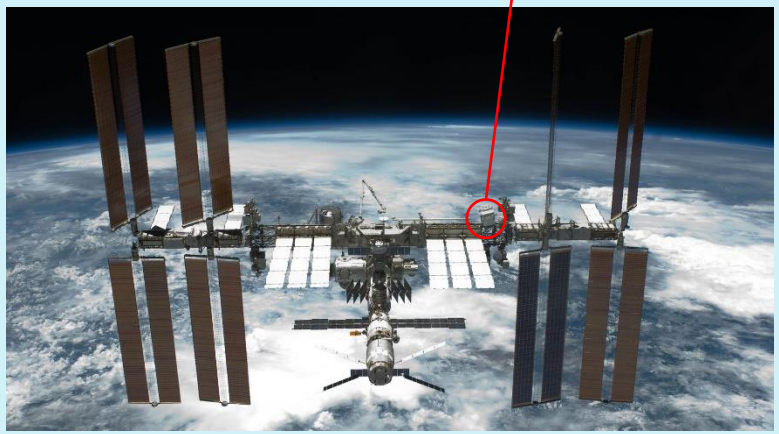
Space Station Based Experiments

L0 Tracker Upgrade

AMS-02



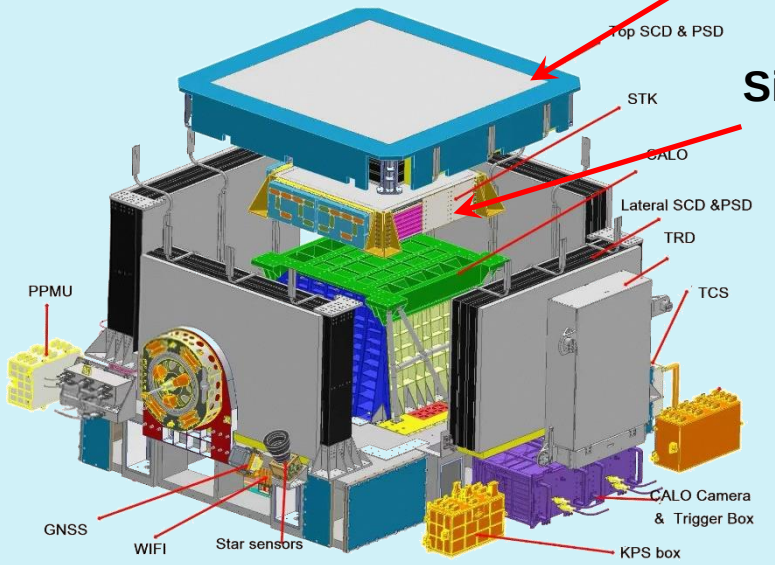
Upgrade launching is expected ~2026-27



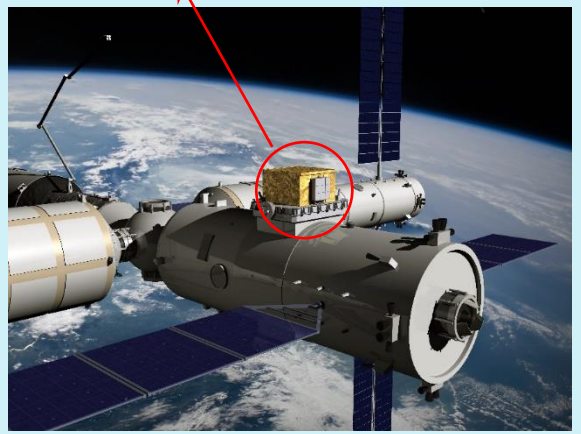
HERD

Silicon Charge Detector (SCD)

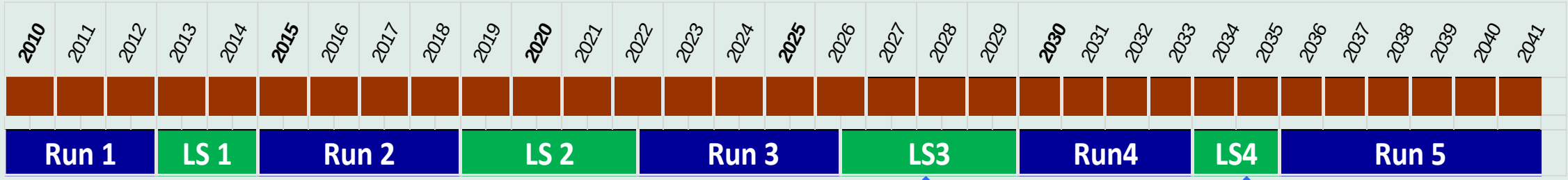
Silicon Tracker (STK)



Detector launching is expected ~2028



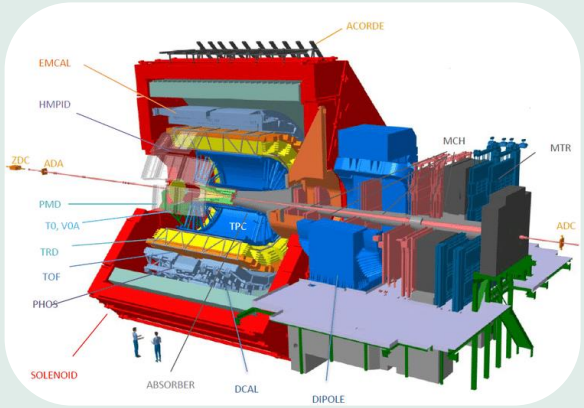
The LHC Experiments



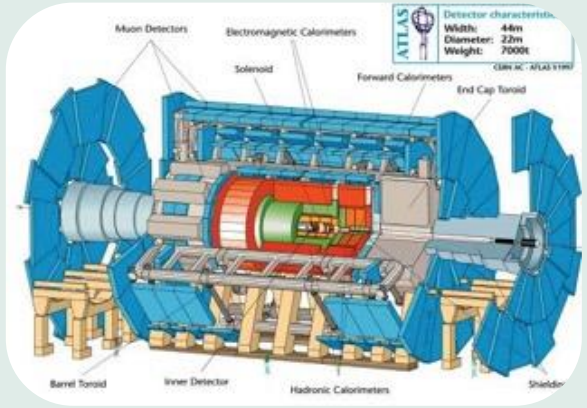
ATLAS	ITK, HGTD
CMS	HGCAL, MTD-ETL
ALICE	ITS3, FoCal

LHCb	UP
ALICE	VD, ML, TOF

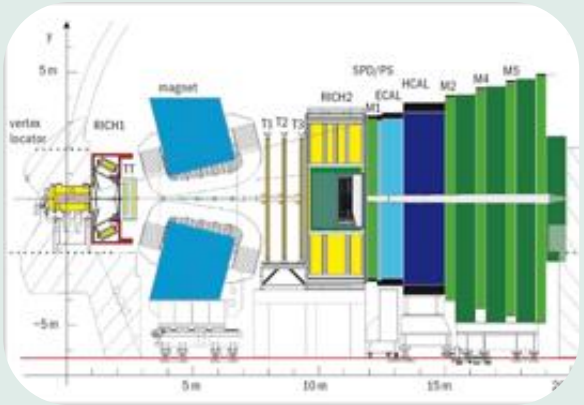
ALICE



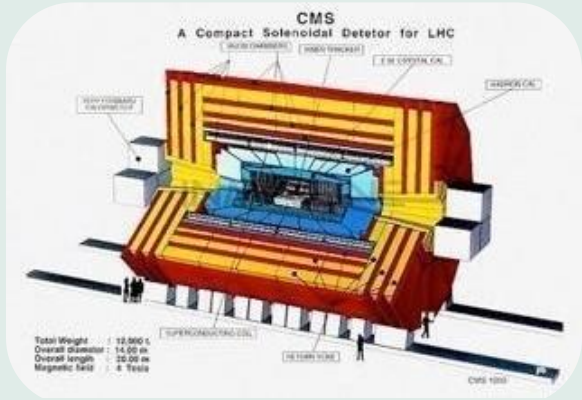
ATLAS



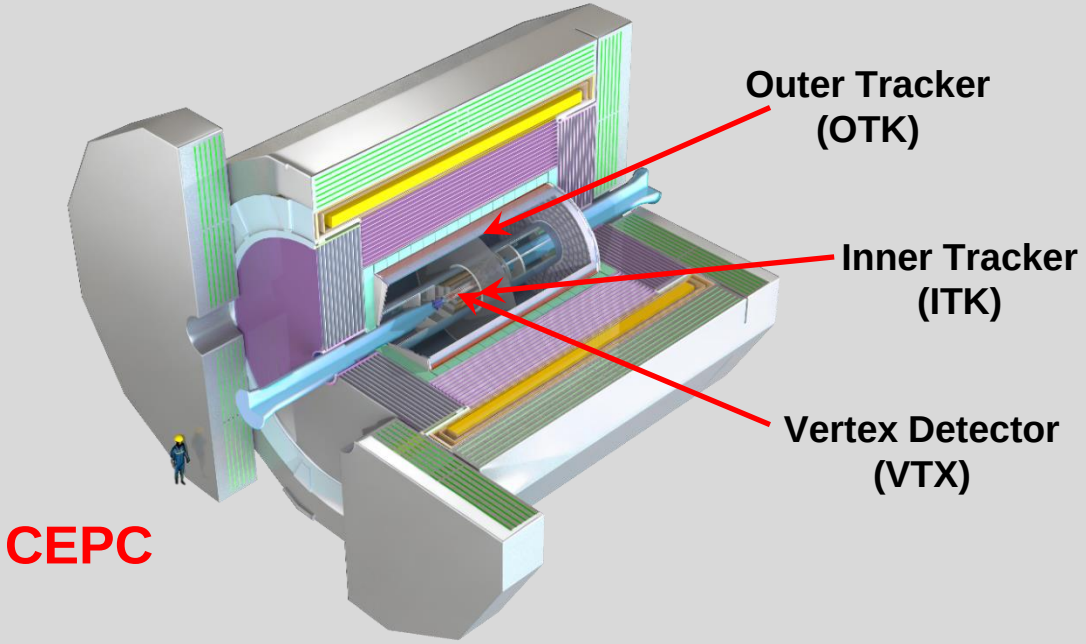
LHCb



CMS

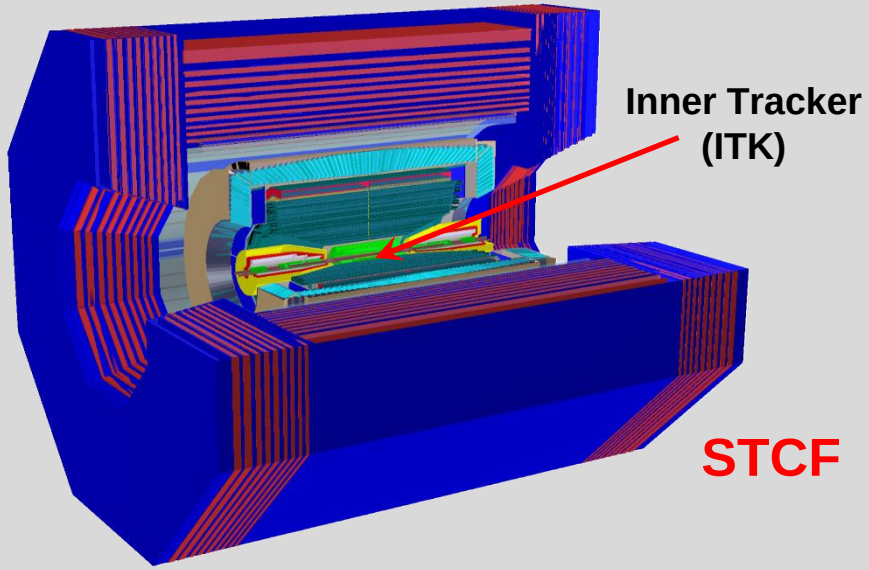


Future Electron Positron Collider Experiments



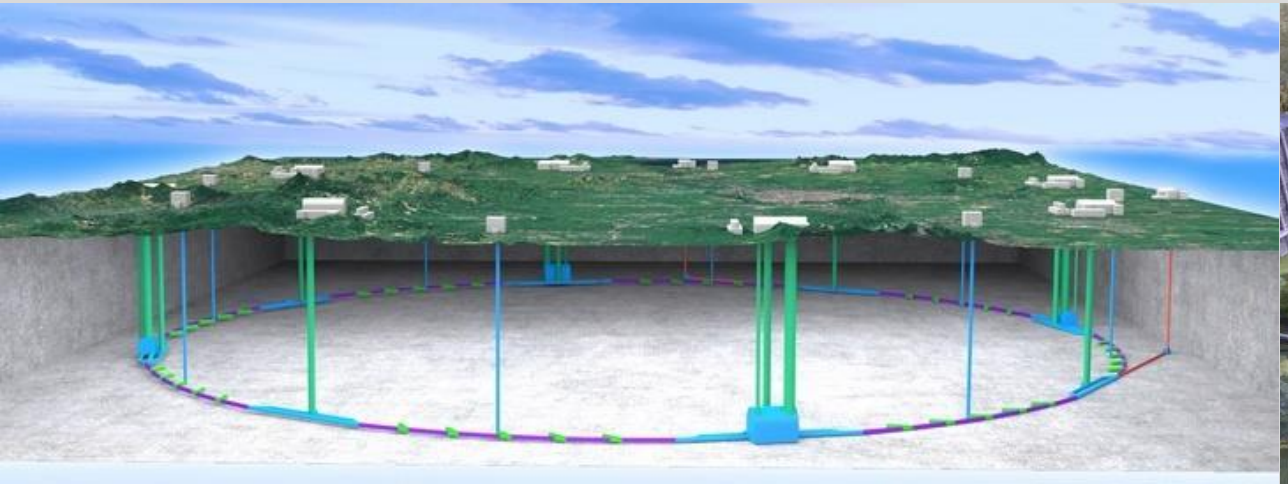
CM Energy ~ 91, 160, 240, 360 GeV

$\mathcal{L}_{max}$~1.9×10^{36} cm^{-2}s^{-1} @ 91 GeV



CM Energy ~ 2-7 GeV

$\mathcal{L}_{max}$~0.5×10^{35} cm^{-2}s^{-1} @ 4GeV

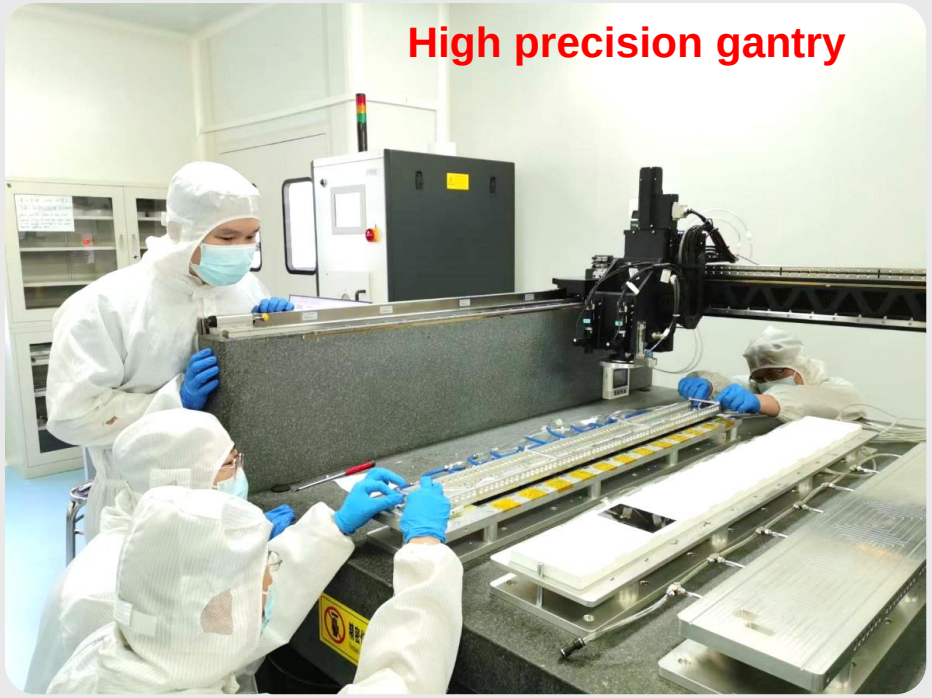


On-going Si Detector R&D Activities

Type	Detectors	Main Motivation
Strip Detector	AMS L0 Tracker	Charge measurement Z=1-28 and trajectory measurement
	HERD SCD, STK	SCD: charge measurement Z=1-28; STK: Photon conversion and trajectory measurement
	ATLAS ITK	Trajectory measurement, radiation-resilient
Monolithic Pixel Detector	ALICE ITS3,VD,ML	ITS3. VD: stitching+bent for low material and close to IP; All: trajectory measurement
	CEPC VTX, ITK	VTX: stitching+bent for low material and close to IP; All: trajectory measurement
	LHCb UP	Trajectory measurement, cost effective, radiation-resilient, high hit rate
	STCF ITK	Trajectory measurement, high hit rate
LGAD Timing Detector	ATLAS HGTD	High precision timing for pile-up separation
	CMS MTD-ETL	High precision timing for pile-up separation
	CEPC OTK	High precision timing and 1-D spatial position measurement
	ALICE TOF	High precision timing and 1-D spatial position measurement
SiDet-based Calorimeter	CMS HGCAL	High precision spatial and timing measurement, sampling calorimeter
	ALICE FoCal	High precision position sampling calorimeter

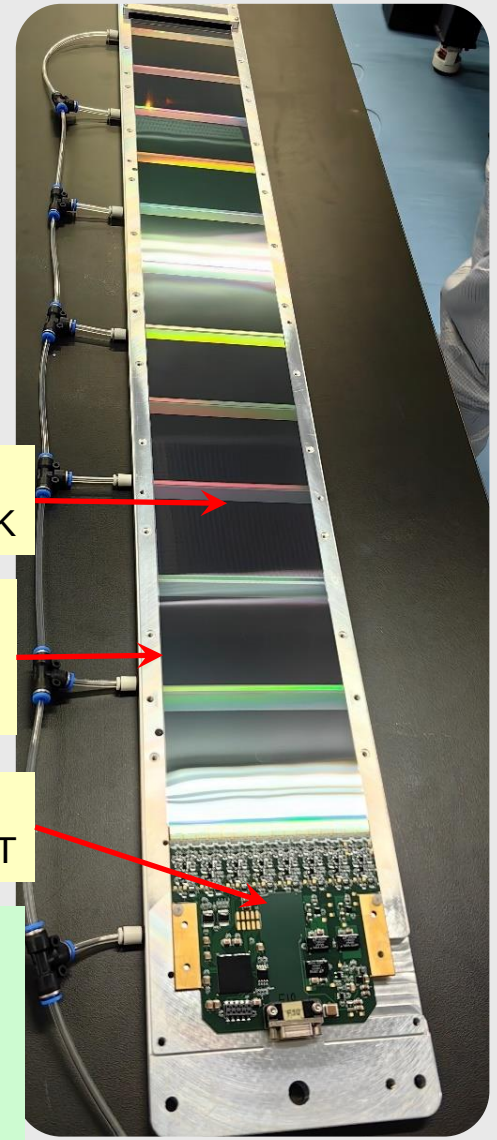
Almost all of them are detailed in the presentations and posters at this symposium

AMS L0 Tracker



Challenges

- Coupling and noise level due to long strips impose big challenges.
- Precise placement of SSDs on a ladder. Aim for a < 5 μm precision.
- Highly reliable wire-bonding (>12K wires per ladder).



SSD designed by **IHEP**+Perugia+HPK

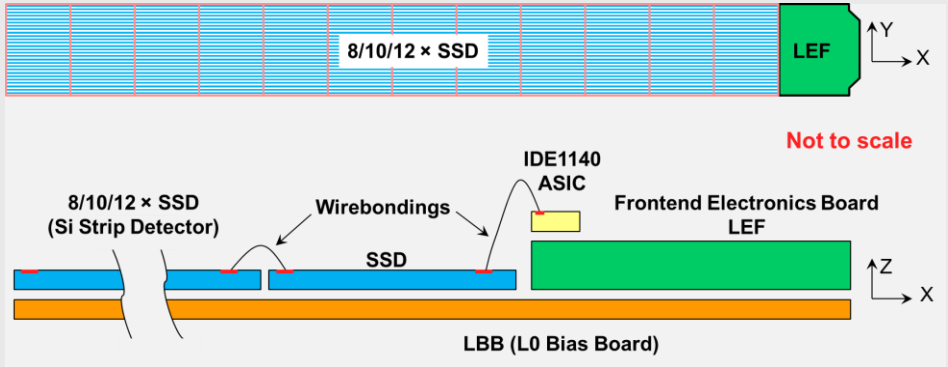
Detetector ladder produced by **IHEP+SDIAT**

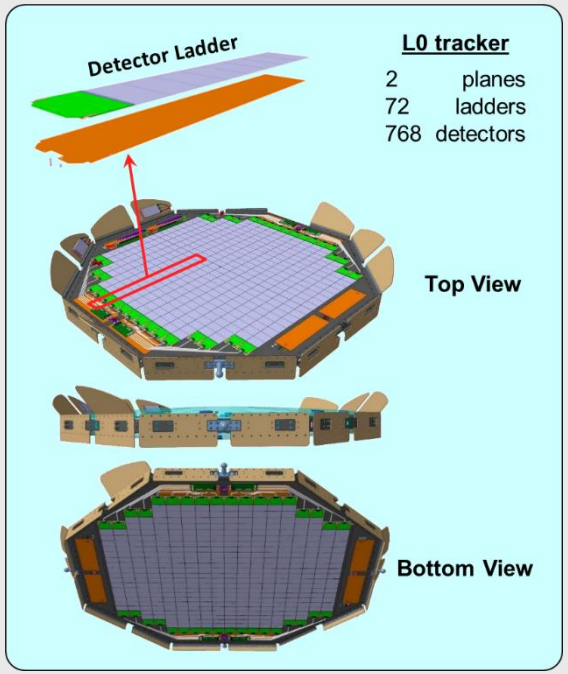
LEF produced by **IPAS+NCSIST**+MIT

HPK SSD
readout pitch 109 μm
readout / bias = 1:4
thickness 320 μm
AC + bias resistor

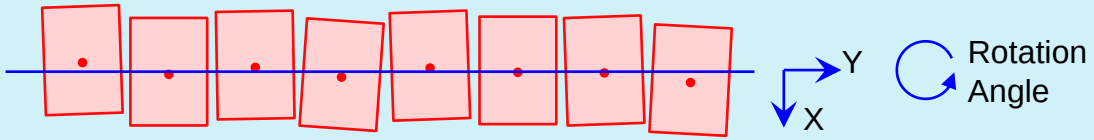
IDE1140 readout chip

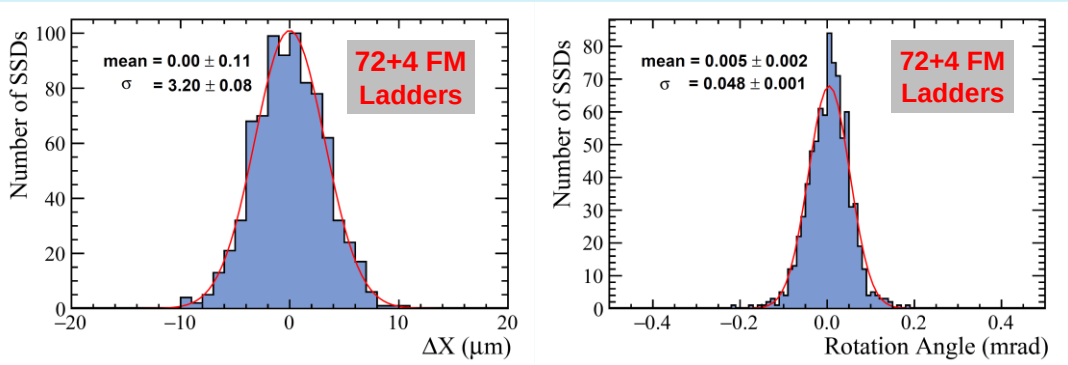
The longest SSD single unit ~ 1 m

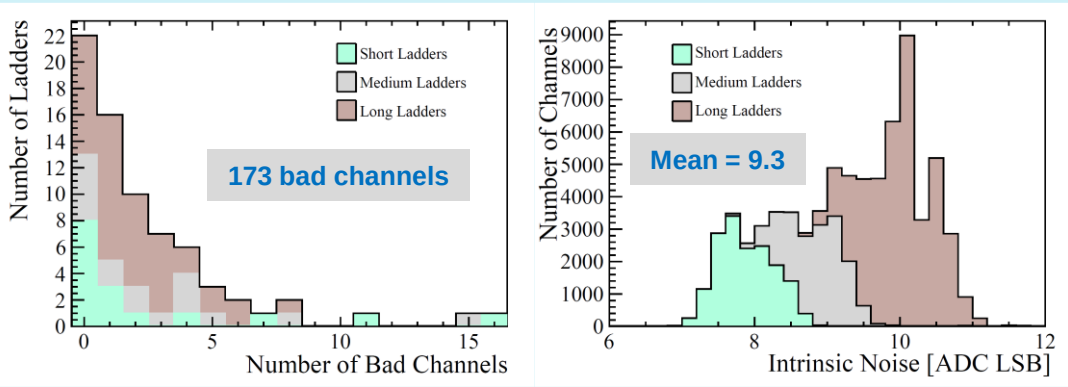




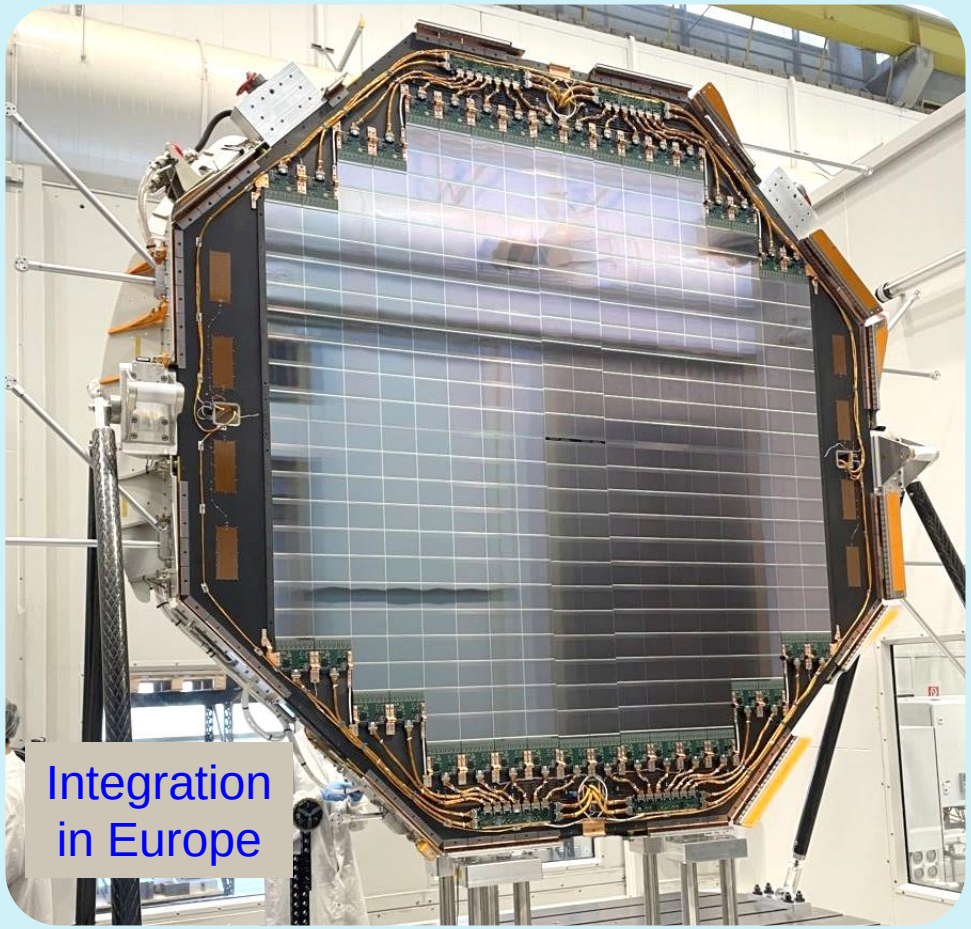
AMS L0 Tracker







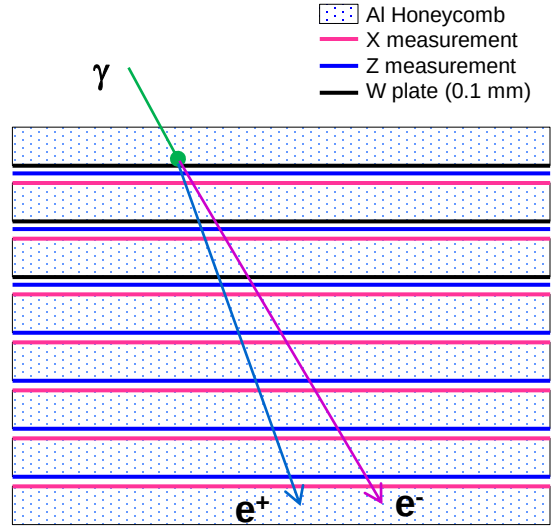
First large silicon detector with major contributions from the Chinese teams

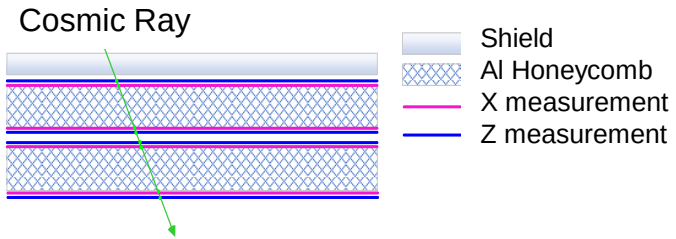


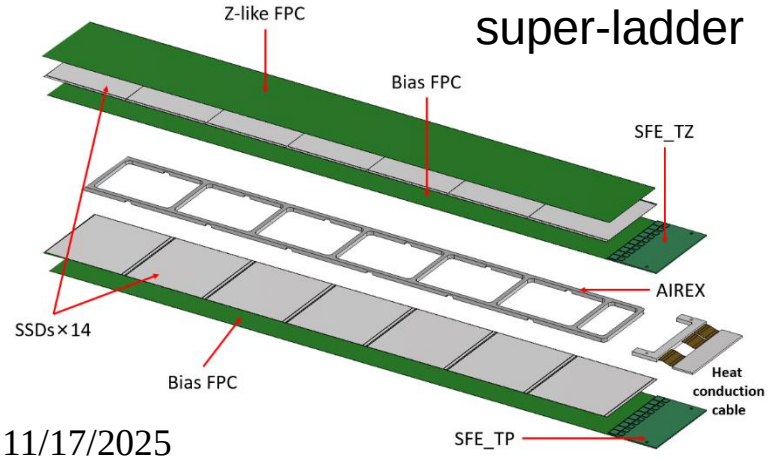
- Dark current of all ladders are < 2 μA @ 50, 80 V
- Optimized for high-Z particles; S/N for MIP ~ 6-7
- Bad channel rate ~ 0.23%
- Non-perfect production contributes to measurement σ_x=3.4 μm, before applying correction

HERD Silicon Detectors: SCD and STK

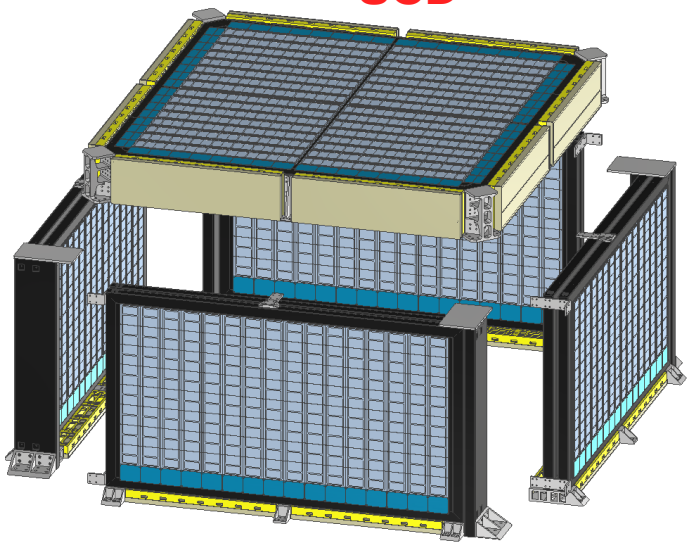
- HERD (High Energy cosmic-Radiation Detection) is to be installed on the Space Station by ~2028. The detector system has SCD, STK, +3 others
- SCD: **5-side, 8-layer** charge measurement Z=1~28, total area 38.8 m^2
- STK: **14-layer** detecting trajectories of $\gamma \rightarrow e^+e^-$ conversion in 3 W plates, angular resolution ≤ 0.1° @ 10 GeV, total active area 8.3 m^2
- HPK SSDs: 150 μm pitch, 320 μm thick, DC with bias resistor
- Front end readout chips: IDE1140, VATA450.3





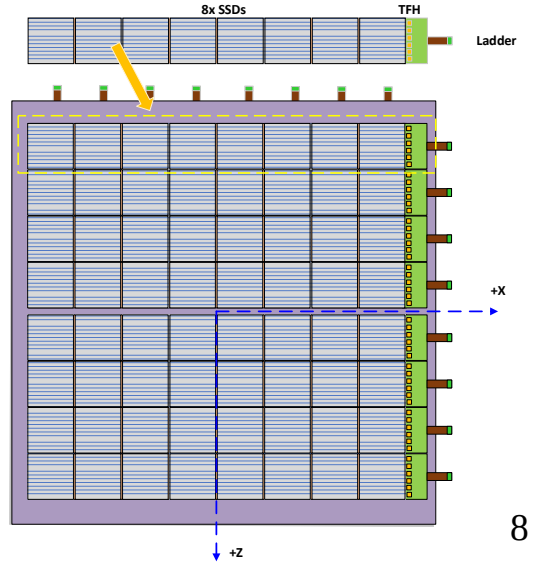


SCD



STK

ladder and layer



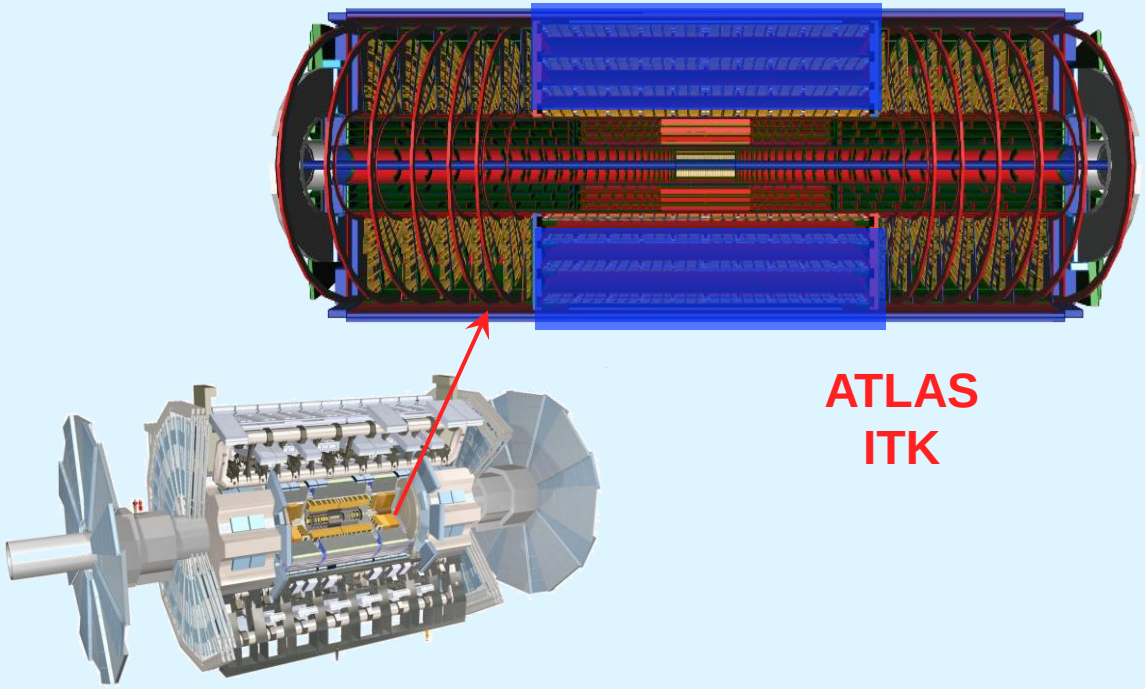
Participating institutes:

IHEP, PMO, Perugia

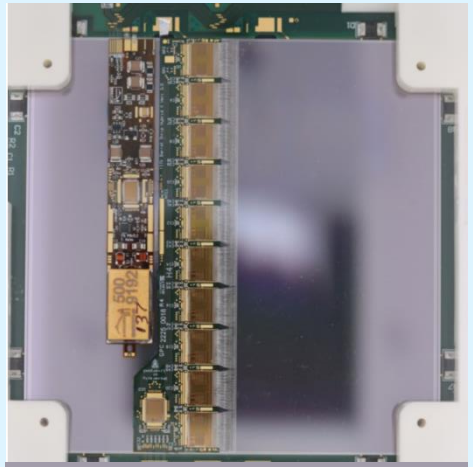
ATLAS Inner Tracker ITK

- Strip strip detector, total area 165 m^2, 18000 strip modules, to be installed during LS3
- HPK p-type sensor, 320 μm thick; 130nm CMOS readout chips: ABC, HCC, AMAS
- The module production task shared by ~20 countries. Chinese groups will produce ~10% of the strip barrel modules (1000 modules)
- The groups will perform sensor characterization (1/8 sites), and quality assurance (1/5 sites) using its 80 MeV proton beam at CSNS of IHEP
- Contribution to the silicon tracker integration at RAL and CERN

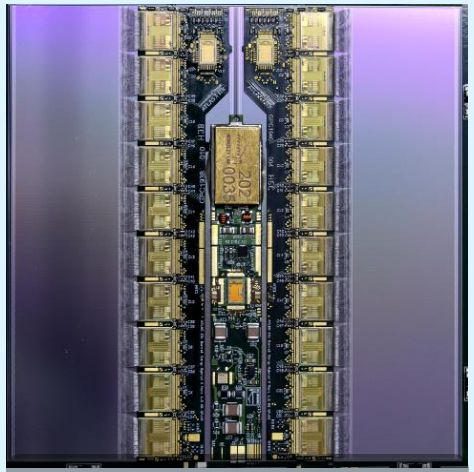
Chinese institutes:
IHEP, THU, SYSU, SJTU, SDU



ATLAS ITK

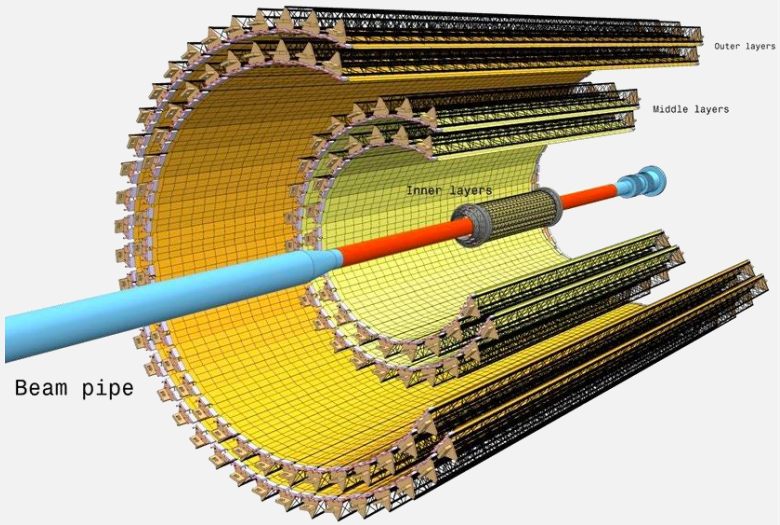


IHEP REPSERIES Module (×15)



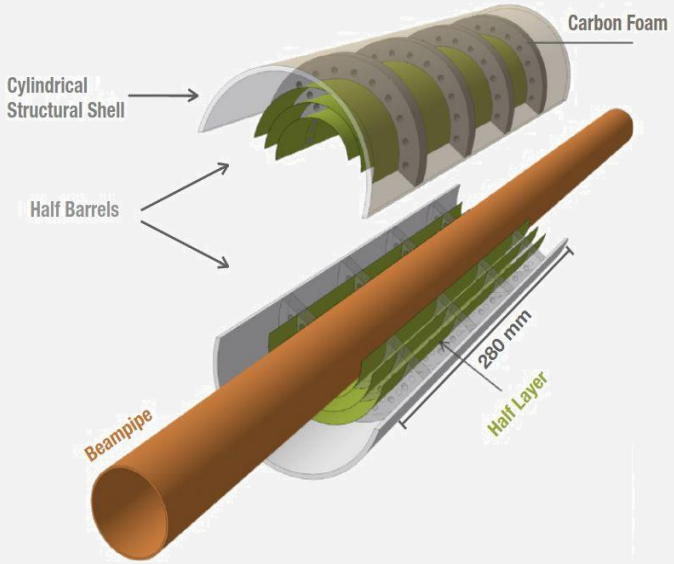
Short-strip Module

ALICE MAPS Tracking Detectors



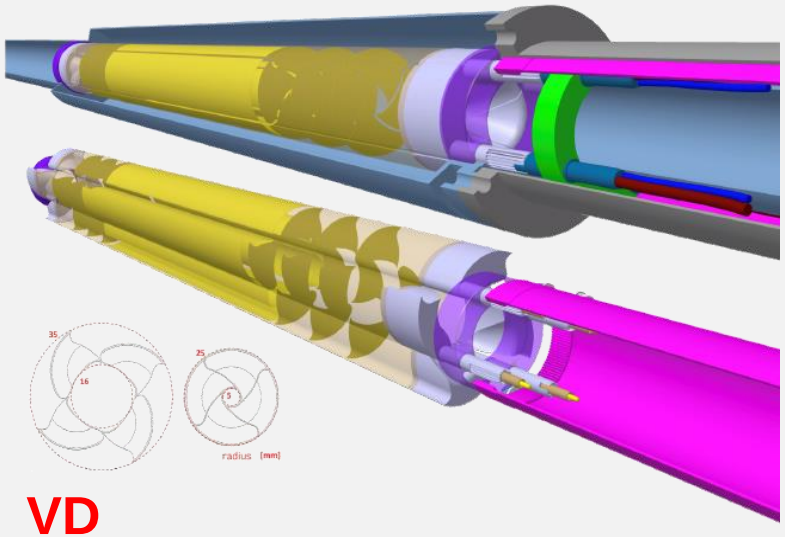
ITS2

- Installed during **LS2**
- 3 inner, 2 middle, 2 outer layers
- MAPS chip: ALPIDE
- TJ 180 nm CMOS process
- Pixel size: 29×27 μm^2
- Low power < 40 mW / cm^2
- IP resolution: 5 μm



ITS3 (replace the 3 inner layers)

- To be installed during **LS3**
- TPSCo 65 nm process
- Wafer-scale MOSAIX sensors
- Cylindrical geometry
- Closer to IP: R= (24→19) mm
- Reduced material: (0.36→0.09)% X_0
- Spatial resolution ~ 5 μm
- Time resolution ~ O(1000) ns
- Radiation hard ~ 3×10^{12} n_{eq} cm^{-2}



VD

- To be installed during **LS4**
- Retractable and close to beam
- Low material mass ~0.1% X_0
- Spatial resolution ~ 2.5 μm
- Time resolution ~100 ns
- Radiation hard ~ 1×10^{16} n_{eq} cm^{-2}

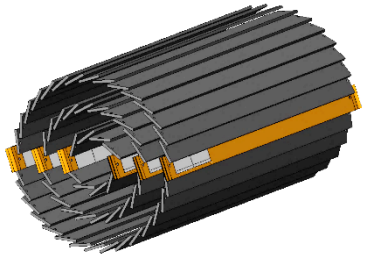
ML

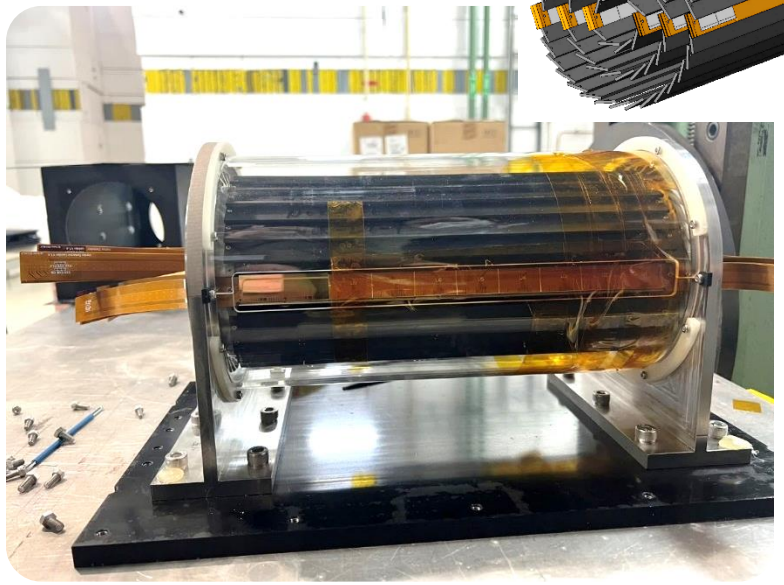
- Low material mass ~1% X_0
- Spatial resolution ~ 10 μm
- Time resolution ~100 ns
- Radiation hard ~ 6×10^{13} n_{eq} cm^{-2}

Chinese institutes: **CCNU, CIAE, USTC, …**

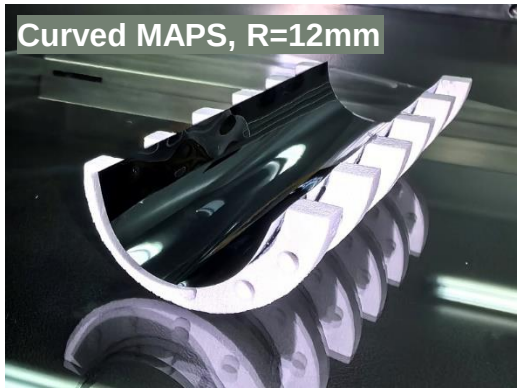
CEPC Vertex Detector

Alternative design: ladder-based

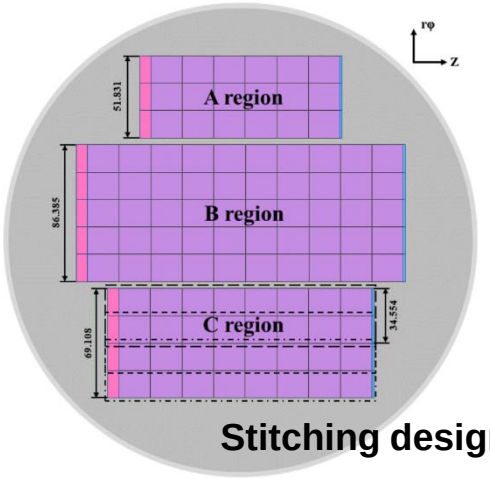




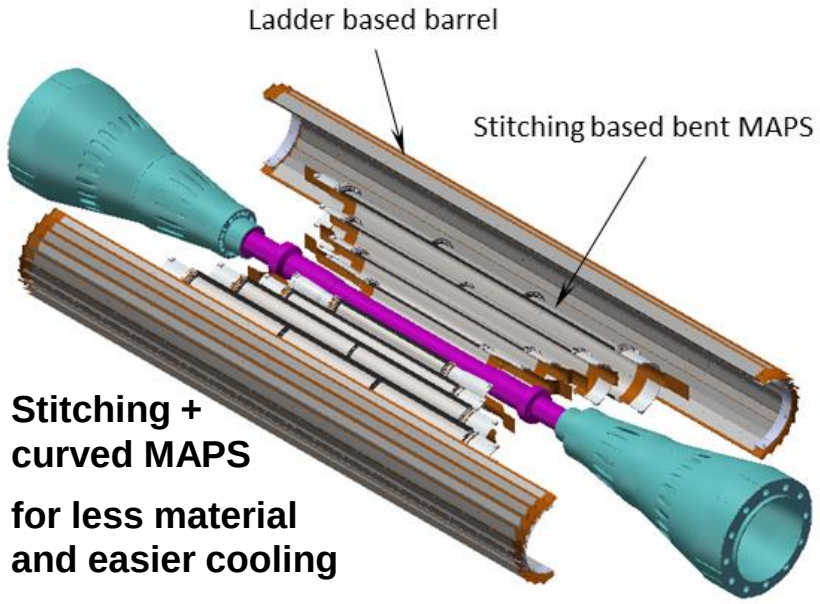
A TaichuPix-based prototype detector



Goal: σ(IP) ~ 5 μm for high P

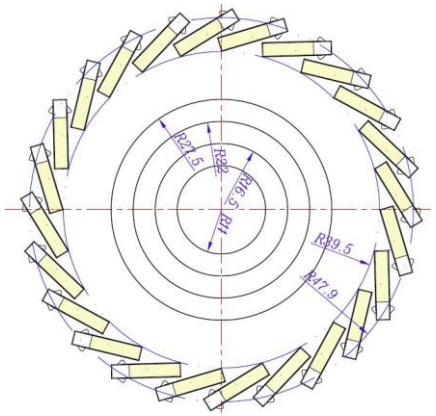


Stitching design



Stitching + curved MAPS

for less material and easier cooling



Outer: double-layer ladder
Material ~ 0.3% X_0 / layer

Inner layer: single bent MAPS
Material ~ 0.06% X_0 / layer

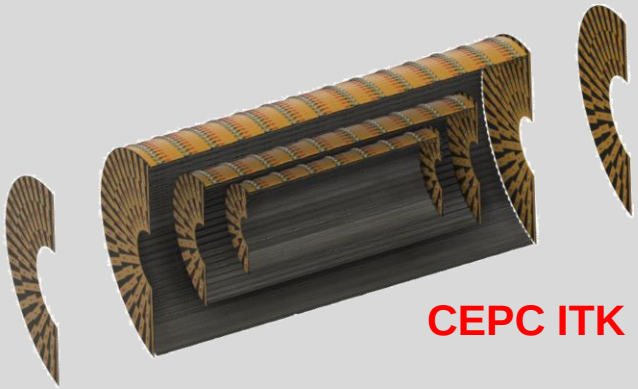
CEPC Inner Tracker ITK

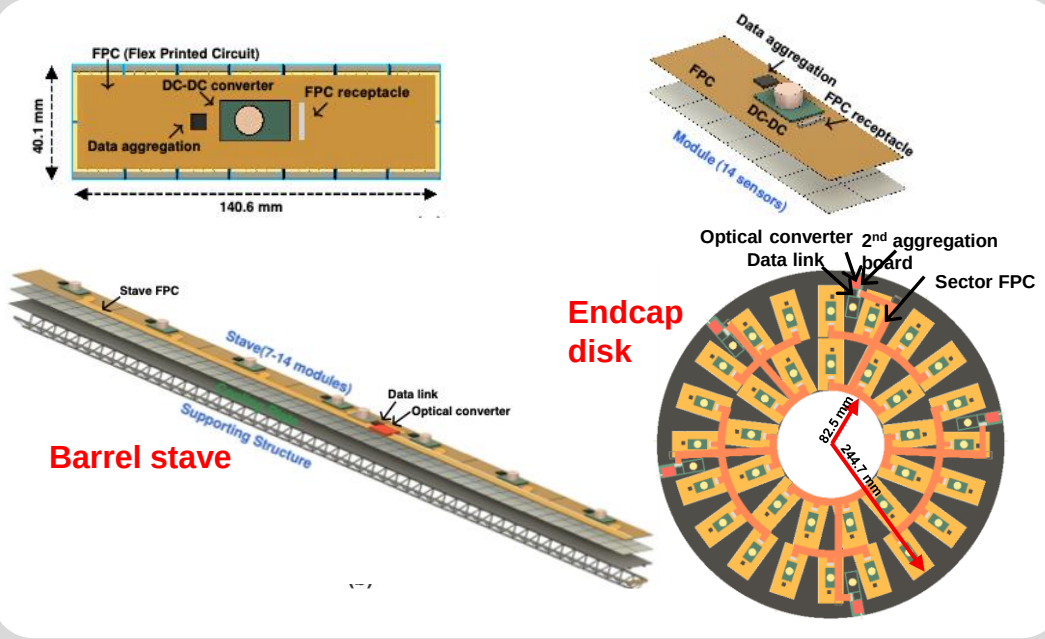
- HV-CMOS pixel detector for CEPC inner tracker ITK, area ~15-20 m^2.
- Explore 55 nm and other processes
- Detector design based on typical chip size

Goal

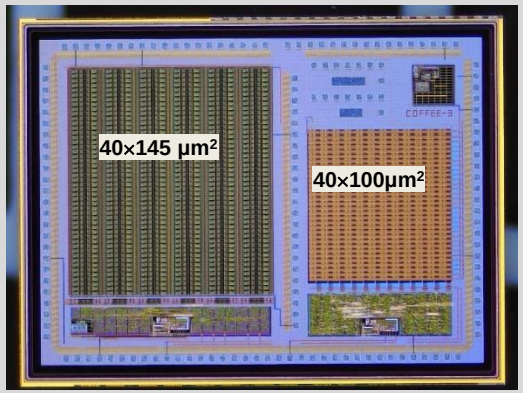
- Cost effective
- Spatial resol. < 10 μm
- Timing 3-5 ns
- Power < 200 mW/cm^2

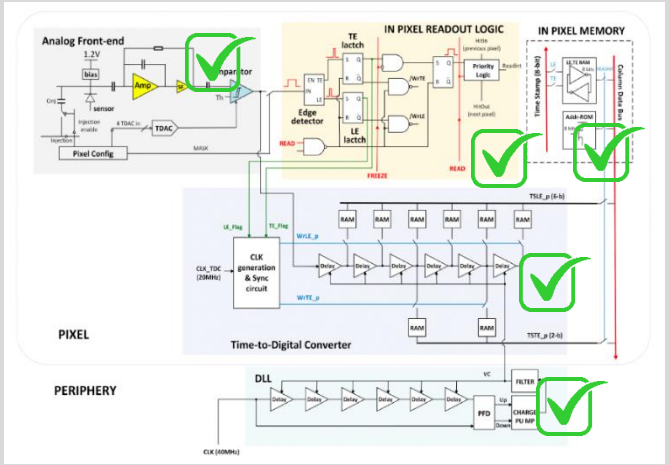
Process node: 55 nm
Chip size: 2 cm × 2 cm
Sensor thickness: 150 μm
Pixel array: 512 × 128
Pixel size: 34×150 $μm^2$
Spatial resolution: 8 / 40 μm
Time resolution: 3-5 ns
Power consumption: 200 mW/cm^2

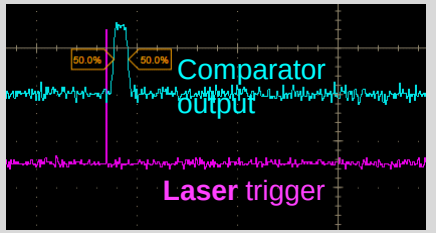


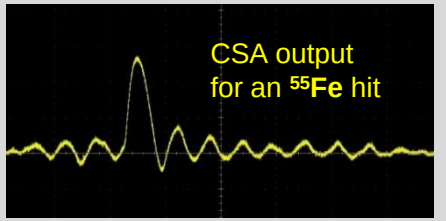


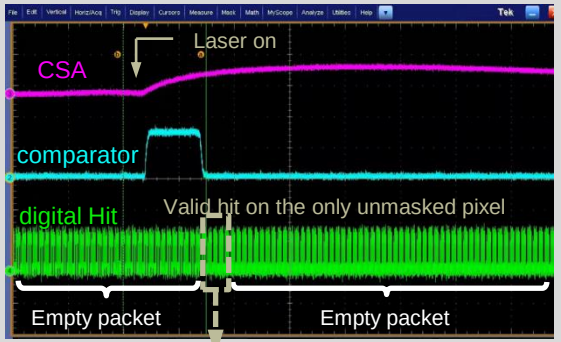
COFFEE 3











4 bit	4 bit	8 bit	8 bit	6 bit	2 bit	7 bit	3 bit
header	CHIP_TS	LE_coarse	TE_coarse	LE_fine	TE_fine	Addr_Row	Add_Col
0 1 1 0	0 1 0 1	0 0 0 1 0 1 1 0	0 1 1 0 1 0 1 1	1 1 0 0 0 0	0 0	0 0 0 0 0 0 1	0 0 0

A valid transmission packet corresponding to a hit

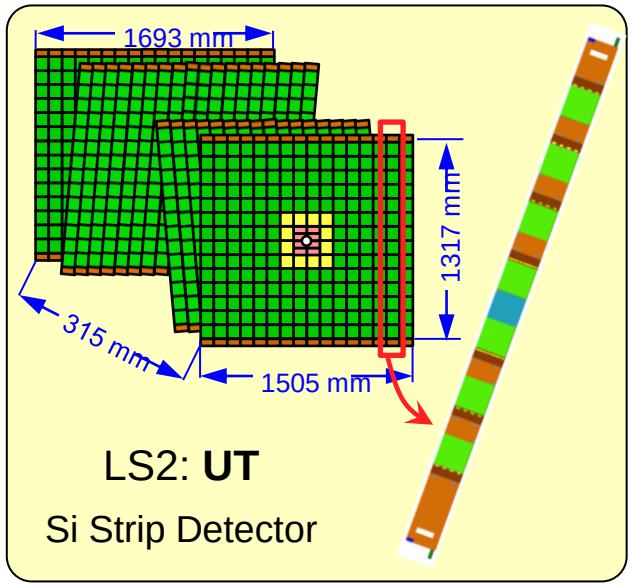
Correct row & column address

LHCb UP Detector

- A HV-CMOS pixel detector, to be installed during LS4
- The active area ~7 m^2
- The team has a big overlap with the CEPC ITK team

- Spatial resolution ~ 10 μm
- Time resolution 3-5 ns
- Power < 200 mW/cm^2
- Rad-hard: 3×10^{15} n_{eq}/cm^2

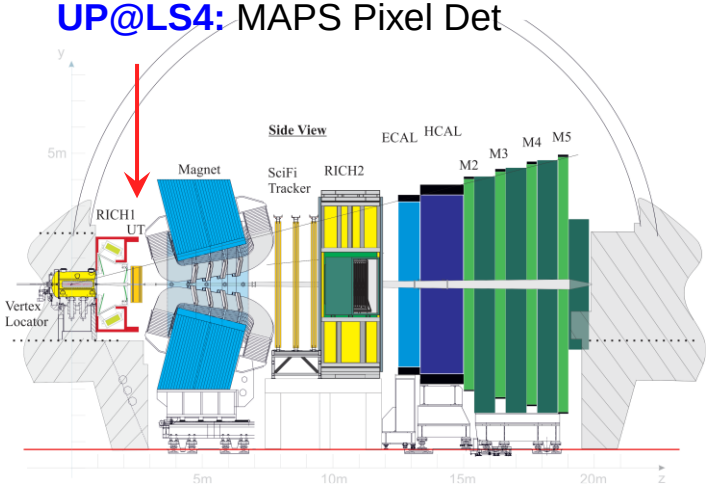
Chinese institutes
IHEP, CCNU, HNU, HTU, LZU, NPU, UCAS, …



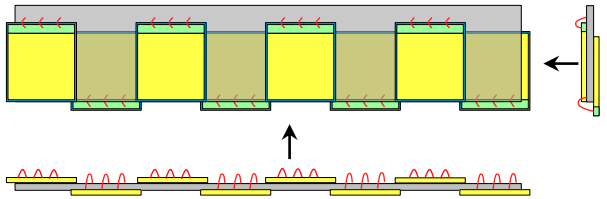
LS2: **UT**
Si Strip Detector

UT@LS2: Si Strip Detector

UP@LS4: MAPS Pixel Det



Module

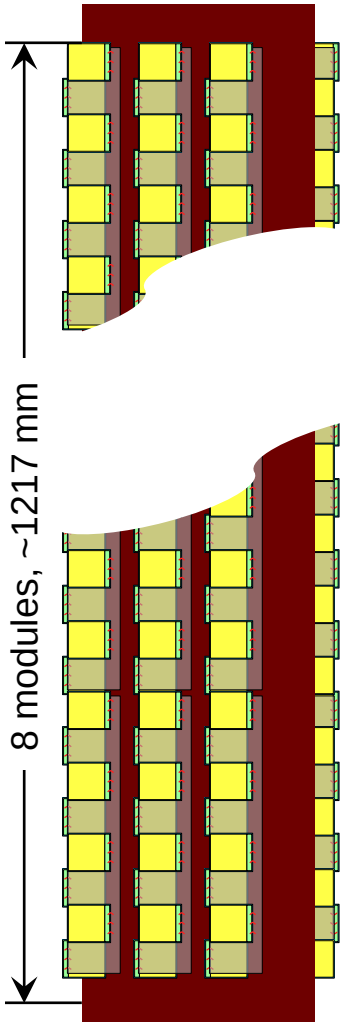


Prototype module

Prototype stave support

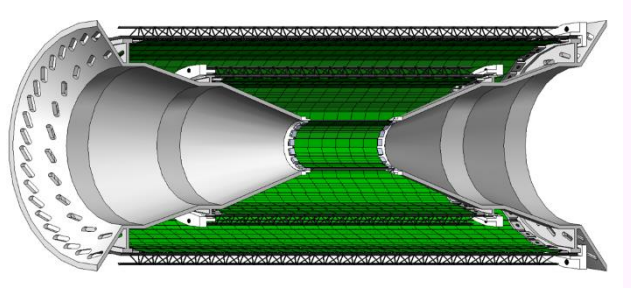
CFRP faces + CF honeycomb,
Ti cooling tubes

Stave



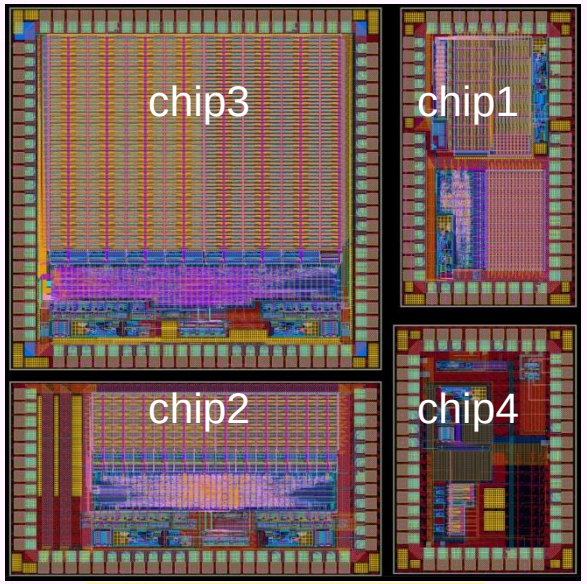
STCF Inner Tracker ITK

- Requirements: tracking efficiency >99% @ p_T>0.3 GeV; >90% @ p_T >0.1 GeV
- Three-layer MAPS detectors (R = 36, 98, 160 mm), total area: 1.3 m^2
- Chinese institutes: **USTC, SDU, CCNU, NPU**



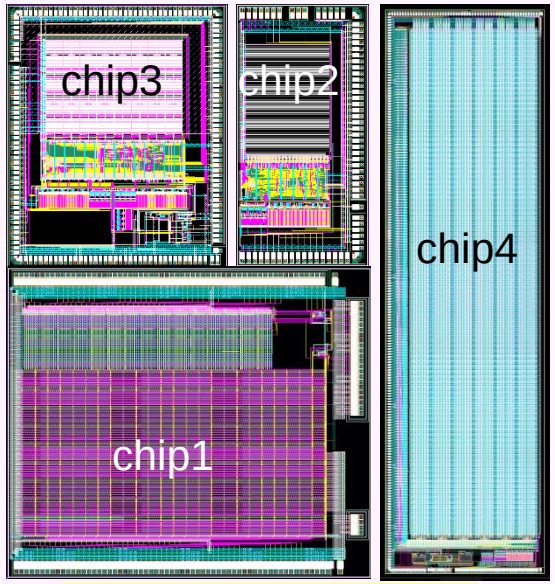
CharTPix chip prototyping

180 nm process, HR epitaxial wafter



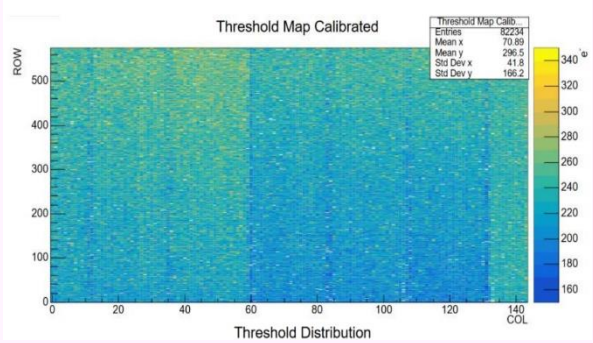
Total area: 5×5 mm^2,
Pixel size: 180×30 μm^2
Other variants

130 nm process, HR wafter



Total area: 24×12 mm^2,
Pixel size: 30×30 μm^2
Other variants

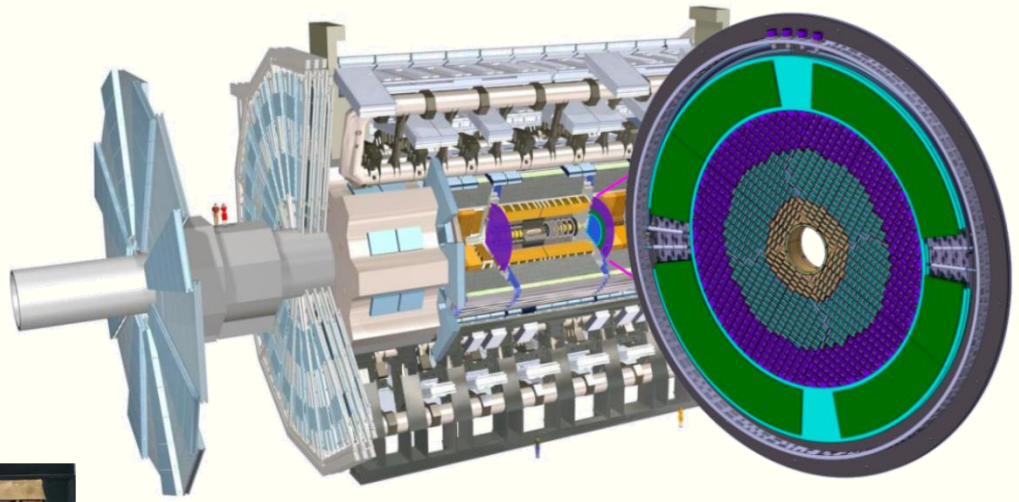
Requirements:
- Power consumption ≤ 50 mW/cm^2
- Material per layer ≤ 0.35% X_0
- Spatial resolution ≤ 30 μm
- Time resolution ≤ 20 ns
- Hit rate capability ≥ 1MHz/cm^2
- Rad hardness: 1Mrad/y, $10^{11}n_{eq}$/cm^2/y
- ToT measurement

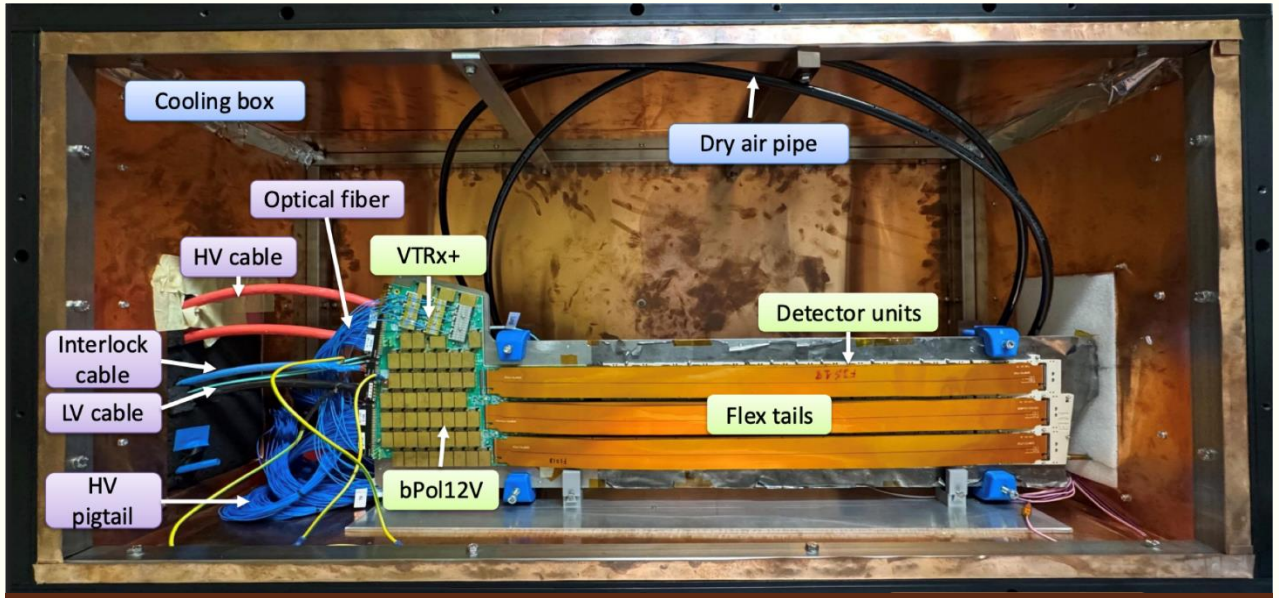


Threshold: 225
Mismatch: 26.5 e
Thermal Noise： 6.6 e
@SUB=-4 V

ATLAS HGTD

- An LGAD-based High Granularity Timing Detector (HGTD), to be installed during LS3
- China team is making key contributions
  - 100% LGAD sensors (IHEP-IME, USTC-IME)
  - 44% detector assemblies
  - 100% FE electronics boards, ~33% flex tails
  - 50% testing of the FE readout ASIC ALTIROC
  - >16% high-voltage electronic systems





First demonstrator of a large scale system (55 modules)

Time resolution 30-50 ps / track

Detection area ~ 6.4 m^2

Pixel pad size: 1.3×1.3 mm^2

Rad-hard: 2.5×10^{15} n_{eq} cm^{-2}, 2 MGy

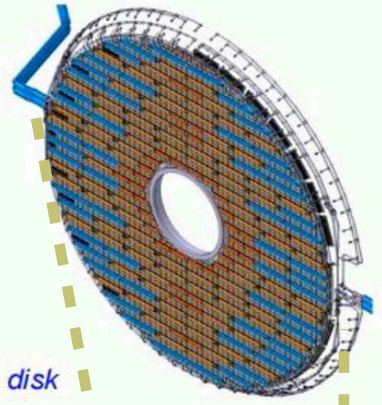
Chinese institutes

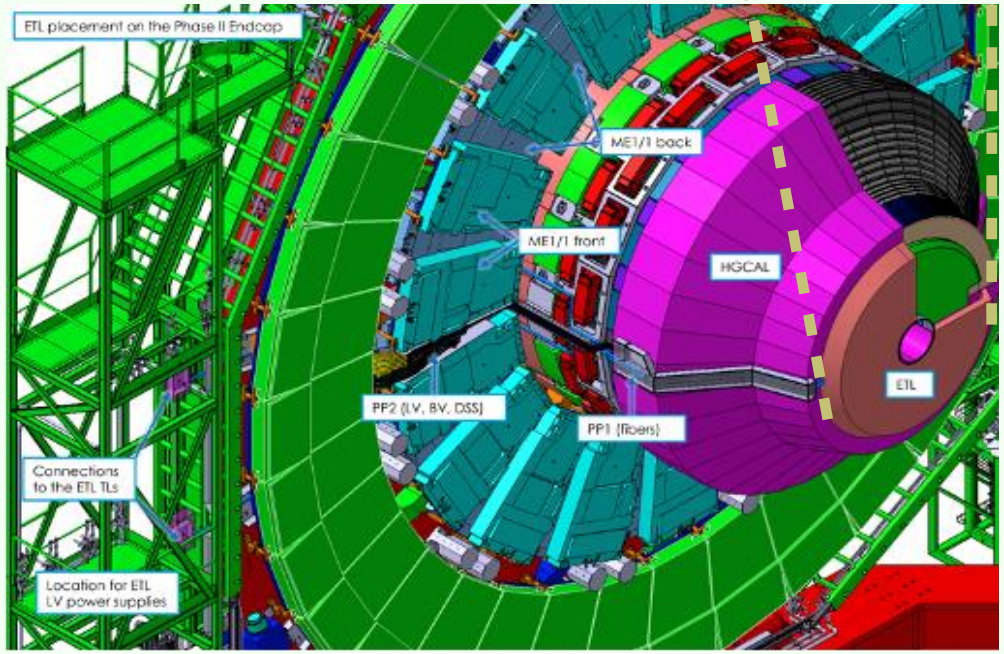
IHEP, USTC, SDU, NJU, …

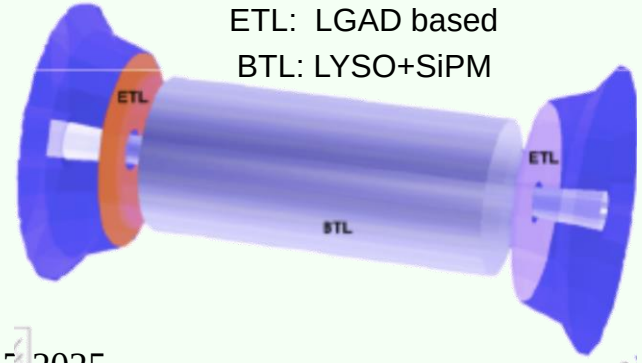
CMS MTD-ETL Detector

- CMS MIP Timing Detector (MTD) will be installed during LS3. It consists of LGAD-based ETL and LYSO+SiPM based BTL
- LGAD producers: HPK and FBK-LFoundry
- FE readout chip: ETROC TSMC 65 nm technology
- Countries involved: USA, Italy, South Korea, Spain, China, Finland et al; total ~ 20 institutes
- Involvement of the Chinese groups in ETL:
  1) LGAD characterization during prototyping phase and quality control during production phase
  2) MUX64 chip procurement and test
  3) ETL DAQ software development

Time resolution 50 ps / hit
Detection area ~ 12 m^2
Sensor pad array: 16×16
Pixel pad size: 1.3×1.3 mm^2
Rad-hard: 2.4×10^{15} n_{eq} cm^{-2}







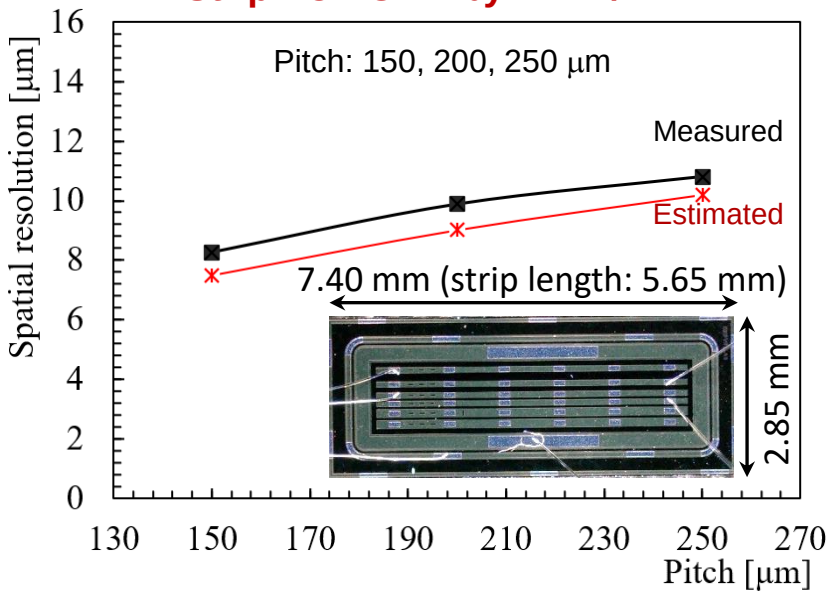
Chinese institutes:

USTC, SCNU, SDU

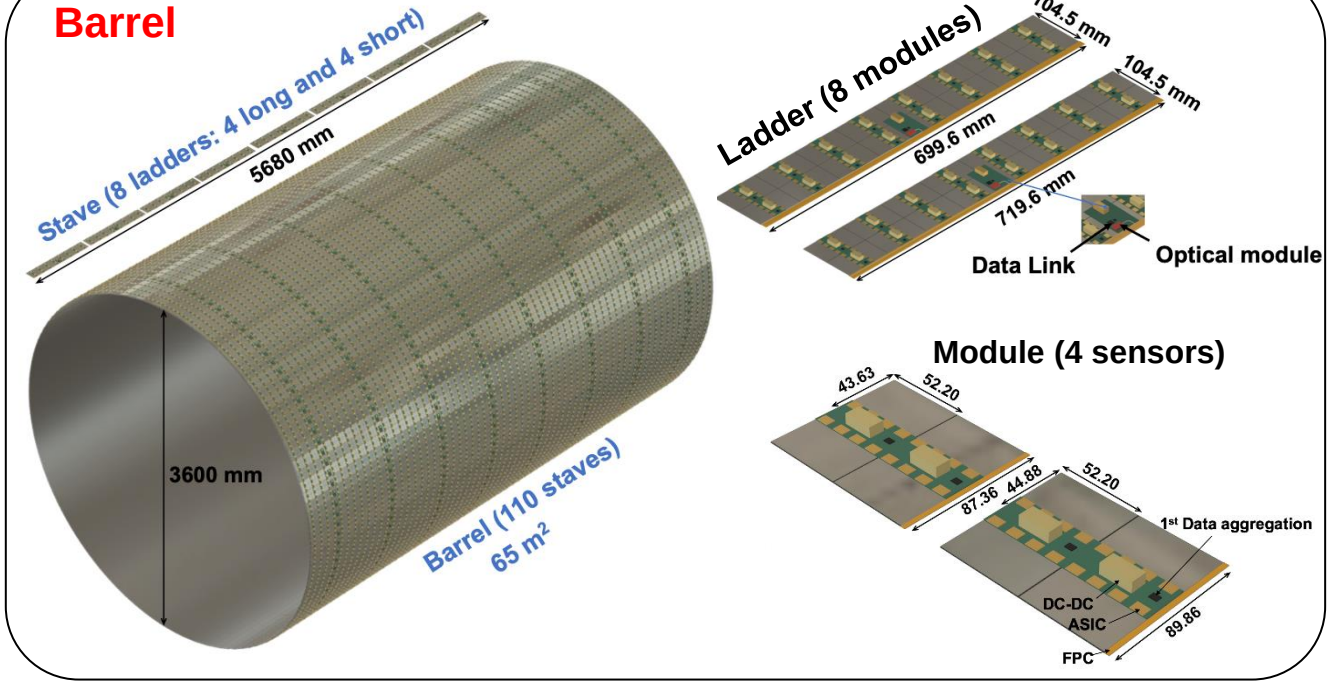
CEPC Outer Silicon Tracker OTK

- The outer tracker ~ 85 m^2, Z precision not crucial ⇒ Cost-effective SSD
- A supplemental PID at low energy ⇒ LGAD TOF
- An **AC-LGAD** Time Tracker for both: σ_t ~50 ps, $\sigma_{R\Phi}$ ~10 μm
- Optimizing sensor: length = 1,2,4 cm, pitch = 100, 200, 500 μm.
- Front end readout ASIC – LATRIC_v0 has been produced

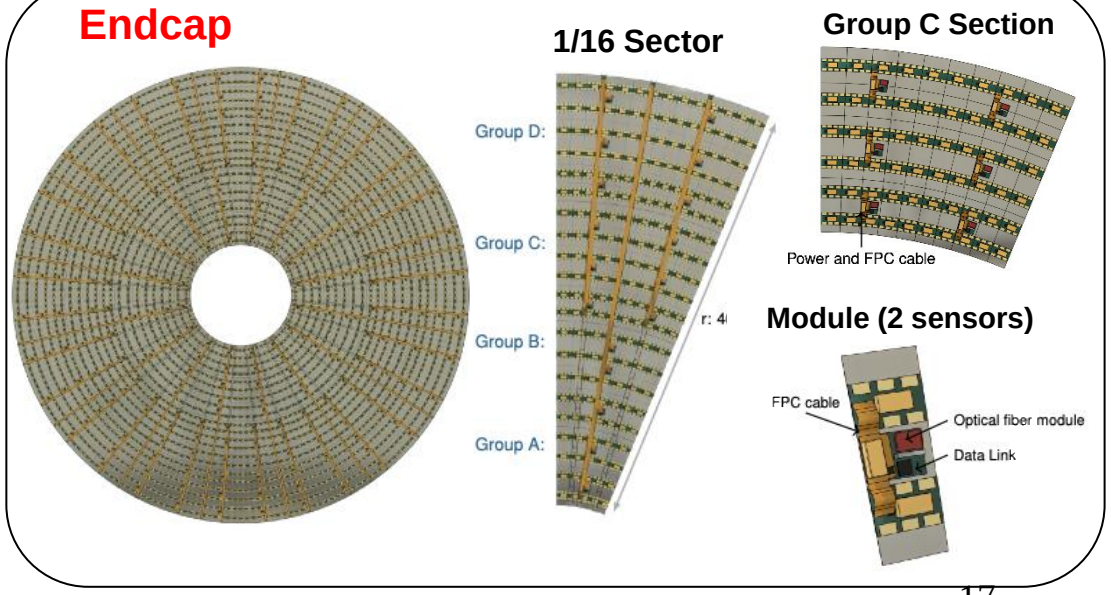
Strip AC-LGAD by IHEP / IME



Barrel

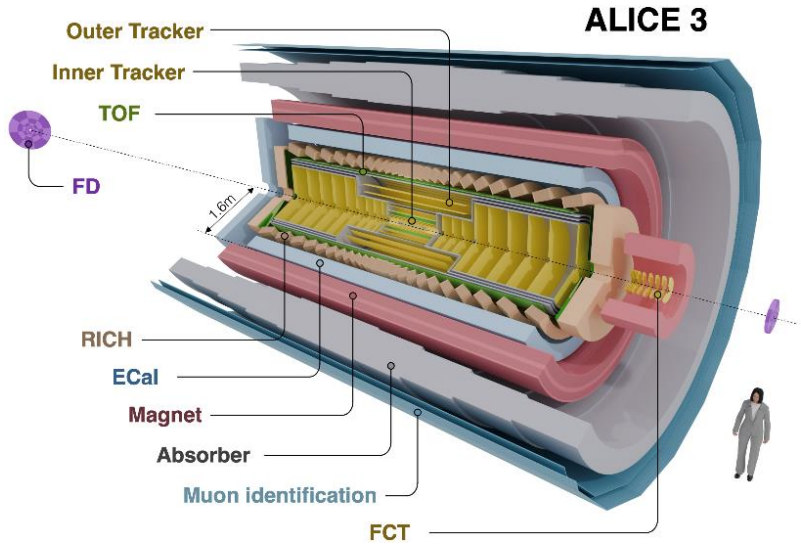


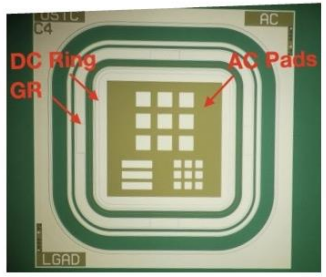
Endcap



ALICE AC-LGAD TOF

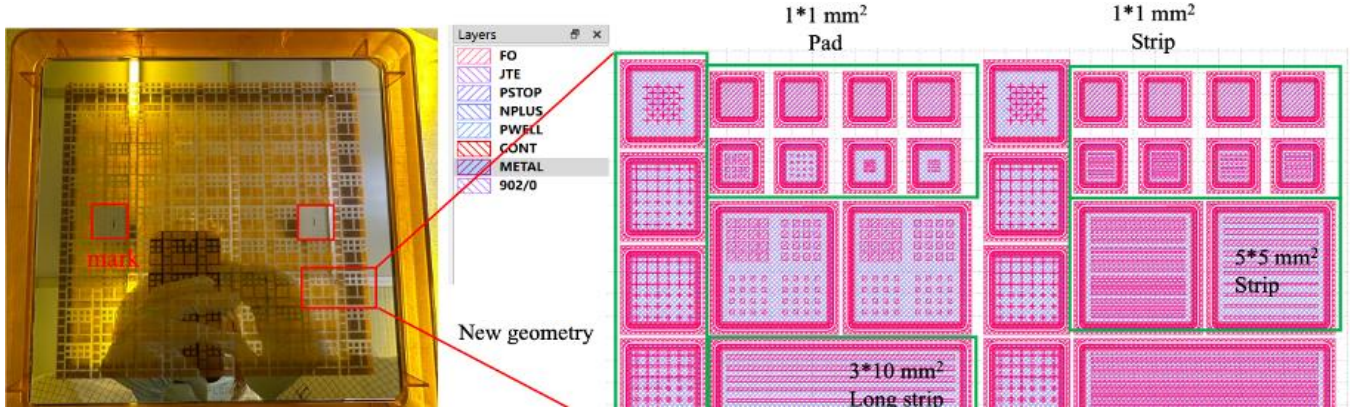
- Exploring an AC-LGAD based TOF as an alternative to the CMOS-LGAD solution, to be installed during LS4
- Total area ~ 40 m^2, including inner, outer and forward TOF
- Key specification: time resolution **20 ps**
- Preliminary achievement: time resolution 35 ps @ room temperature, 26 ps @ -30 ^oC, spatial resolution ~ 5-9 um





Type	Small pad	Large pad	Strip
electrode pitch (μm)	75×75	150×150	75
electrode size (μm)	50×50	100×100	50×200
column × row	3×3	3×3	3

v1 is fabricated and characterized, paper in preparation

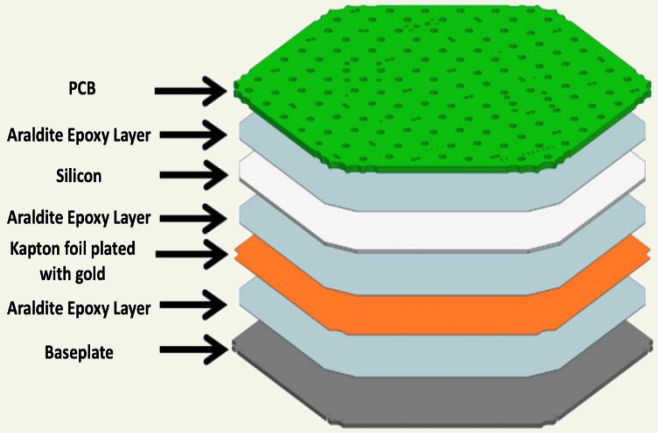


v2 is fabricated and being characterized

Proposed by: **USTC**

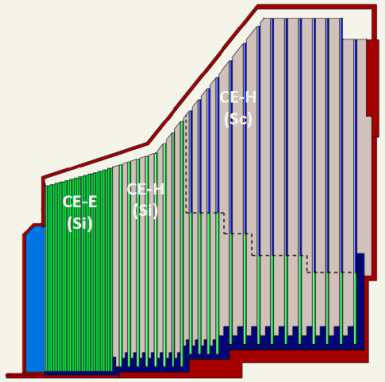
CMS HGCal and ALICE FoCal-E

> 50 institutes including
IHEP, FDU, NNU, THU, ZJU



- First 5D calorimeter: spatial, energy, time; rad-hard ~ 10^{16} n_{eq}/cm^2
- HPK SiPAD sensor, 8" wafer, 1 or 0.5 cm^2 cell size, 300/200/120 μm thick
- HGCROC chip readout by LLR, Omega group
- Total 26000 modules, 620 m^2 Si sensor. Module production is shared among 6 module assembly centers (MACs). **IHEP** and **NTU** each hosts 1 MAC.
- Responsible for production of 90% **CuW** baseplates

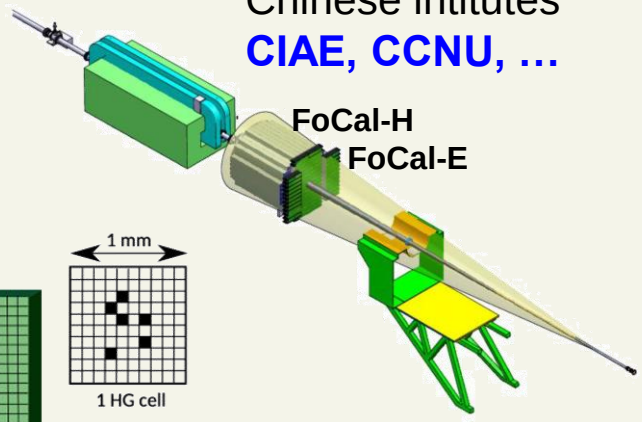
CMS HGCAL

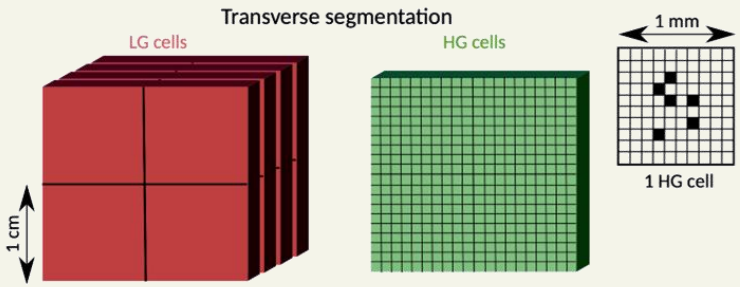


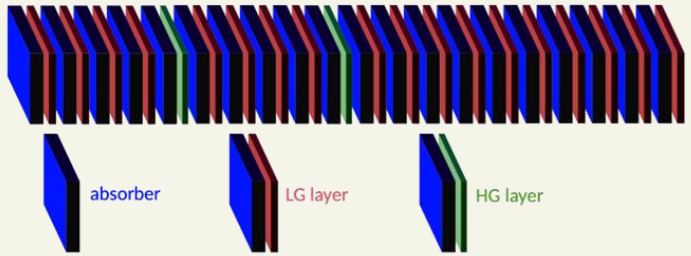

HGCAL module assembling at IHEP MAC

ALICE FoCal-E

Chinese intitutes
CIAE, CCNU, …







20 W layers (3.5 mm)
+18 pad layers(1×1cm^2)
+**2 pixel layers** using **ALPIDE**(29×27μm^2)

Closing Remarks

- In the recent years, research of silicon detector technology develop fast in China.
- The Chinese groups are very active in silicon detector efforts for major international experiments: AMS, HERD, ATLAS, CMS, LHCb, ALICE, CEPC, STCF, …
- Enhanced collaborations are welcome. Hopefully Chinese groups could bring in more ideas, technologies, opportunities and other resources to this fascinating domain.

Thank you for your attention!

Disclaim: There are many other interesting silicon detector R&D activities by the Chinese groups. The selection is simply based on my personal taste and preference. My sincere apology to those that could not be covered.

Acknowledgement: Thanks to my colleagues who provided very useful materials in a short notice. Special thanks to Xiaomei Li, Yiming Li, Zhijun Liang, Nan Lu, Wenxi Peng, Xin Shi, Zebo Tang, Lailin Xu, Huaqiao Zhang