progress

yao

prog

- update daq
- Server worker OS too old, update?

V792 QDC

- V792AC

Table 3.2 – Model V792/V792 N main technical specifications

Packaging	6U-high, 1U-wide VME unit (versions AA and NA require the V430 backplane)			
Power requirements	Refer to Table 3.1			
Inputs	32/16 channels, 50 Ω impedance, negative polarity, DC coupling			
Input range	0 ÷ 400 pC[4]			
Resolution	12 bit			
Gain	100 fC/count			
Max. tolerated positive voltage input	>25 mV; See also § 2.1.4			
Reflections	<5% with 2 ns fall time input signals			
Input offset	±2 mV			
Noise[5]	**Settings**		**Measured value**	
	Gate width (ns)	*Iped (count)*	*Average (count)*	*σ (count)*
	100	180	107.58	0.50
	500	180	326.44	0.54
	1000	180	597.32	0.56
	2000	180	1139.92	0.61
RMS Noise	0.7 counts typical			
Interchannel gain uniformity	± 4%			
Interchannel Isolation	> 60 dB			
Fast clear time	600 ns			
Gate timing	The GATE signal must precede the analog input by >15 ns			
Conversion time	Mod. V792: 5.7 µs / 32 Ch.; Mod. V792 N: 2.8 µs / 16 Ch.			
Dead time	Mod. V792: 6.9 µs / 32 Ch.; Mod. V792 N: 4 µs / 16 Ch.			
Zero suppression	Thresholds values programmable in: 16 ADC counts step over the entire FSR 2 ADC counts steps over 1/8 of FSR			
Integral non linearity	± 0.1% of Full Scale Range[6]			
GATE/COM input	NIM signal, high impedance temporal window for current integration .			
Control inputs	Mod. V792: active-high, differential ECL signals Mod. V792N: NIM signals **GATE:** temporal window for peak detection (ECL/NIM). **RST:** resets PEAK sections, MEB status and control registers. **VETO:** inhibits the conversion of the peaks. **FCLR:** FAST CLEAR of PEAK sections and conversion.			
Control outputs	Mod. V792: active-high, differential ECL signals Mod. V792N: NIM signals **BUSY:** indicates the presence of data **DRDY** (Mod.V792 only)**:** board full, resetting, converting or in MEMORY TEST mode			
VME interface	A24/A32, Geographical addressing, Multicast commands D16/D32, BLT32/MBLT64, CBLT32/CBLT64			
MultiEvent Buffer	32 events			

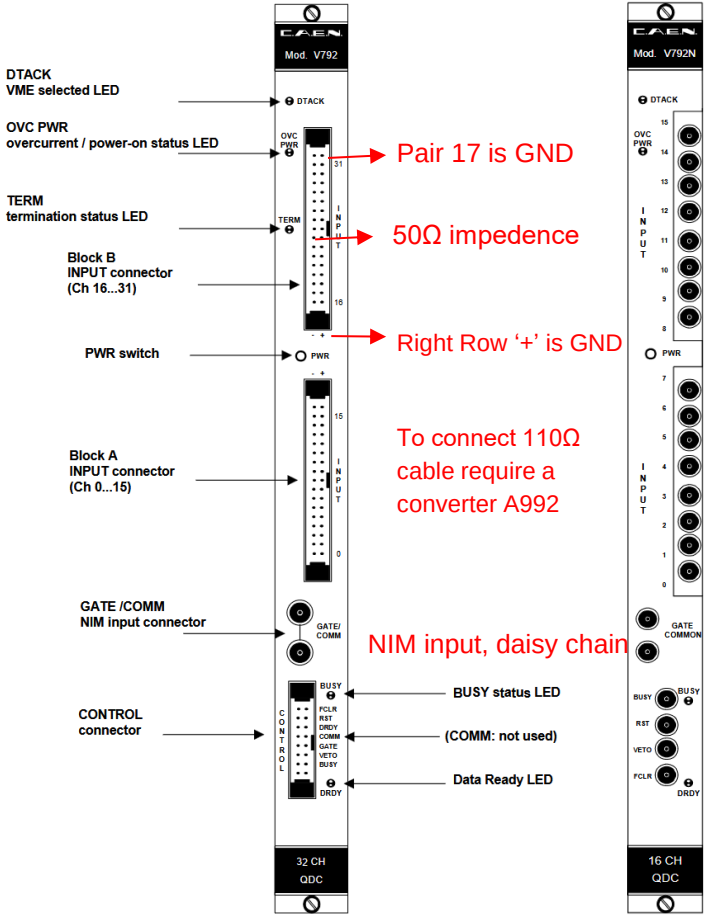
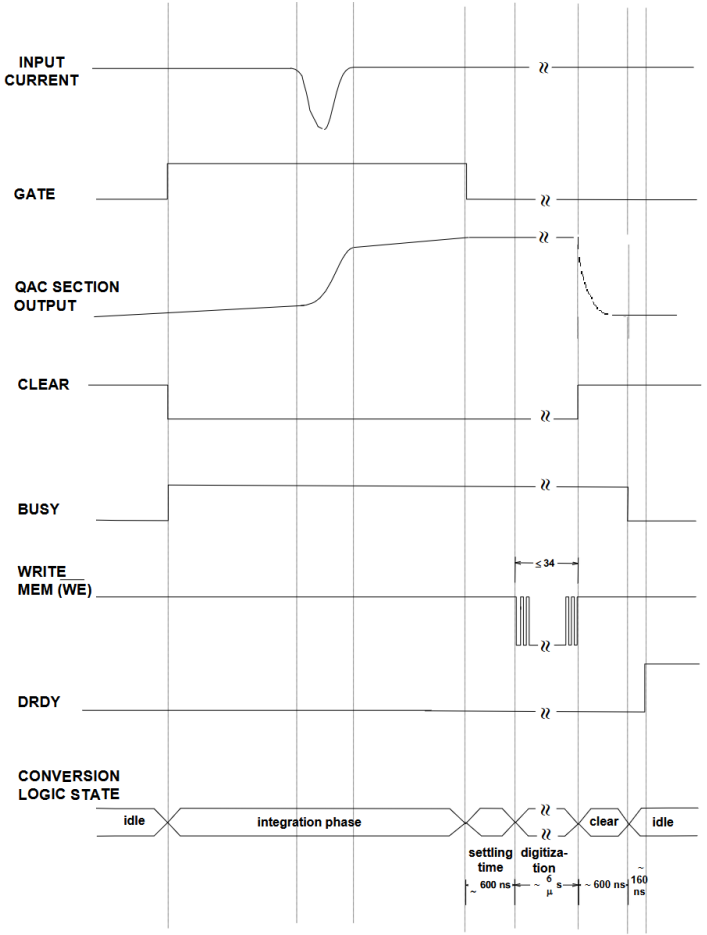


Fig. 3.1: Model V792 front panel

V792 QDC

- The GATE signal must precede the analog input by >15 ns
- CLAER signal input is used to **abort** the conversion
- Maximum GATE width is 400pC / Ip
- CLEAR signal input must be happen between GATE ~ GATE+7us (programmable)



1mA x 1ns = 1pC

Pedestal

- Pedestal is programmable
- Default setting is 180

	Settings		Measured value	
	Gate width (ns)	*Iped (count)*	*Average (count)*	*σ (count)*
Noise[5]	100	180	107.58	0.50
	500	180	326.44	0.54
	1000	180	597.32	0.56
	2000	180	1139.92	0.61

2.1.1.1. Piggy back board version 2 and later (Mod. V792 and V792 N)

The input current to current converter (negative inputs) is shown in Fig. 2.3; it uses a differential amplifier and a bipolar transistor; a minimum bias current is required to flow through the transistor T1 in order to:

- Allow T1 to operate in the linear region even for small input signals
- Tolerate small positive input currents still ensuring linear response

This bias current is provided by the I_0 (≈ 500 μA) and I_1 (VME programmable, see § 4.34) current generators (see figure below).

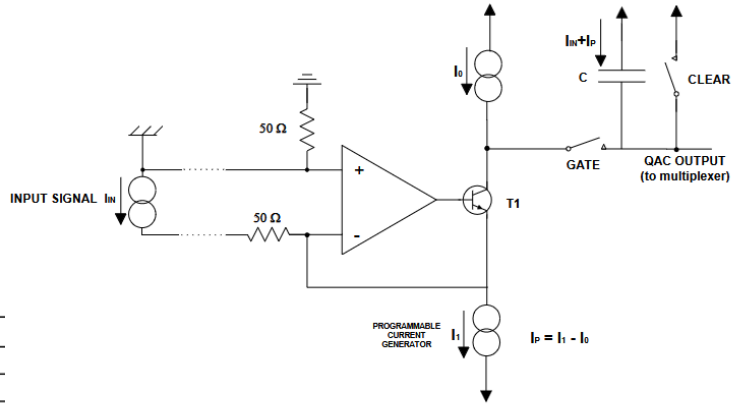


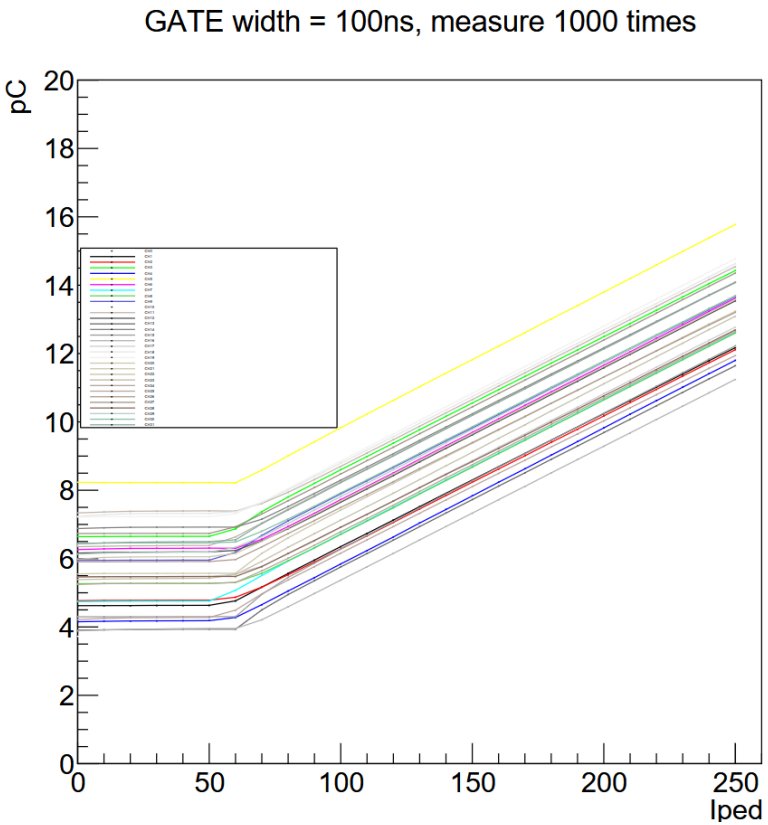
Fig. 2.4: QAC section (piggy back board rev. 2 and later)

Pedestal test

Use V1718 generate 100ns GATE signal

32 input channel un-connected

pedestal = 0, 10, 20, ..., 250



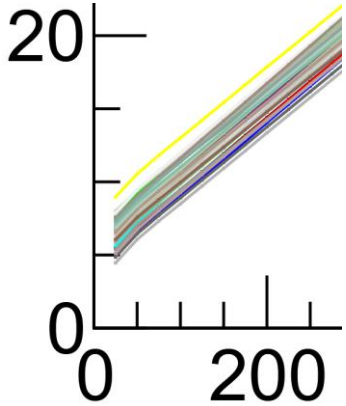
GATE width test

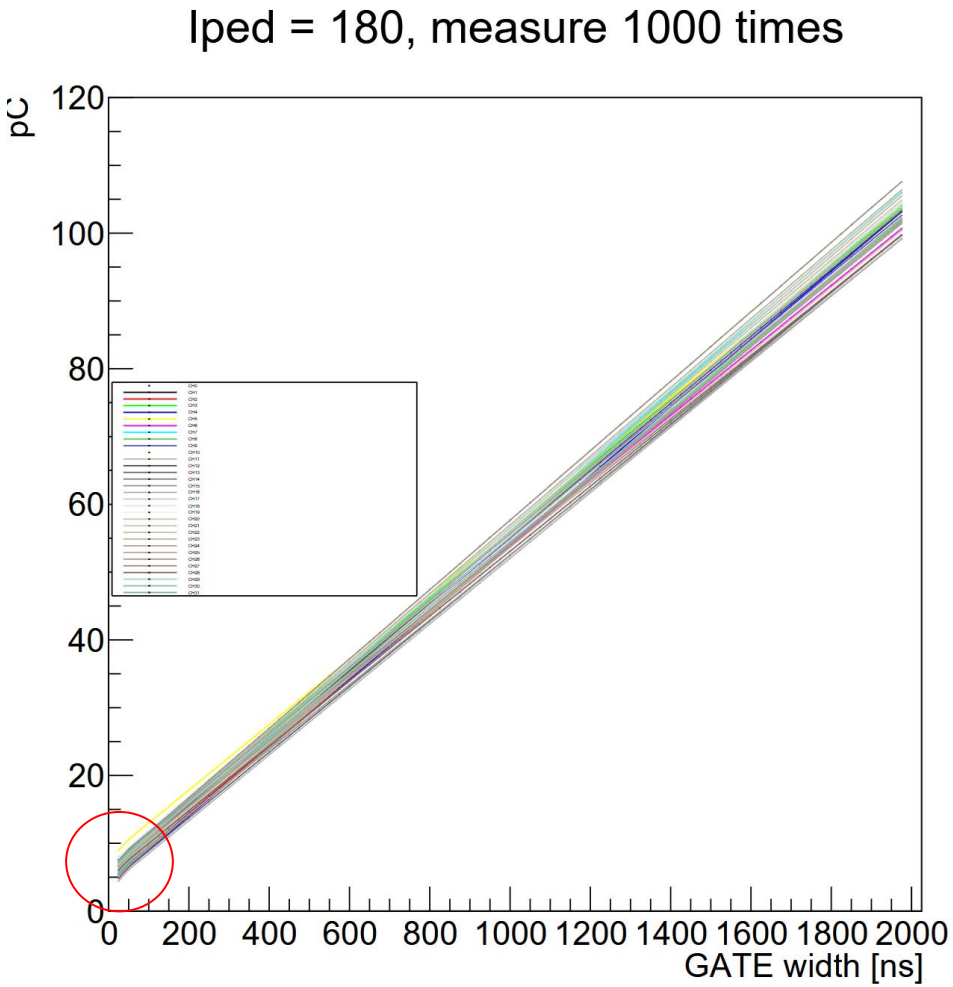
Use V1718 generate GATE signal

32 input channel un-connected

Fix pedestal = 180 (default)

GATE width = 25ns, 50ns, ..., 1975ns





V792 Data format

From Manual

UN = Under-Threshold

OV = Overflow

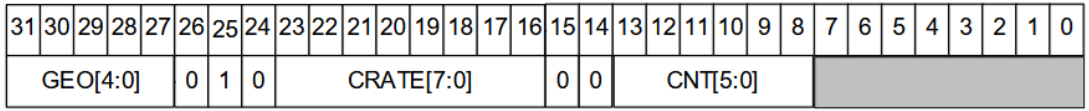


Fig. 4.5: Output buffer: the Header

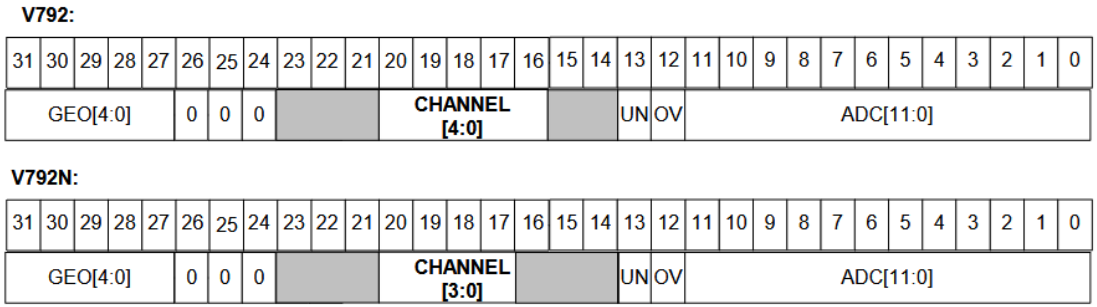


Fig. 4.6: Output buffer: the data word format

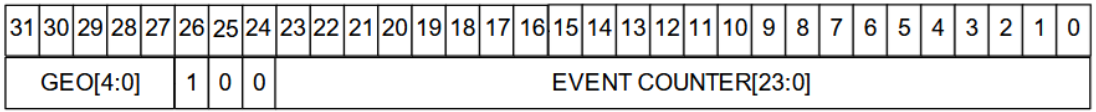


Fig. 4.7: Output buffer: the End Of Block

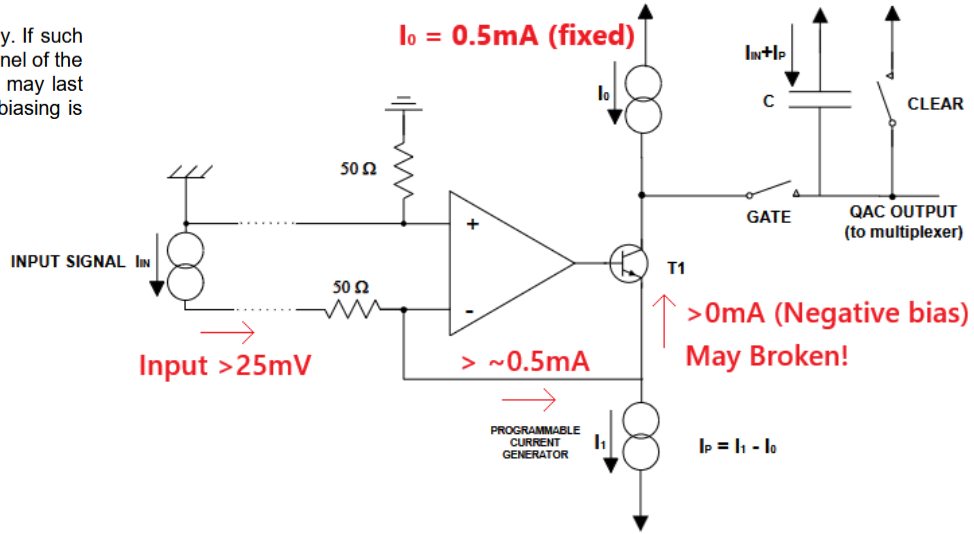
Maximum positive voltage input

2.1.4. Maximum tolerated positive voltage input

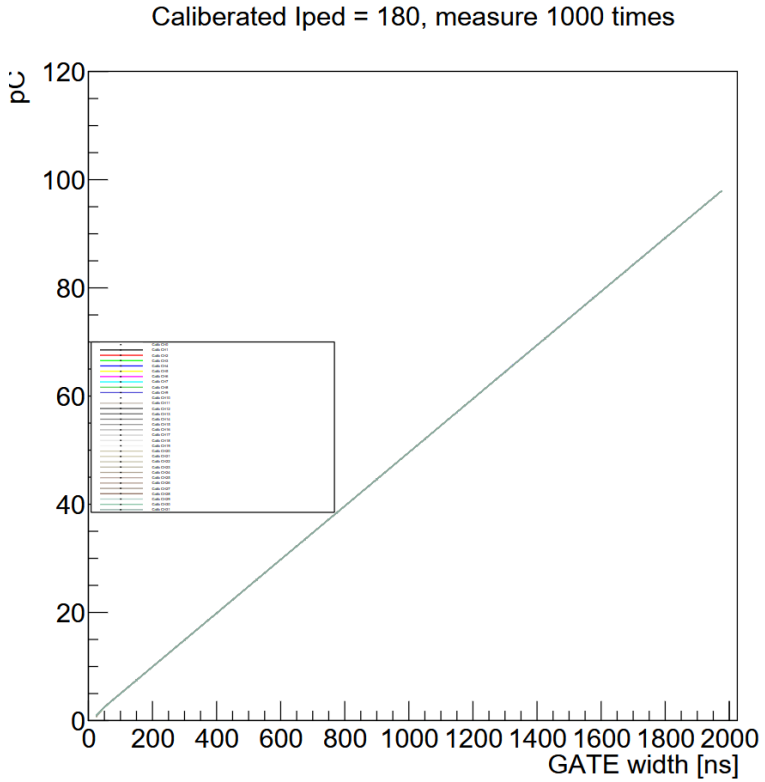
The ability of the input stage in tolerating a positive input voltage depends on the pedestal setting, according to the formula below:

Vmax (mV) = (Iped + 0.5) * 50

Where Iped (expressed in mA) is given by the settings described in § 2.1.2.1. Such maximum value is 30 mV circa when the Iped is set to its maximum.
This value guarantees that the input stage is biased correctly and works properly. If such value is exceeded, a BJT in the input stage will be reverse-biased and that channel of the QDC will not work; furthermore, this wrong biasing will cause a saturation that may last for tens or hundreds of µs. Permanent damages might occur if the reversed biasing is constant and/or the positive offset is a “spike” much greater than Vmax.



Questions


Caliberated Iped = 180, measure 1000 times
pC
120
100
80
60
40
20
0
0
200
400
600
800
1000
1200
1400
1600
1800
2000
GATE width [ns]