Solid State Detector

TIDC workshop on Future detector R&D for HEP

Sep. 10, 2021

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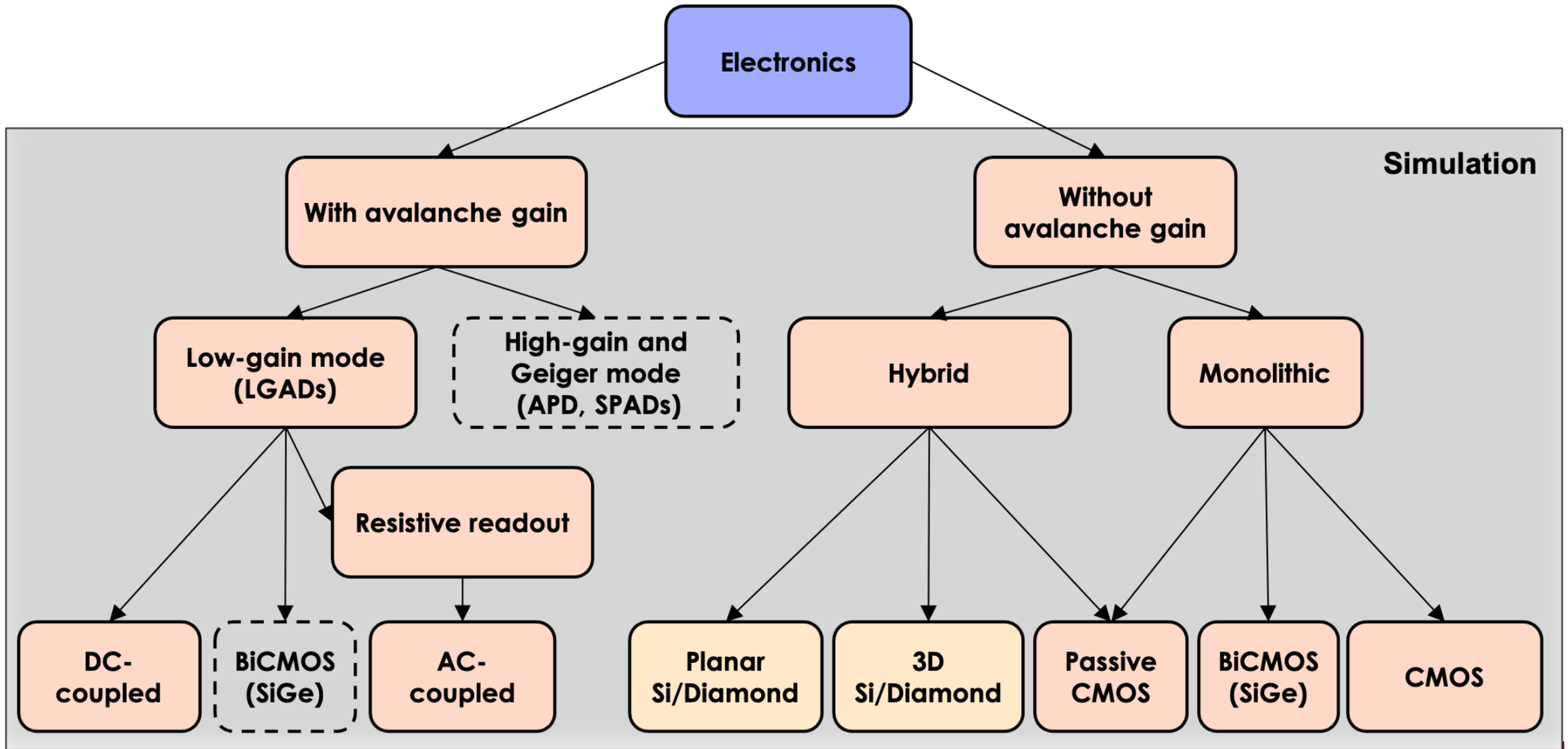
National Taiwan University

ECFA Solid State Detector Session

https://indico.cern.ch/event/999816/

Summary of the input section



N. Cartiglia, INFN Torino

Requirements for future solid state devices at accelerator experiments

Project timescales for new solid sate devices

Projects	Timescale	Vertex Det.	Tracker	Calorimeter	Time of Flight
Panda (Fair/GSI)	2025	✓			
CBM (Fair/GSI)	2025	✓			
NA62/KLEVER	2025	✓			
ALICE	2026-27 (LS3) – 2031 (LS4)	✓	✓	✓	✓
Belle-II*	2026	✓			✓
LHCb	2031 (LS4)	✓	✓		
ATLAS-CMS	2031 (LS4) - 2035 (LS5)	✓			✓
EIC	2031	✓	✓	✓	✓
ILC	2035	✓	✓	✓	✓
CLIC	2035	✓	✓	✓	✓
FCC-ee	2040	✓	✓	✓	✓
Muon-collider	> 2045	✓	✓	✓	✓
FCC-hh	> 2050	✓	✓	✓	✓

Projects representative of most demanding requirements, timescales reflect target for installation/start of operation – progress in specifications and state of approval can be at different stages**

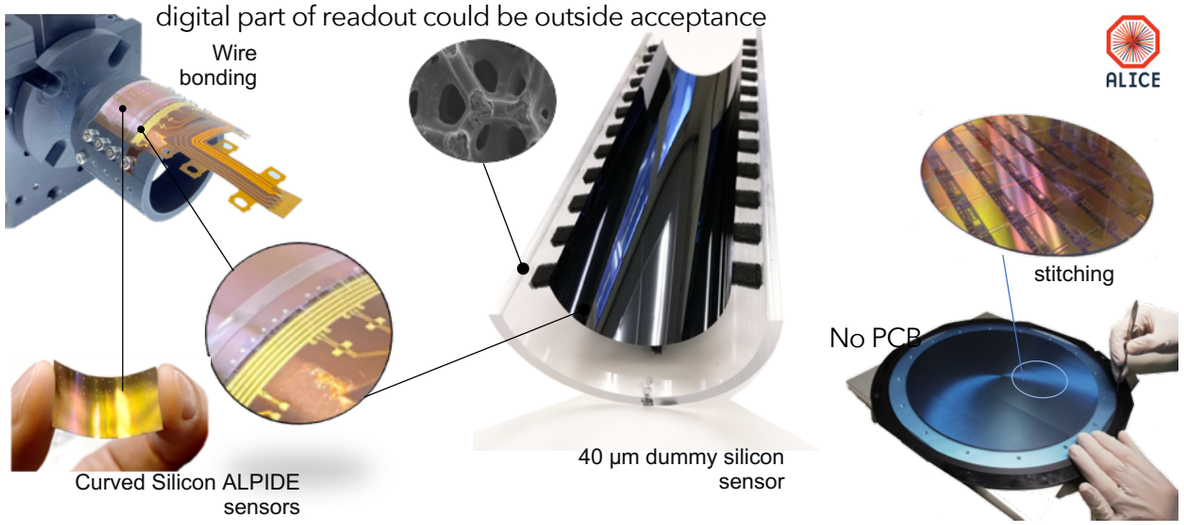
- R&D completion typically ≃ - 5 years for construction, and including typically ≃ 5 years system engineering on top or in // to technology demonstration***
- Upgrade programs earlier than future colliders provide opportunities to iterate technologies and mature systems in real operation environments

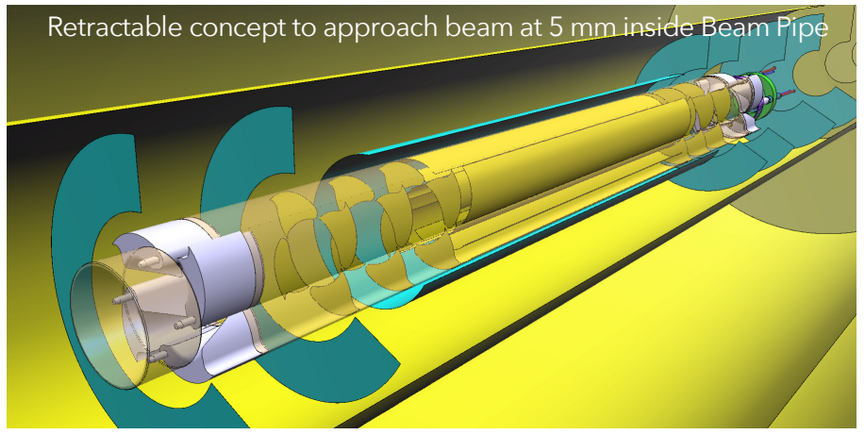
** Belle-2 may have another upgrade in 2030*
*** Alternative technology options are also considered for calorimetry and time of flight*
**** To minimize time and cost* several parameters need to be tested at once in few prototype iterations

Vertex Detectors high position precision

- Most demanding are ALICE and ILC, CLIC, FCC-ee colliders
  - FCC-ee target: $\sigma(d_0)/d_0 \simeq 2(20)$ μm at 100(1) GeV (90°), flavor physics benefit with higher precision
- Drivers are hit position precision (σ_{hit}), multiple scattering (X/X_0), layer configuration*
  - ALICE ITS3 target: $\sigma_{hit} \simeq$ 3 μm, $X/X_0 \simeq 0.05\%$ / layer
    - 10-20 μm pixel pitch, thickness down to 20 μm**
    - 12″ wafers (10 x 28 cm sensors), power ≃ 20 mW/cm^2 for gas flow cooling (TF7 and TF8)

➢ MAPs with stitching process in 65 nm node (TowerJazz)





From C. Gargiulo TF8 Symposia

ALICE ITS2: ALPIDE 30 μm pitch, 50 μm thick, $\sigma_{hit} \simeq 5$ μm, $X/X_0 \simeq 0.3\%$ / layer (of which only < 20 % from sensors, 16 mm bending test encouraging
** Beam pipe X/X_0 can depend on operating condition, ex x 2 thicker for FCC-ee compared to ILC for beam background reduction*
*** Charge sharing is an optimization of pitch, active thickness, pixel design and process, track angle, B-field*

Vertex Detector radiation tolerance

- ALICE, CBM, BELLE-2, EIC, ILC, CLIC, FCC-ee: NIEL $\lesssim 10^{15}$ neq/cm^2 and TID $\lesssim$ 100 MRad
  - Well within HV-CMOS radiation tolerance*
- LHCb, ATLAS, CMS: NIEL $\simeq$ 2-5 10^{16} neq/cm^2 and TID $\simeq$ 1 Grad
  - Marginally compatible with current hybrid technology requiring - inner layer replacement(s)
  - Limiting ability for low radius and forward η coverage

Challenge to enable MAPs to these levels (ex to be considered in ATLAS/CMS inner layer replac.)

- Lower technology nodes (65 nm – 28 nm)… process-design developments

Improvements of hybrid technology (would benefit LHCb)

- Smaller pitch and thinner planar/3D sensors, improved process and design
- Lower ASIC node 28 nm

** Even consistent for ILC, CLIC and FCC-ee with standard process rad. tol. $\simeq 10^{13}$ MeV neq/cm^2 and TID $\simeq$ 3 MRad*

Time of Flight precision requirements

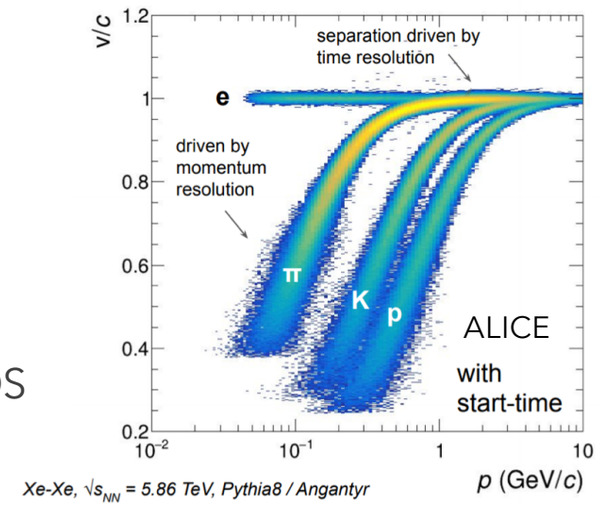
- Particle Identification (PID) dedicated layer(s)
  - ALICE 3 (post LS4), targeting $\sigma_t \simeq 20$ ps for 3σ π/K up to 5 GeV/c
  - Belle-2, FCC-ee similar requirement to cover dE/dx crossing at low P, better resolution highly desirable to extend PID potential to higher P
- 4D tracking for track collision time association
  - Dedicated layer(s) or implementation in VD and/or tracking layers*
  - ATLAS/CMS HGTD/MTD $\sigma_t \lesssim 30$ ps (pile-up mitigation) desirable for high η LGADS replacement in LS4-LS5 (for rad. tol.)
  - LHCb pile-up mitigation for vertex precision
  - Options for e-e colliders to reduce beam backgrounds and improve 1st, 2nd, 3rd vertices identification, to be balanced with impact on X/X_0
  - FCC-ee at $\sigma_t \simeq 6$ ps can allow to correct √s variation within bunches

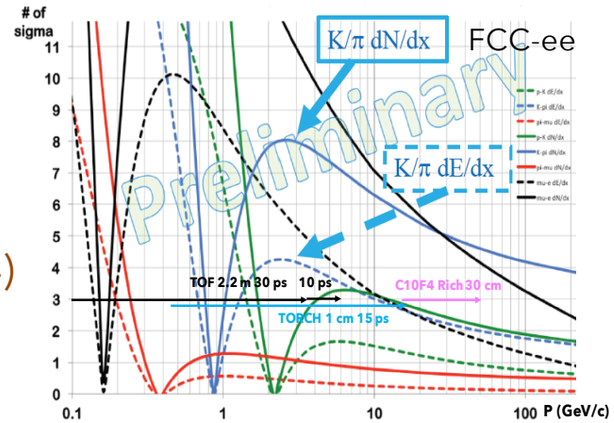
Develop designs with fast signal collection, small stochastic fluctuation

- ➢ w/o amplification (MAPS, Hybrids 2D/3D)**, w/ amplification LGADS***, SPADS (TF4)
- ➢ Improve radiation tolerance, develop LGADs with pixel pitch,

Develop fast FE (TF7)

- ➢ Pre-amp with similar rise time as signal, high resolution TDC and clock distribution, with low power in high channel density (technology nodes 65 – 28 nm)





** Number of layers in tracking systems would improve track time resolution, also for PID*
*** NA62 VD achieved $\sigma_t \simeq 100$ ps and CMS HGC $\sigma_t \simeq 50$ ps with current 2D hybrid sensor technology*
**** Currently $\sigma_t \simeq 25$ ps limited by Landau fluctuation*

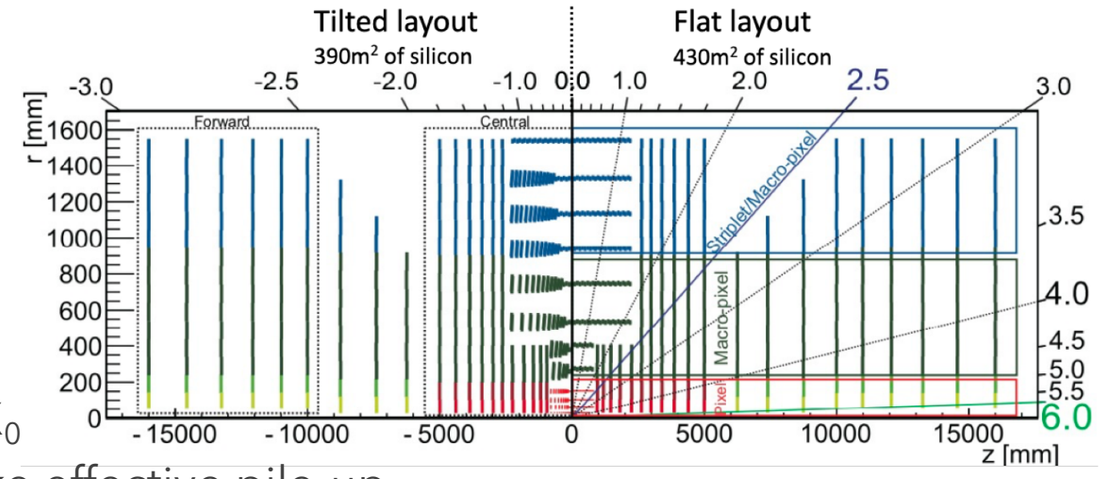
FCC-hh requirements

New territory of operation conditions

- L = 30 x 10^{34} cm^{-2} s^{-1} – 30 GHz of collisions 1000 per BC - 30 ab^{-1} integrated over physics program
- Physics coverage up to η = 6

Tracking requirements

- <0.4> ps vertex separation and <130> μm
  ≃ BP MS resolution limit for 1 GeV/c p_T at η = 2
- Track rates 30 GHz/cm^2 (r = 2.5 cm)
- Granularity close to FC-ee with pitch ≃ 25 μm
- Precision will be limited by ability to minimize X/X_0
- σ_t ≃ 5 ps would be required to recover HL-LHC like effective pile-up
- Fluence 10^{18} neq/cm^2 and TID 30 GRad at 2.5 cm*



New paradigms needed for radiation tolerance**

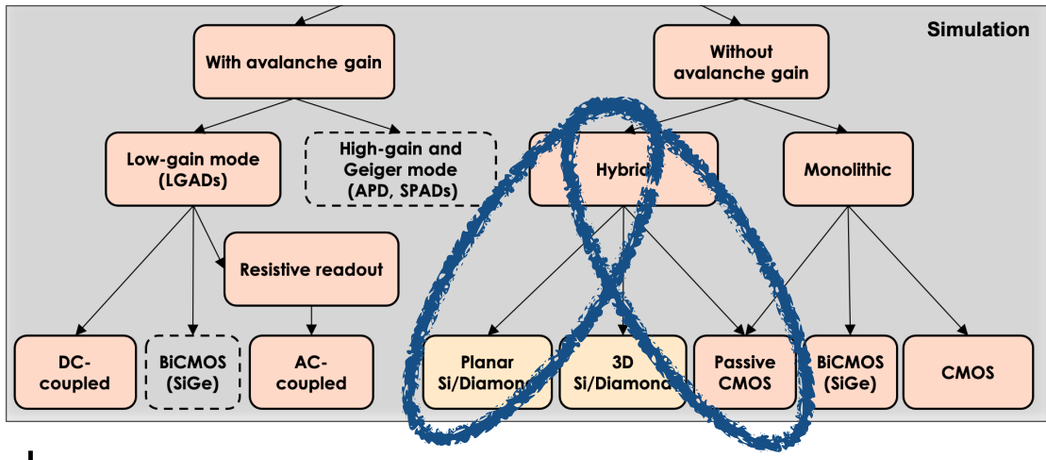
- R < 30 cm out of reach of currently used hybrid sensor technologies
- Current MAPS and LGADS marginally at level of rad. tol. for outermost layers

New paradigms needed for rates (TF7)**

** Forward calorimetry requires up to x 2-5 higher rad. tol. – timing at similar level as for tracking could also be needed to mitigate pile-up*
*** HE-LHC @ 2 HL-LHC would also need new technologies*

Passive CMOS

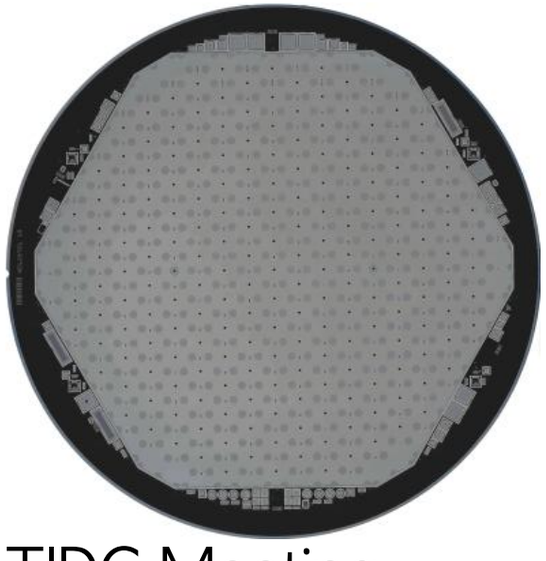
Passive CMOS Sensors



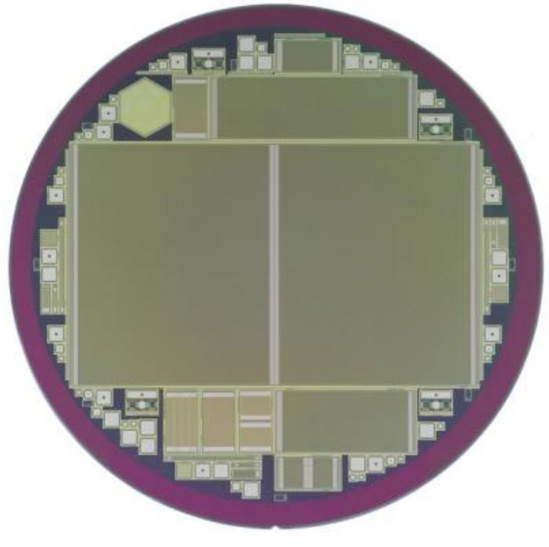
- Current situation :
- Full-wafer lithography with 6/8 inch wafers for passive sensors
- Increasing demand for large-scale production
- Only few large-scale suppliers available; Risk of single-vendor (Hamamatsu) supply (Infineon, Austria, participated CMS phase 2 tracker R&D but dropped out to focus on CMOS-ASIC production)

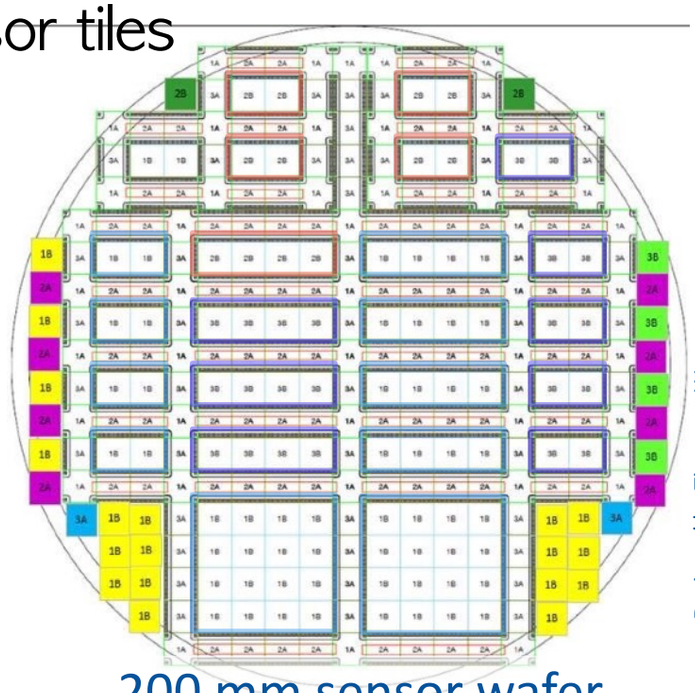
- Idea :
- Use CMOS processing lines (foundry) on large, high-resistivity wafers
- N-well/p-well/metal layers for sensor implantations and biasin
- No active components ➔"passive CMOS" (not MAPs)
- Stitching over reticle boundaries for large sensor tiles

8" p-type pads



8" p-type strips





Designed by Tianyang Wang

200 mm sensor wafer

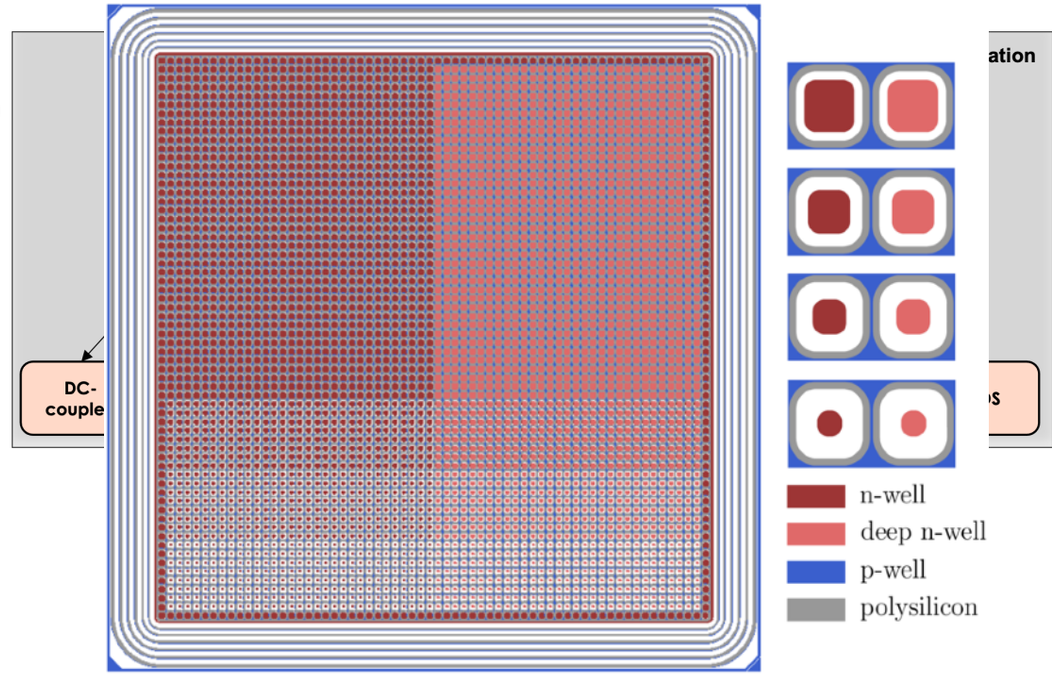
台灣光罩/NCKU experiences

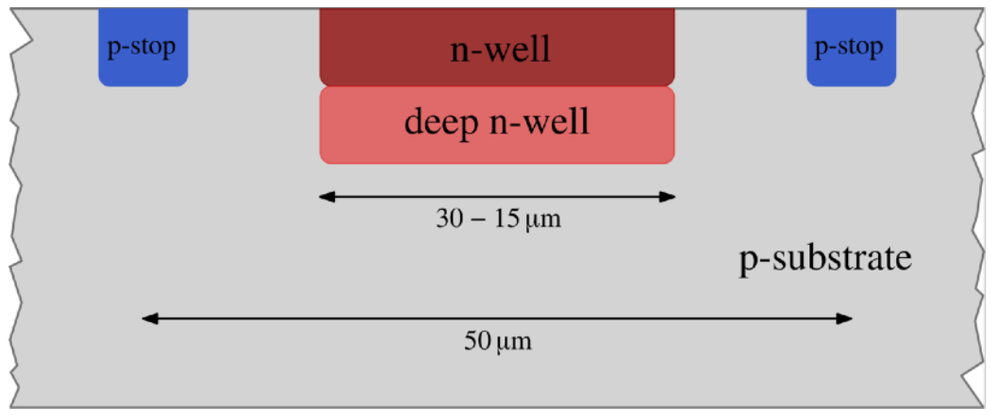
- Most recently,
  - 台灣光罩 has produced 6-inch CMS HGCAL p-on-n passive pad sensors and
  - NCKU has a grad student 李宸葳 working with 台灣半導體研究中心 (TSRI) to reproduce STAR p-on-n passive strip sensors.
- In short, they are (still) not easy. We know the principle but know-how is the gold. The experience is still worth the effort if we will pursue the passive sensor production in the future.

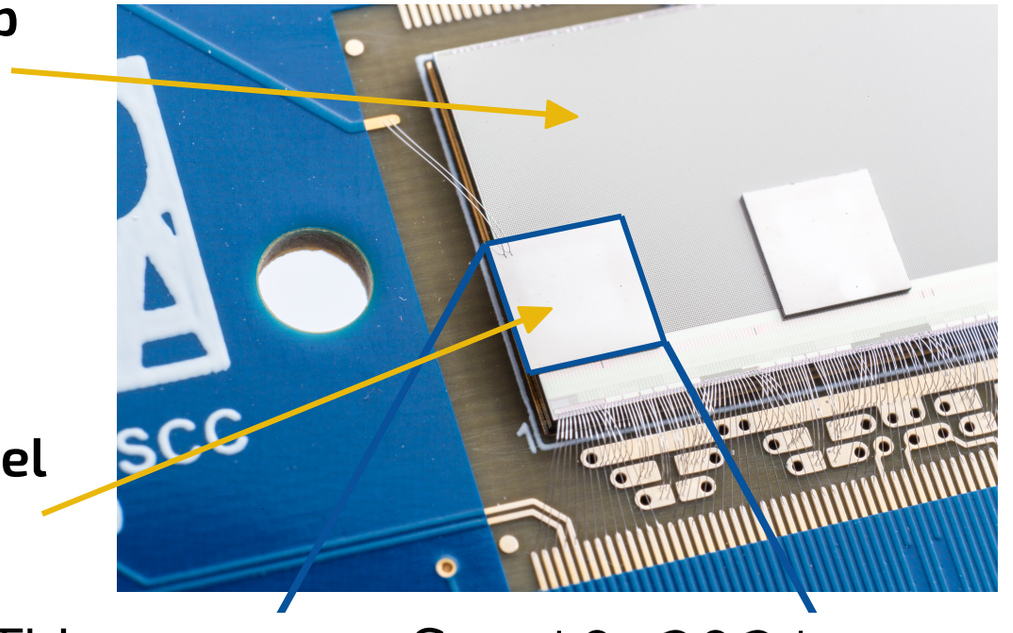
Passive CMOS

Passive CMOS pixel sensors in 150 nm LFoundry technology bump-bonded to the RD53A readout chip

- High resistivity 4-5 kΩ cm p-type CZ wafer
- 50 µm x 50 µm pixels in 64 × 64 matrix
- 100 µm thickness with TAIKO thinning
- Bump bonded to RD53A
- DC coupled pixels:
  - No biasing structure
  - Variation of implantation width: 15 µm - 30 µm
  - Variation of n-well depth: n-well (NW) and deep n-well (DNW)
- More info in: https://doi.org/10.1016/j.nima.2020.164130





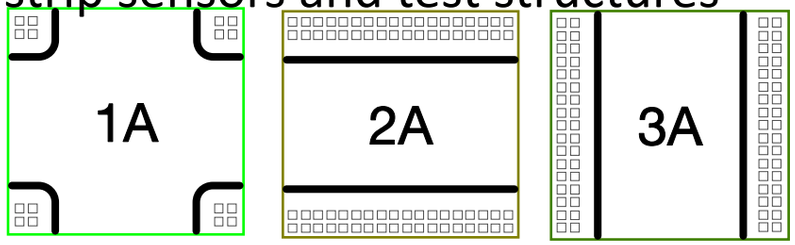


Passive CMOS

STITCHING

- Sensor size > reticle size
  → Stitching needed
- Additional rules for stitching (no fine-pitch)
  → Not too relevant for sensor designs
- Different blocks:

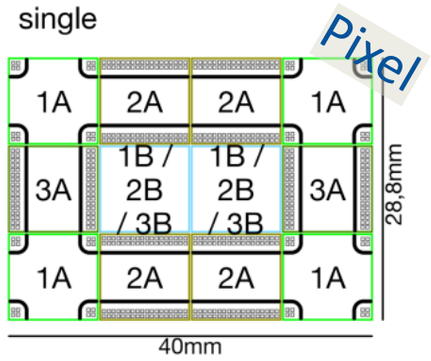
  Edge blocks with guard rings,
  strip sensors and test structures

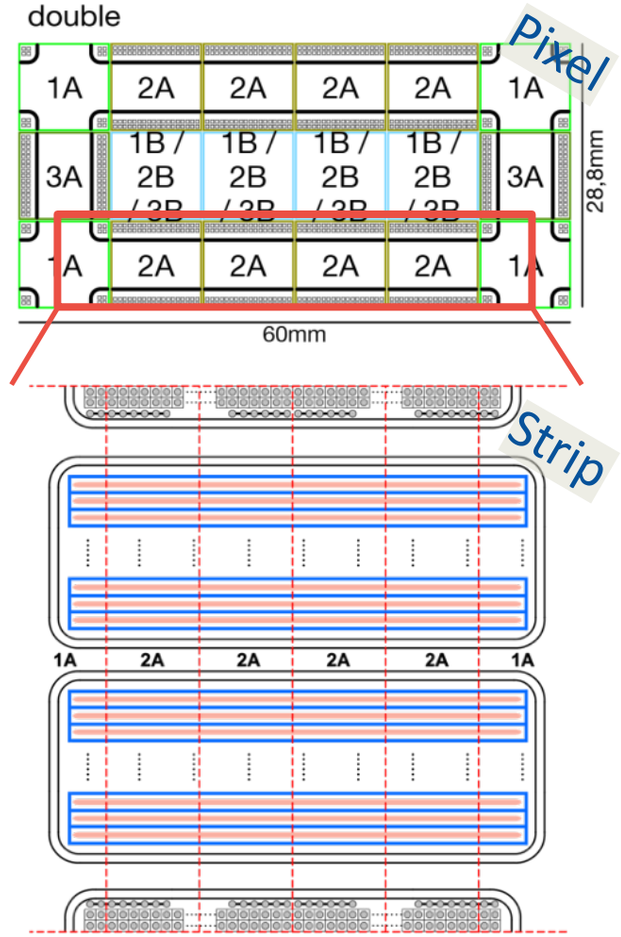


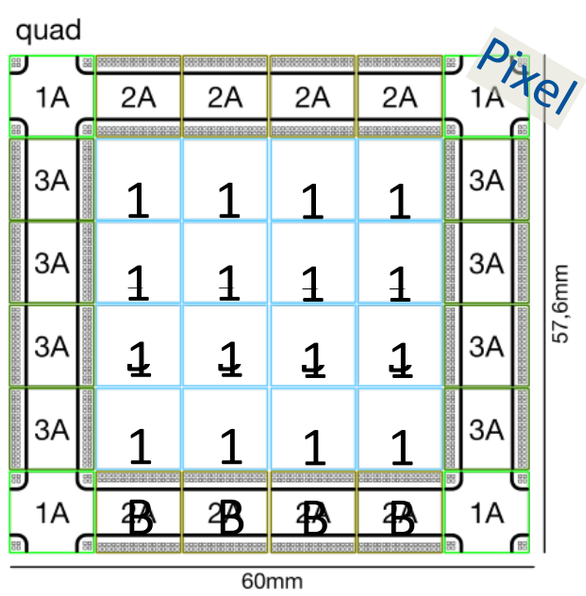
Center blocks with different pixel flavors

DC coupled	AC coupled	DC coupled
1B	2B	3B
50 x 50 µm²	50 x 50 µm²	25 x 100 µm²

- Different configurations possible
  → arrange and repeat blocks in different order



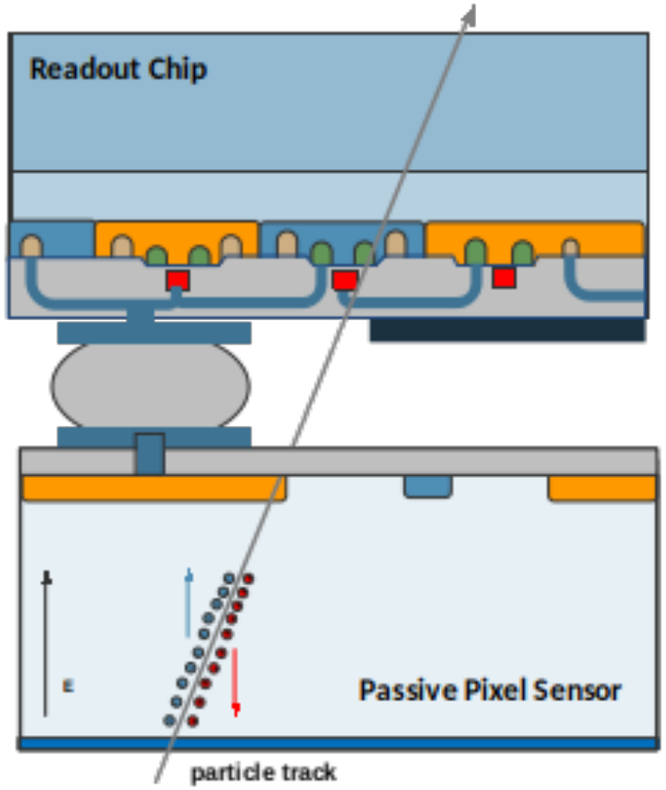




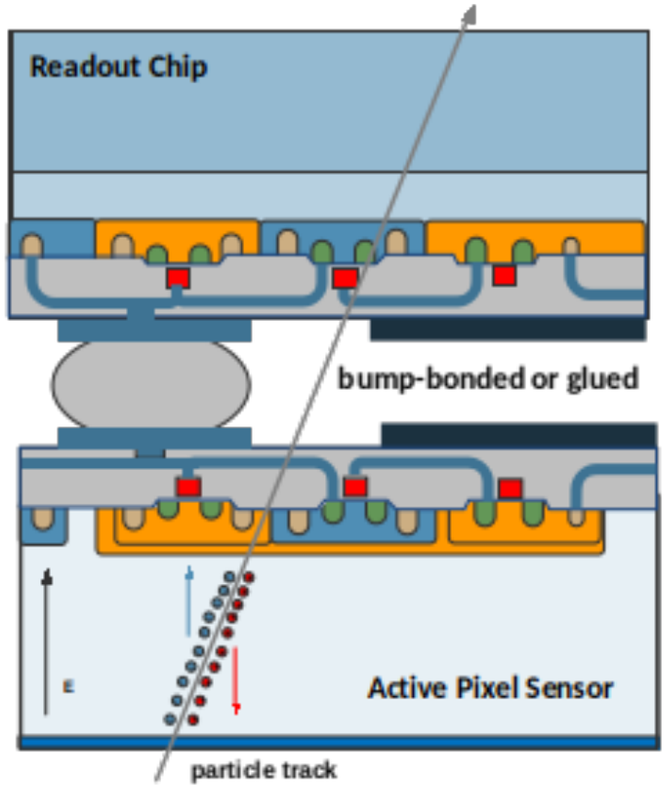
Passive CMOS

OUTLOOK: ACTIVE CMOS HYBRIDS?

Standard Hybrid



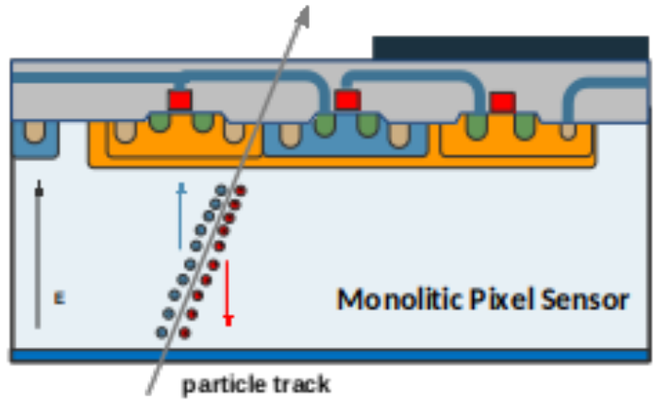
Active CMOS Hybrid



Depleted Monolithic

➔ ECFA talk

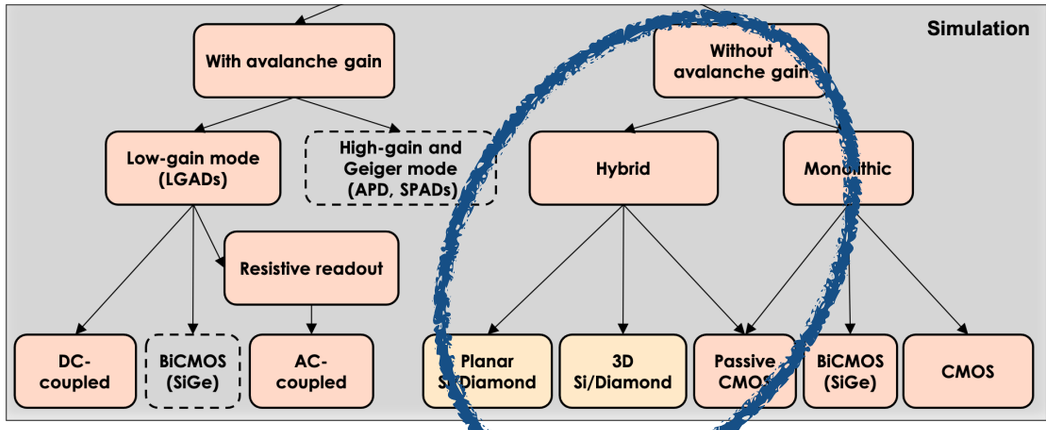
by P. Riedler today
14:30



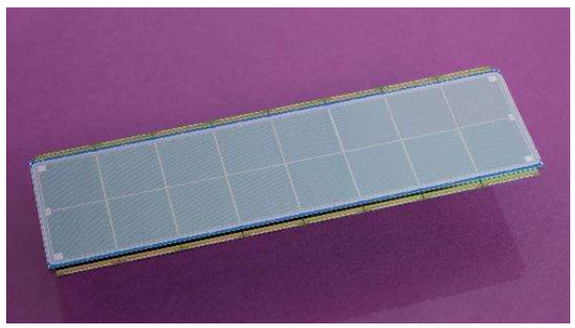
- CMOS active hybrids for high performance solutions (extreme irradiation and hit rates):
  - Active CMOS sensor (amplification included)
  - Digital readout: smaller feature size process for digital logic

InterConnect

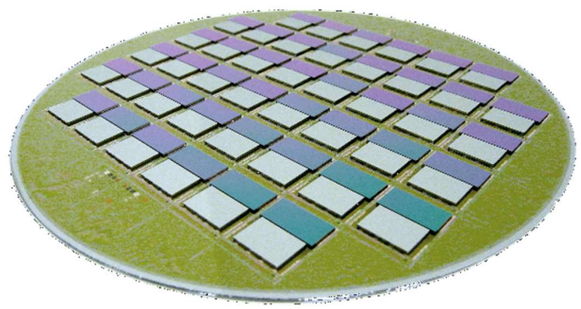
Future Requirements on Interconnection Technologies for Hybrid Detector Modules

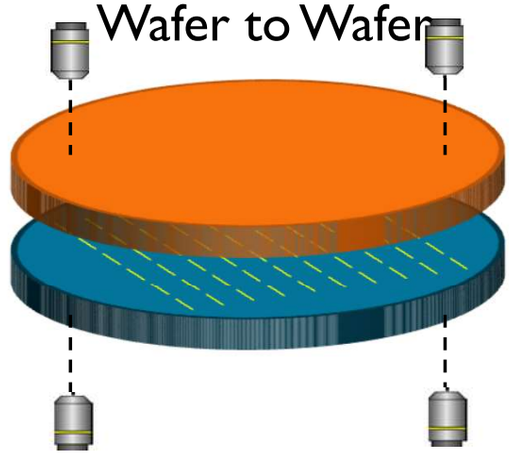


Chip to Chip



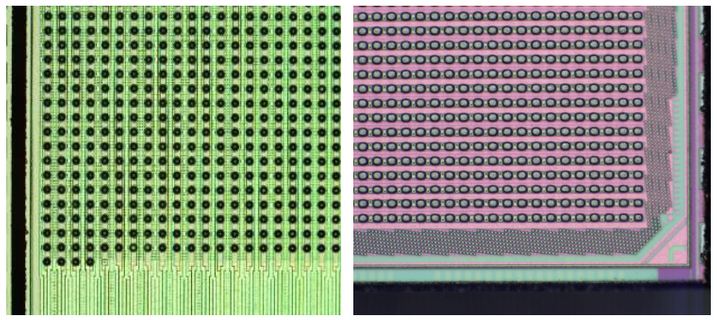
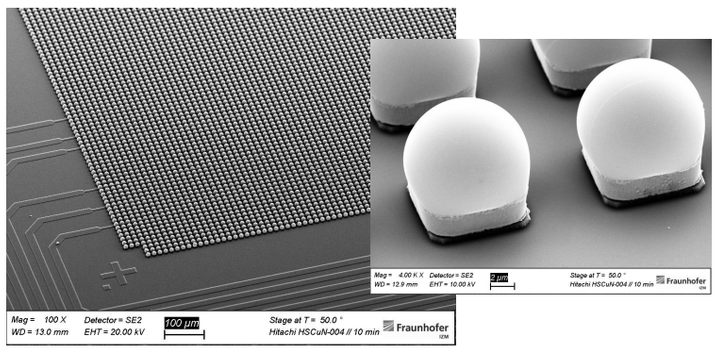
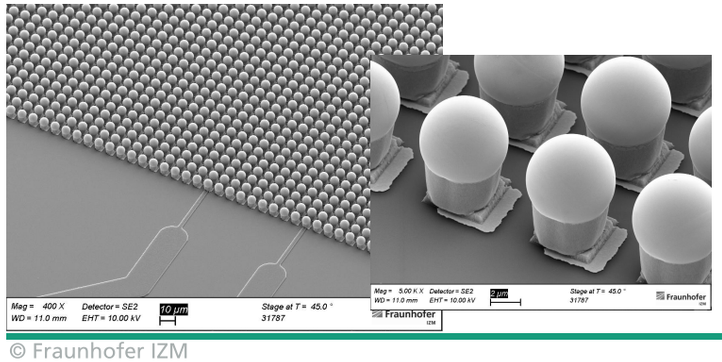
Chip to Wafer





- Assembly by Flip Chip Bonding : Chip-to-Chip, Chip-to-Wafer
  - Require High accuracy of pick and place $< 1\mu\mathrm{m}$
  - Chips/wafers diced, different size and pattern can be merged.
- Assembly by Flip Wafer Bonding : Wafer-to-Wafer
  - Require wafer size and pattern matched between top and bottom wafer

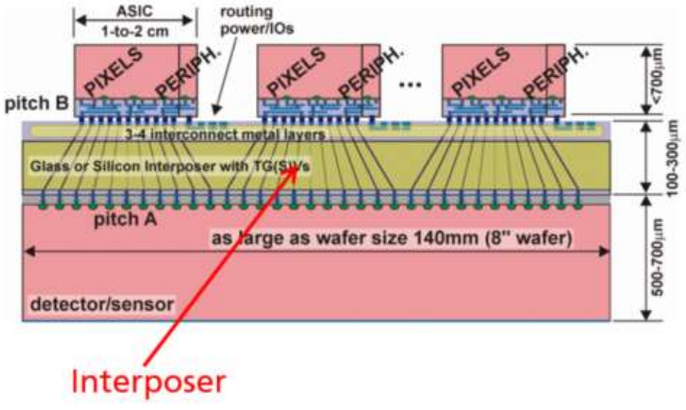
Solder Bump Bonding – Bump Size and Bump Pitch Developments

	Bump pitch	Bump size/material	Wafer size
	RD53/ITKPix: 50µm	RD53/ITKPix: 50µm SnAg	300mm TSMC65nm
	ClickPix2: 25µm	ClickPix2: 17µm SnAg	Single chips
	IZM Test-chip: 15µm	IZM Test-chip: 9µm In, SnAg	200mm
	IZM Test-chip: 7.5µm	IZM Test-chip: 4µm In, SnAg	200mm

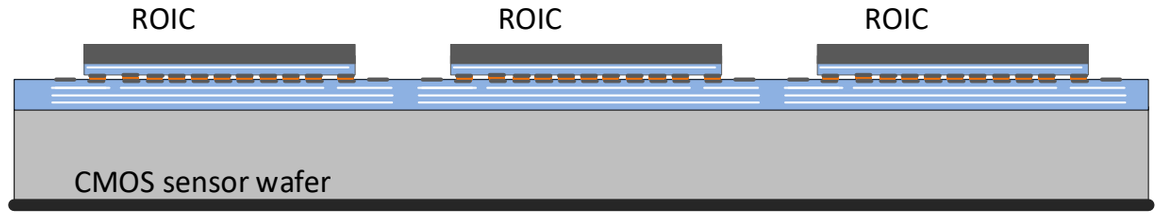
InterConnect

Concept in HEP: CMOS Sensor Interposer

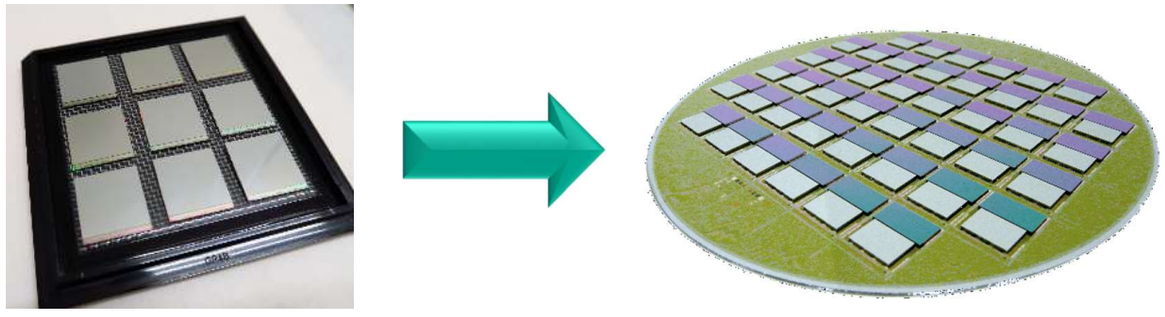
Concept presented by Grzegorz Deptuch, Fermilab, CPIX 2014:



- Readout chips bonded onto Si/Glas Interposer top side with bumping pitch B
- Sensor bonded onto interposer bottom side with pitch A
- Interposer to sensor W2W bonding possible
- ROC assembly by C2W bonding possible



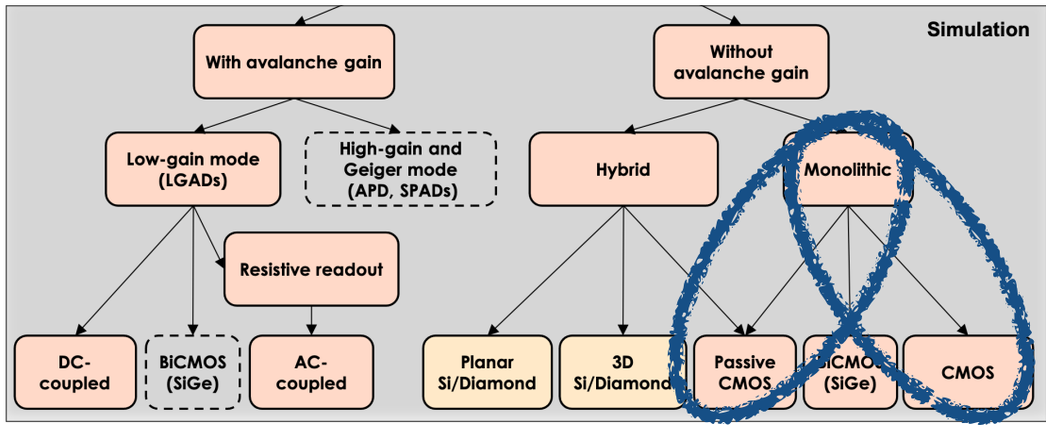
- Readout chips bonded onto sensor wafer with BEOL RDL and bonding pads
- Readout IO contact pad fan-out RDL on sensor top metal layer
- Connection to module support flex via bond pads on sensor
- optional ROCs with TSV first or middle → reduce post processing steps
- C2W assembly → sensor chip has to be slightly bigger than ROC



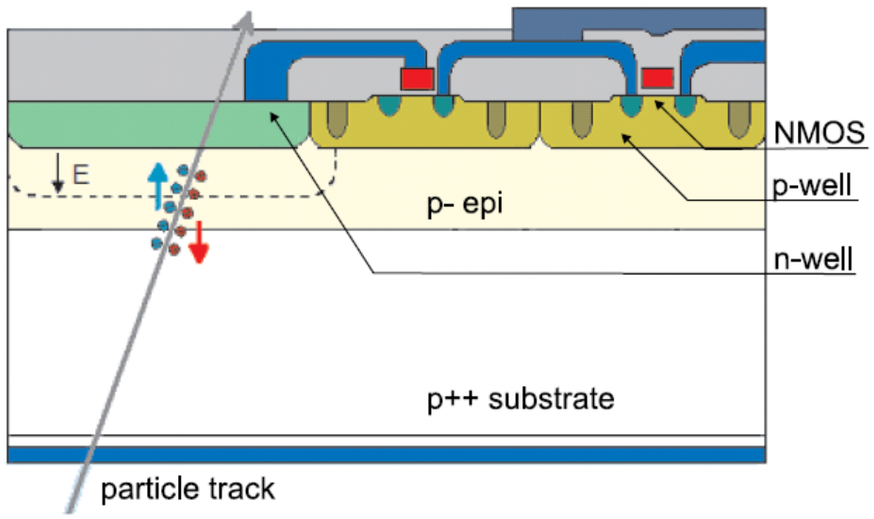
- Adaption of trends from industry for integration technologies, i.e.
  → chiplet stacking
  → embedding and fan-out packaging
  → photonic packaging

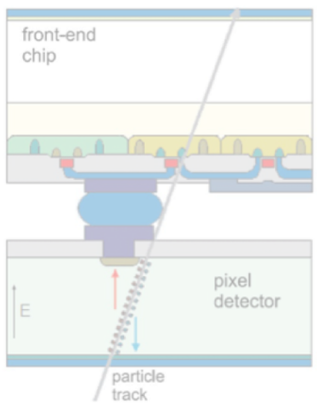
CMOS sensor

CMOS monolithic silicon pixel sensor



Offer a number of interesting aspects that can help to address these points:





Hybrid silicon pixel detector

FE electronics and sensor are integrated in one piece of silicon and produced in commercial CMOS processes → see *talk by W. Snoeys.*

Commercial processes offer high volume and large wafers (200mm, 300 mm) that reduce detector cost and opens possibility for large quantity productions.

CMOS sensors can be thinned to achieve ultimate low mass trackers (0.3% X_0 in Heavy-Ion experiments or <1% for pp).

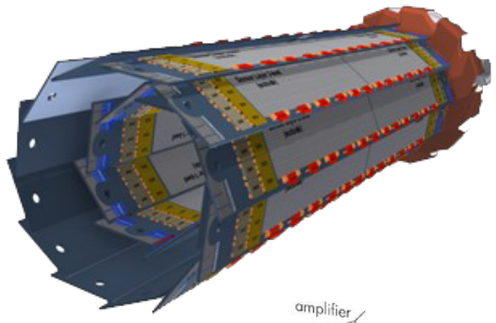
Small pixel sizes (~20 µm)).

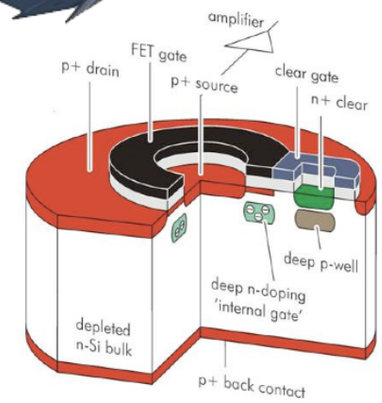
No cost (and complexity) of bump-bonding.

Highly integrated modules using industrial post-processing tools.

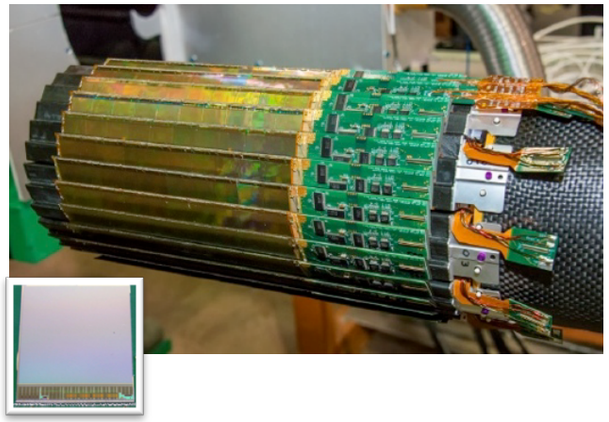
CMOS sensor

Monolithic sensors in HEP move into mainstream technology





DEPFET in Belle



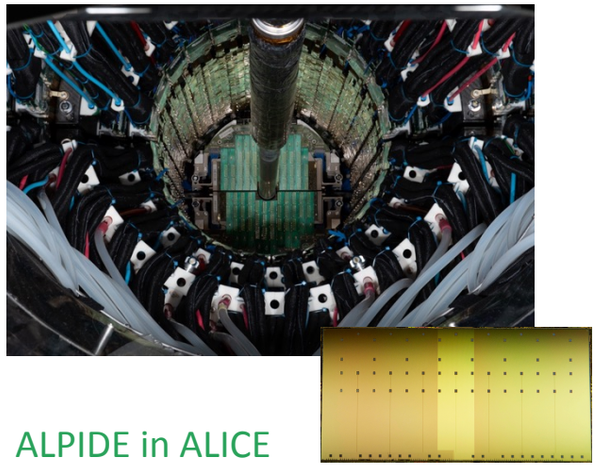
MIMOSA28 (ULTIMATE) in STAR

IPHC Strasbourg

First MAPS system in HEP

Twin well 0.35 µm CMOS

- Integration time 190 µs
- No reverse bias -> NIEL few 10^{12} 1 MeV n_{eq}/cm^2
- Rolling shutter readout



ALPIDE in ALICE

First MAPS in HEP with sparse readout similar to hybrid sensors

Quadruple well 0.18 µm CMOS

- Integration time <10 µs
- Reverse bias but no full depletion -> NIEL ~10^{14} 1 MeV n_{eq}/cm^2

DEPLETED MAPS for better time resolution and radiation tolerance

Large collection electrode

LF Monopix, MuPix,…

Extreme radiation tolerance and timing uniformity, but large capacitance

Small collection electrode

ARCADIA LF, TJ Malta, TJ Monopix, Fastpix, CLICTD, …

- Sub-ns timing
- NIEL >10^{15} 1 MeV n_{eq}/cm^2 and beyond

Commercial deep submicron CMOS technology evolved “naturally” towards

- Very high tolerance to ionizing radiation (some caveats, cfr G. Borghello, F. Faccio et al.)
- Availability of substrates compatible with particle detection
- Imaging technology not absolutely required, but some flexibility/features very beneficial for sensor optimization, both for small and large collection electrode structures.

CMOS sensor

- Developments : Sensor optimization: Moving the junction away from the collection electrode for full depletion, better time resolution and radiation hardness… and better efficiency, especially for thin sensors
- Challenges : Power consumption (analog and digital) and distributions; Yield if sticking to large area;
- LGAD (mentioned later in 4D sensor) is part of the MAPS development, and there are many more including industrial applications like medical imaging to medical tracking.

Concluding remarks

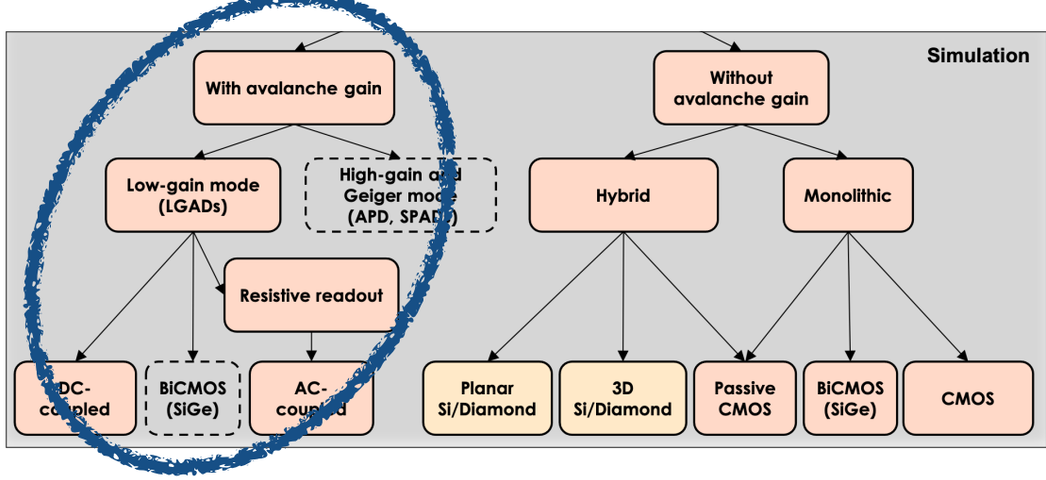
A Monolithic Active Pixel Sensor or MAPS is a complex circuit with extra constraints: sensor bias, coupling into the sensor, …

- The increasing complexity of the sensors and the chips we design require evolution towards digital-on-top design techniques with increasing verification effort (cfr F. Faccio and A. Rivetti's presentations).
- Need team of expert chip designers, complemented with device/TCAD/Monte Carlo experts for sensor optimization and simulation. It takes years to train people for this activity and our community, also at CERN, does not sufficiently preserve critical mass and know-how for this activity.

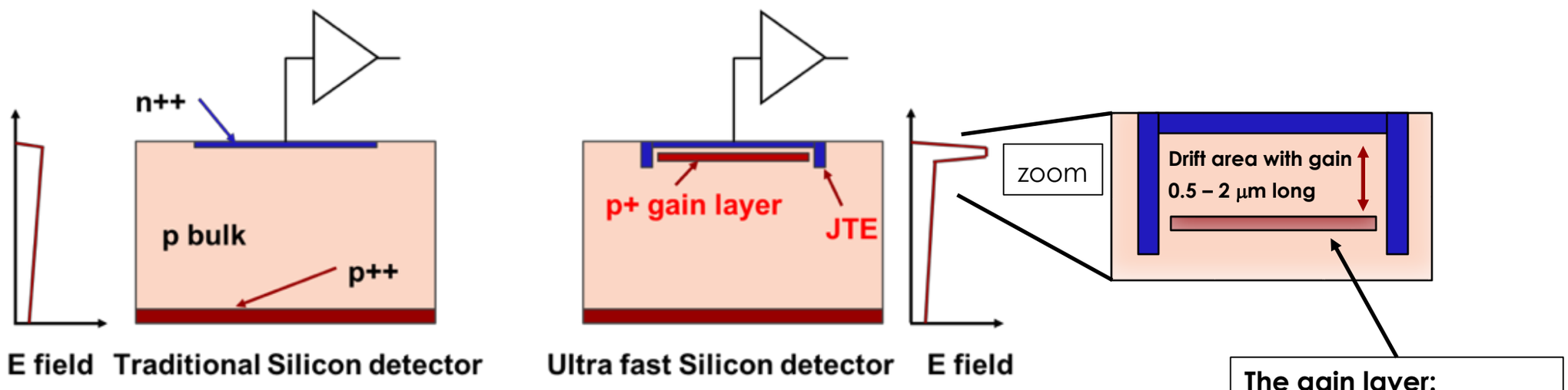
Large area pixel sensors are enabling devices for many cutting edge research fields and practical applications like tracking in HEP, medical imaging, space-borne instruments, etc, illustrated by the interest in chips like ALPIDE and others but also by other successful developments like Medipix/Timepix

MAPS are one of the few areas where production volume even within HEP would not be negligible, but where our community can have an impact not only on the quality of its own measurements, but also on society in general, and which we should try to exploit to enable access to the most advanced technologies.

4D tracking – sensors with internal gain



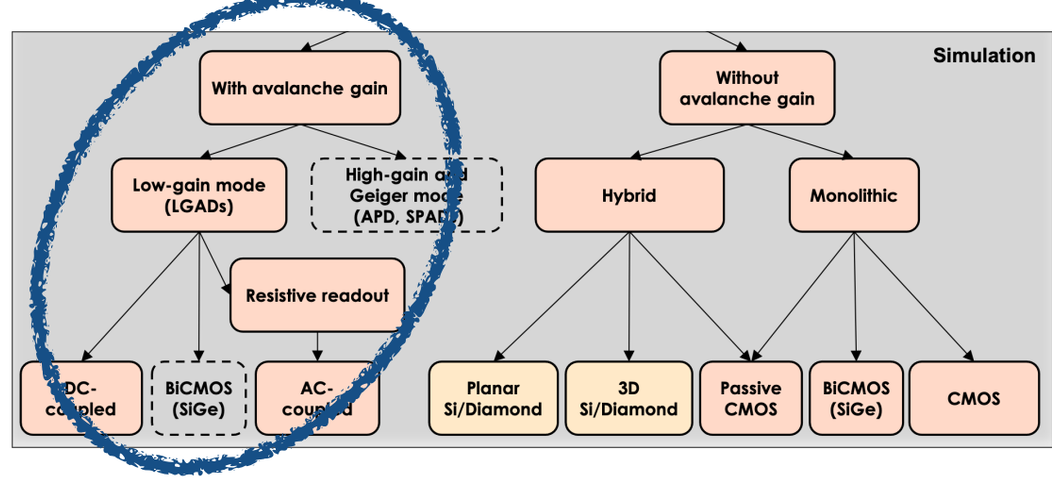
- First design innovation: low gain avalanche diode (LGAD)
  - ~ 20 gain, thin sensors, large signals, large dV/dt .
  - Excellent timing resolution (~ 30 ps), not so good spatial resolution (pixel/sqrt(12))
- Second design innovation: resistive read-out (joining RPC, GEM..)
  - Spread the signal over many pads while maintaining good efficiency (due to internal gain)
  - Excellent position and timing resolutions (<5 um, ~ 30 ps)
- Hybrid detector. Needs ASIC to readout amplified signal.



The LGAD sensors, as proposed and first manufactured by CNM

(National Center for Micro-electronics, Barcelona):

4D tracking – sensors with internal gain



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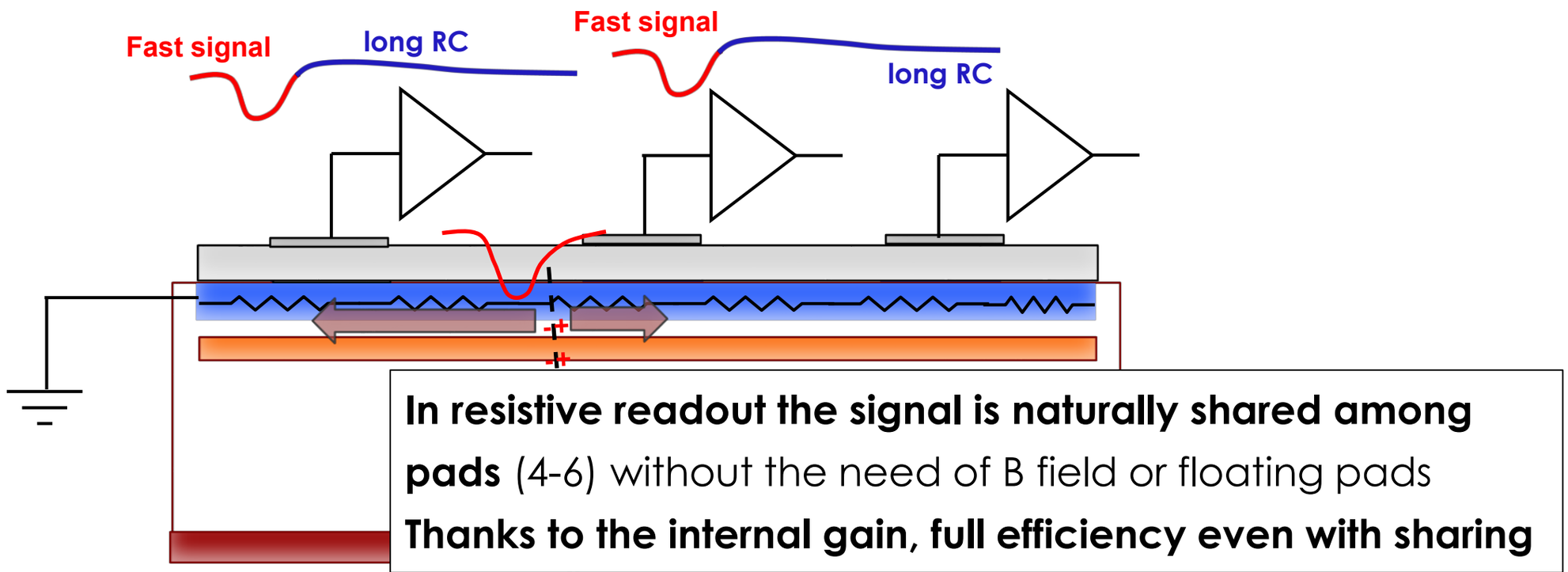


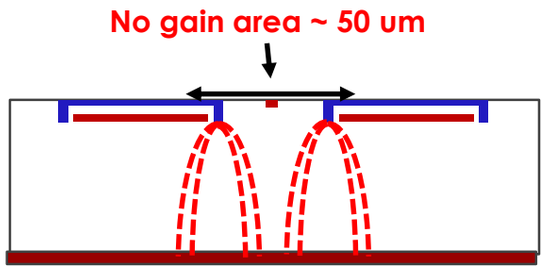
ECFA
European Committee for Future Accelerators

Manufacturers: a pretty large pool

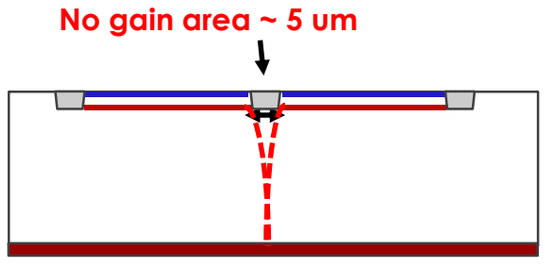
Red: Research Institutions
Blue: large commercial manufacturers

Producer	LGAD	RSD	Funding Source	Collab. Institute	Projects
CNM Barcelona (Spain) RD50 member	Doping Radiation Arrays Carbon, Gallium	Time Resolution	Spanish Ministr. RD50 (DoE R&D) AIDA	IFAE RD50	ATLAS HGTD CMS-ETL
FBK Trento (Italy) RD50 observer	Radiation Carbon Isolation	Detailed investigation: Geometry Spatial & Time Resolution.	INFN, ERC AIDA RD50 (DoE R&D)	INFN Torino RD50	ATLAS HGTD CMS-ETL
Micron (UK)	Small Pixels		UK Science Council	Glasgow U.	X-ray Diamond
HPK (Japan)	Doping Thickness Radiation Arrays	Time Resolution	(DoE R&D) BNL ATLAS CMS	UCSC KEK	ATLAS HGTD & CMS-ETL Collaboration
BNL (US) RD50 member		Time Resolution	DoE LDRD	BNL FNAL UCSC	
NDL (China)	8"		Chinese Gov	IHEP	ATLAS HGTD
IME (China)	8"		CAS	USTC	ATLAS HGTD

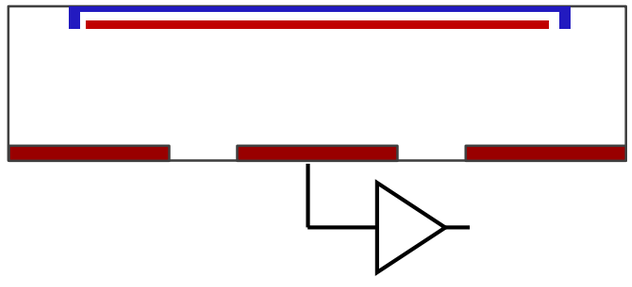
LGAD Present results & short term evolutions



JTE + p-stop design



Trench-isolated design



JTE/p-stop LGAD

- CMS && ATLAS choice
- Signal in a single pixel
- Not 100% fill factor
- Very well tested
- High Occupancy OK
- Rate ~ 50-100 MHz
- Rad hardness ~ 1-2E15 n/cm2

LGAD evolution: use trenches

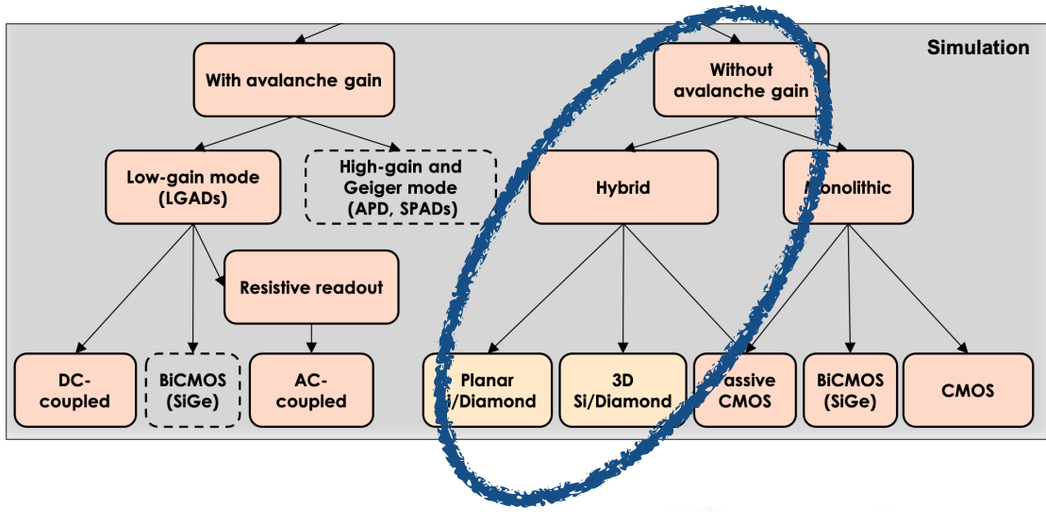
- Signal in a single pixel
- Almost 100% fill factor
- Temporal resolution (50 μm) : 35-40 ps
- High Occupancy OK
- Rate ~ 50-100 MHz
- Rad hardness: to be studied

i-LGAD

- p-side segmentation
- Signal in a single pixel
- 100% fill factor
- Thin i-LGAD with single side processing under development (using trenches, spring 2021 @ CNM)
- High Occupancy OK
- Rate ~ 50-100 MHz
- Rad hardness: to be studied

- In the far future, thin LGAD can do better in timing, but from 30 ps to 10 ps per hit is difficult
- Spatial resolution : $< 5\mu\mathrm{m}$ for RSD, $\sim 100\mu\mathrm{m}$ for LGAD.
  - LGAD have a resolution of pixel/sqrt(12). If goes to small pixel, timing measurement is difficult.
  - RSD has an extraordinary position resolution with large pixels but only for low occupancy experiments

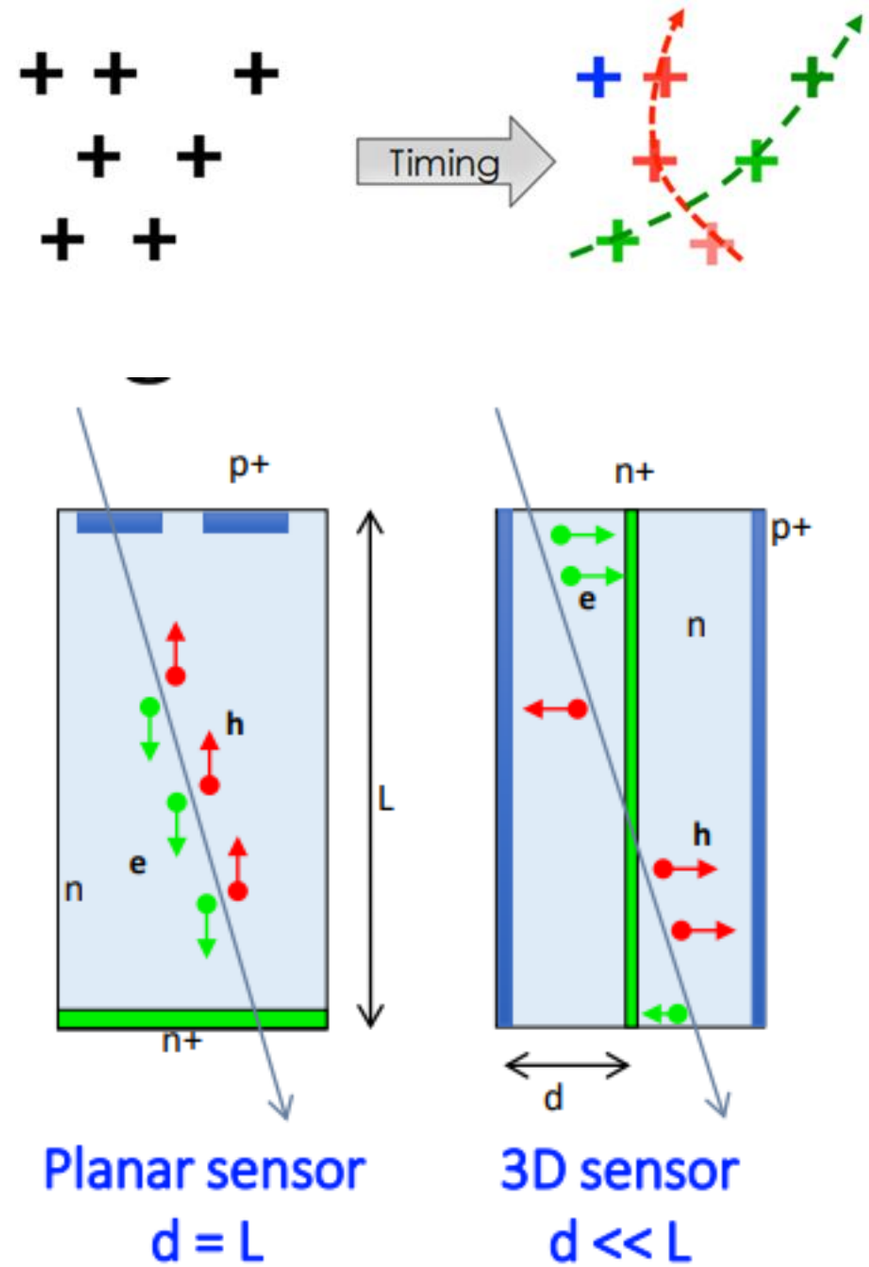
4D tracking - sensors without internal gain - 3D and intrinsic limitation



- 3D pixel detector has been installed in ATLAS and is known to be more radiation tolerated than planar.

- 3D can be fast from short drift distance, thus compatible with timing detector design

- Still a passive sensor with hybrid detector concept



JSI
Ljubljana
Slovenia

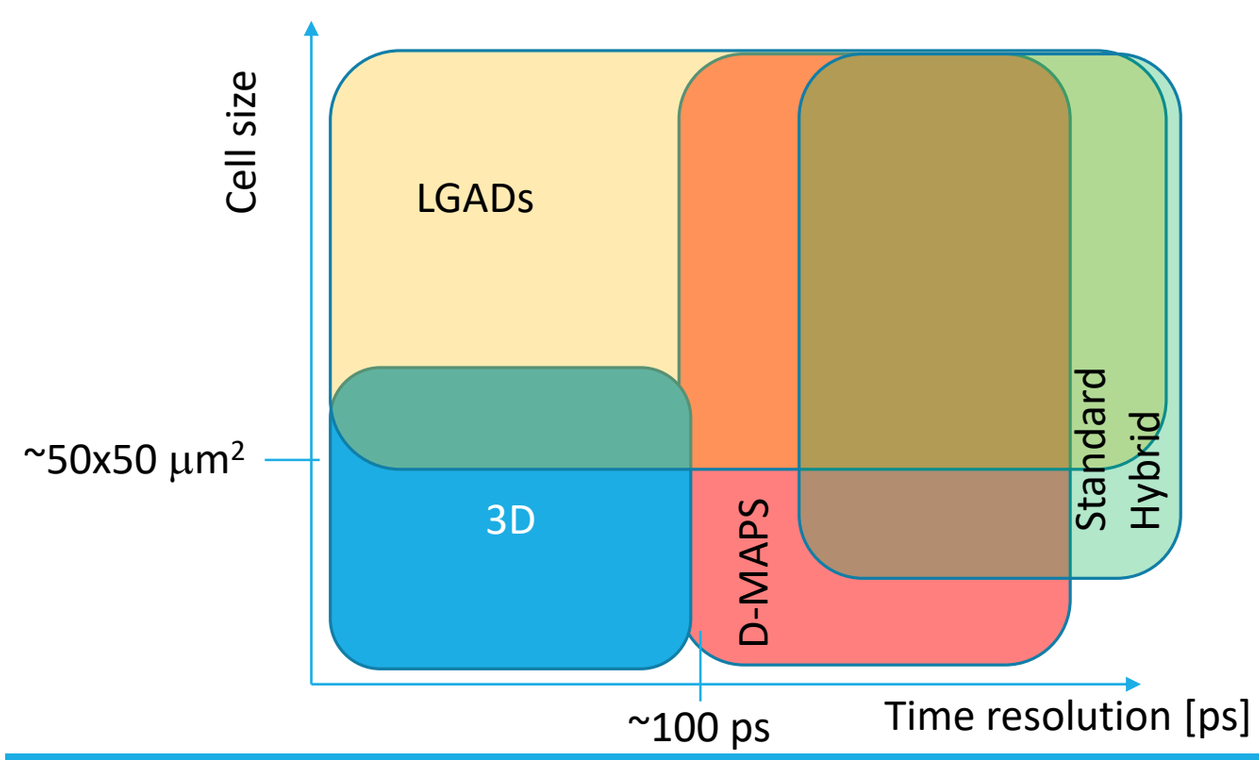
Conclusions

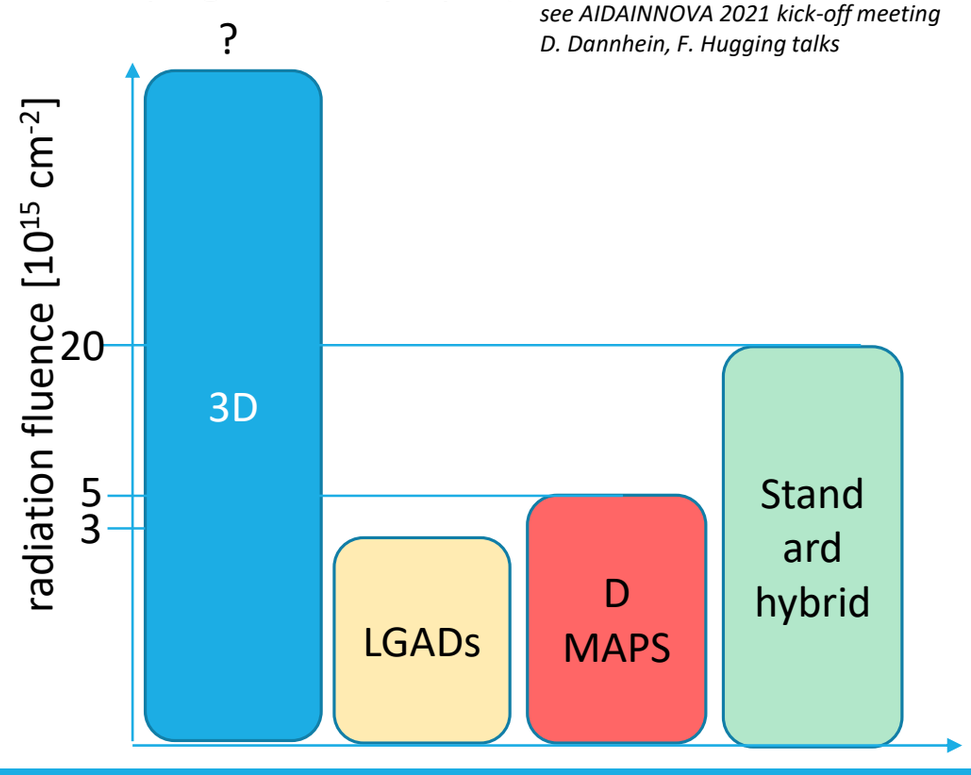
The 3D design developments can lead to sensor solution for 4D tracking where ultimate radiation tolerance accompanied with small pixel size is required. The challenges ahead are very large, but there is no a clear show stopper.

Appropriate ASIC development is likely more challenging in terms of radiation hardness, power consumption connectivity and required functionality per pixel (not to mention cost).

Connectivity of sensors is something that is very important/challenging, but the progress is very rapid (ACF, 3D Wafer-Wafer bonding).

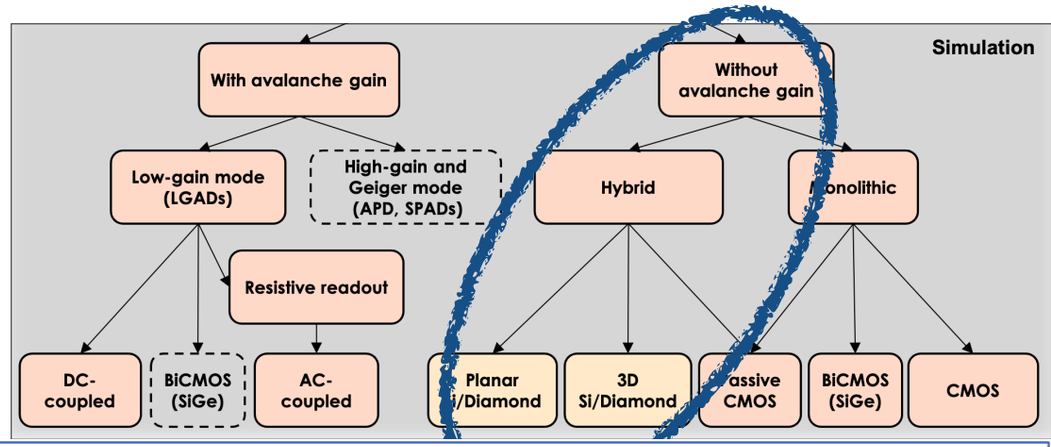
see AIDAINNOVA 2021 kick-off meeting
D. Dannhein, F. Hugging talks





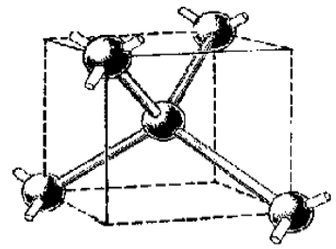
Dimond Det.

Dimond Detector

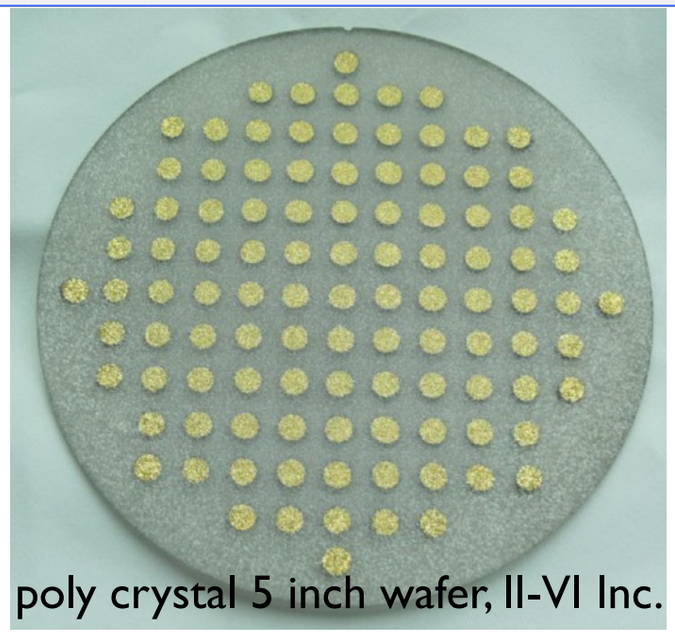


- Research Challenges for the next 20y
- Polycrystalline CVD diamond.
  - Collection distance 25% increase.
  - Decrease price by 50% (happens with larger use as in Si).
- Radiation tolerance.
  - Go to smaller cell size.
  - True 3D field electrodes (internal cages) offer huge potential to optimize electric field distribution to minimize drift time.
  - Also offer possibility of gain in diamond.
- Processing of 3D graphitic wires in diamond.
  - Reduce resistivity.
  - Scale production capability.

Property	Diamond	Silicon
band gap	5.47	1.12
mass density [g/cm^3]	3.5	2.33
dielectric constant	5.7	11.9
resistivity [Ωcm]	>10^{11}	2.3e5
breakdown [kV/cm]	1e3...20e3	300
e mobility [cm^2/Vs]	1700	1400
h mobility [cm^2/Vs]	2100	440
therm. conductivity [W / cm K]	10..20	1.5
radiation length [cm]	12	9.4
Energy to create an eh-pair [eV]	13	3.6
ionisation density MIP [eh/mm]	36	89
ion. dens. of a MIP [eh/ 0.1 ‰ X_0]	450	840



- Low dielectric constant ➔ low capacitance
- Low leakage current ➔ low noise
- Room temperature operation –MIP signal ~2 smaller at same X_0
- Fast signal collection time –Efficiency < 100% (pCVD)


poly crystal 5 inch wafer, II-VI Inc.

Discussions

- Questions for the “facilities” panel
- Beam test facilities: (DESY runs 1~6 GeV electrons with a stable beamline setup)
- Irradiation facilities: (neutron and gamma sources)
- Questions for the Industrialization panel
- Analog: How are we making experiments if HPK stops making sensors? Will Chinese firms save us since no one in Europe does
- Monolithic: Can we make a large experiment without analog detectors? Are monolithics a real step forward? Cons: monolithic actually don’t simplify the design since monolithic readout will never be complex enough ==〉 we will need anyway a second layer of more complex circuitry
- Why do we have a European leadership in sensors R&D but a lack of production capabilities? Involvement of European foundries
    - Up to now, they saw no beneficial returns on their investments. What can we do to change their minds?

Summary

- Hybrid detector with passive sensor has been the norm of HEP. It may still be the option in the lower energy and luminosity experiments.
- MAPS is the new trend. DEPFET@BELLE-II and LGAD@CMS are the closest to us.
- MAPS is attractive to TW community, but we need a team to pursue this. Most of TW physicists are users and doing system. We need expertise on design and layout of CMOS technology.

Silicon at Extreme Fluences
Summary

- Measurements performed on Si detectors irradiated to extreme fluences
  - Neutrons from 10^{15} to 4.6x10^{17} n_{eq}/cm^2 , PS protons from 5x10^{14} to 3x10^{16} p/cm^2
  - Velocity vs. electric field impact observed and interpreted as reduction of zero field mobility
    - Zero field mobility follows power law with $|a| \leq 1$, $\Phi_{½} \approx 10^{16}$ n/cm^2
    - Protons degrade mobility more than neutrons
    - Induces resistivity increase in-line with measured *I-V*
    - Exhibits adverse effect on charge multiplication !
  - Simple field profile for very high neutron fluences
    - Diminishing SCR and highly resistive ENB
    - Effective acceptor introduction rates reduced by factor ~100 wrt low fluences
    - Current much lower than anticipated. Generated in SCR only ? Ohmic at highest fluences…
  - Trapping estimates for very high neutron fluences
    - from charge collection in FW and reverse bias
    - from waveforms
    - All estimates point to severe non-linearity of trapping with fluence, 10x lower at 10^{17}
    - Trapping appears independent of electric field
- Conclusion: ***Low fluence extrapolations do not work at all !***

… go out and ***measure*** to get anything working at ***extreme*** fluences !!!

Technology Computer-Aided Design (TCAD)

- Understand and design sensors that meet specific requirements

Universität Hamburg
DER FORSCHUNG | DER LEHRE | DER BILDUNG

CONCLUSIONS

TCAD:

- TCAD is an essential tool for the development of new detectors. The long term access to TCAD (in this case Synopsys) tools through Europractice or similar frames is essential (similar for TF7)
- Cooperation with software providers needed to add certain new features in TCAD
- Community wide data availability for the development and validation of radiation damage models.
  - Data from test structures to disentangle different effects

Signal simulation tools:

- Large number of individually maintained tools. The community could benefit from fewer but well maintained and supported detector simulation packages.
- Implement empirical models which are accurate but does not degrade the runtime
- Validation data and reference data for new algorithms (beam tests, data preservation)

Displacement damage simulation:

- Simulation chain can be build with open-source code
- Requires good set of reliable experimental data

Thank you for your attention!