Electronics (Taskforce 7)

Main subjects:

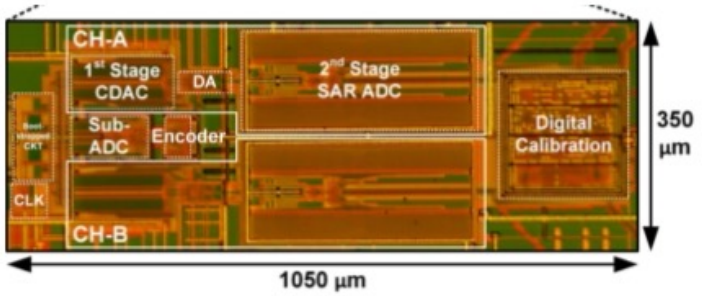
- **On-detector ASICs**
- **Links, powering and interconnects**
- **Trigger and DAQ systems**

ASICs in HEP

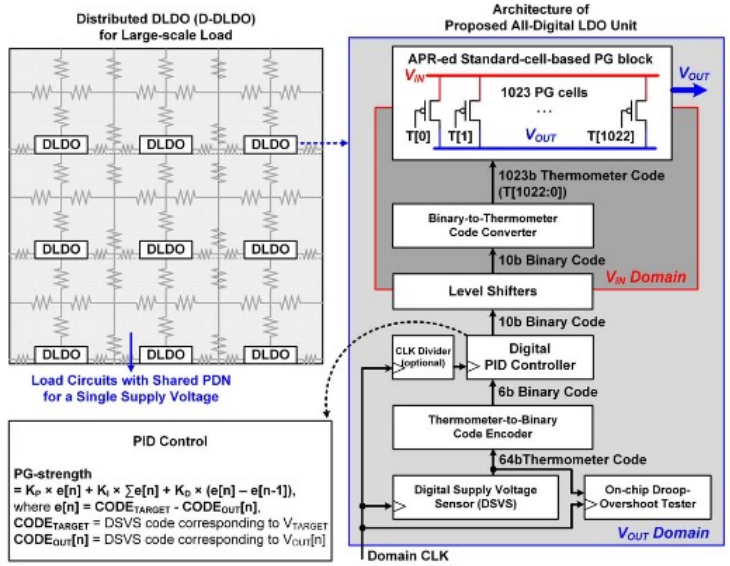
- We need ASICs mostly for front-end, power management, data transmission;
- High resolution timing is becoming a must for many detectors;
- Finer granularity (but not so extreme), less power
- In (inner) layers of hadron colliders, life is complicated by radiation damage, which imposes lengthy technology testing procedure;
- We are adding cold ASICs to the menu;
- Production volumes are, at best, very modest compared to industry standard;
- HEP ASICs are very specific systems fabricated in mainstream technologies built out of very common critical blocks (ADCs, TDCs, PLLs, DLLs, Power converters, ser-des, etc..)

Some key components in non-HEP world that we can adapt:

1. ADC:
    1. Design based on 7nm FinFET exist. But not really necessary, 28nm technology is good enough.
    2. Typically with few hundred MS/s rate, 12-14 bits.
    3. Core size of ~ 0.01-0.5 mm^2. Single side dimension ~130nm.
    4. < 10mW.
    5. Big advances due to SAR (Successive-approximation-register) architecture.

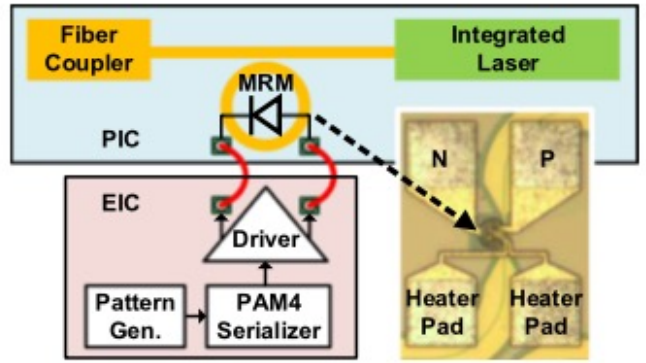


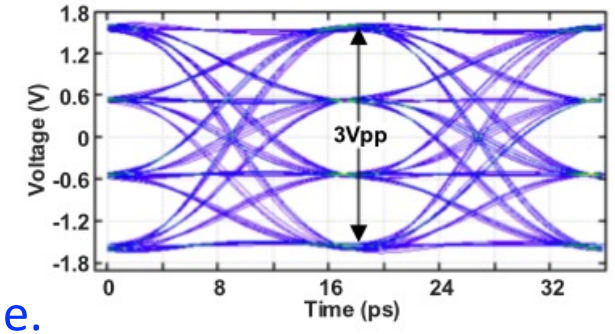
2. LDO (Linear Regulator):
    1. Distributed power management.
    2. Analog function designed with digital approach
    3. On chip DC-DC converters



3. Data transmission

1. 100 Gb/s Silicon photonic transmission
2. With multi-level digital signal (PAM4).
3. 28nm technology

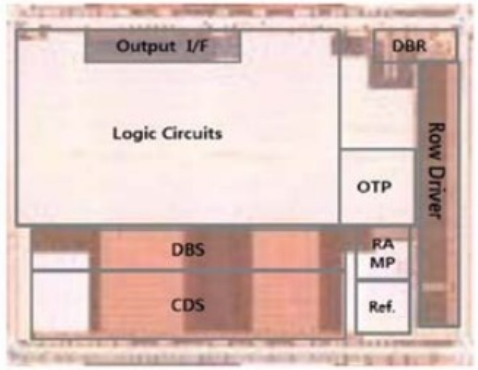


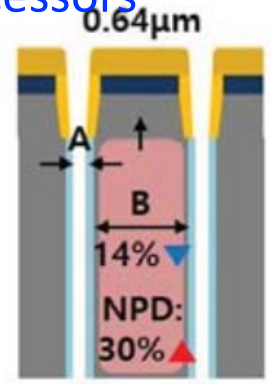


4. TDC

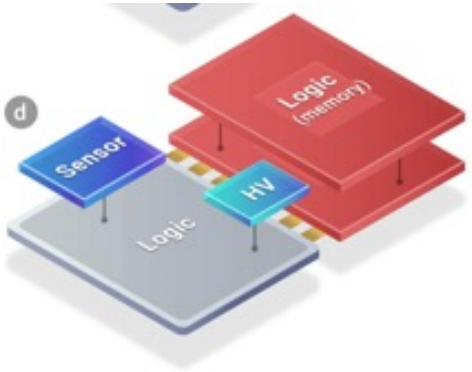
1. < 1V supply voltage
2. ~ 1 ps resolution ➔ precision limit on the detector side.
3. 65 nm technology
4. Few mW power
5. 0.1 mm^2 area.
6. Plenty of different architecture, no problem to adapt.

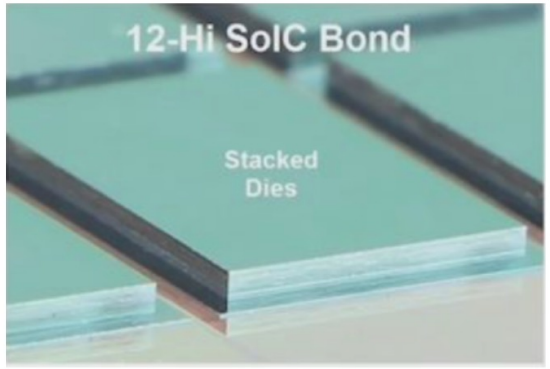
5. High density pixel: (from mobile phone camara industry)
    1. <1 μm CMOS pixel
    2. ~ 1 e^- random noise
    3. Requires 3D packaging to interconnect to processors

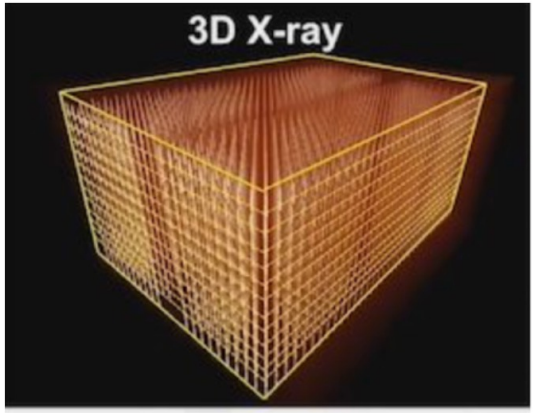




6. 3D integration technology:
    - Moore laws may continue due to 3D integration and new devices.
    - TSMC SoIC microbonds reaches 10^6 bonds/mm^2



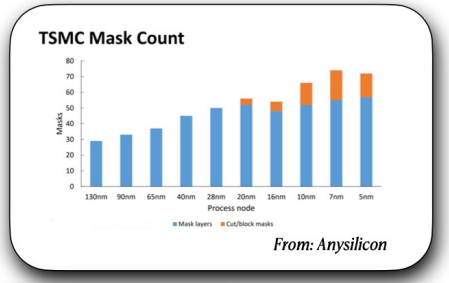


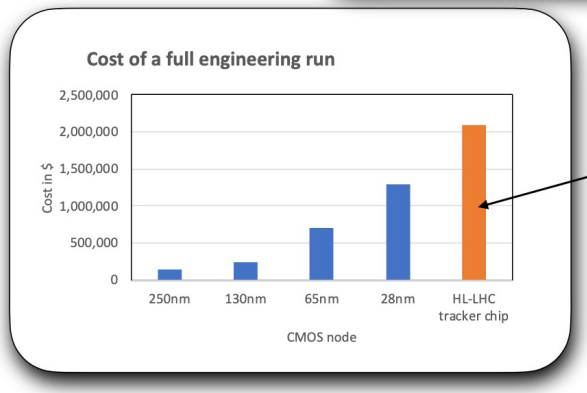


Making a detector out of this?

- The negative side of these new developments is the cost, manpower, more complex development cycle, software.

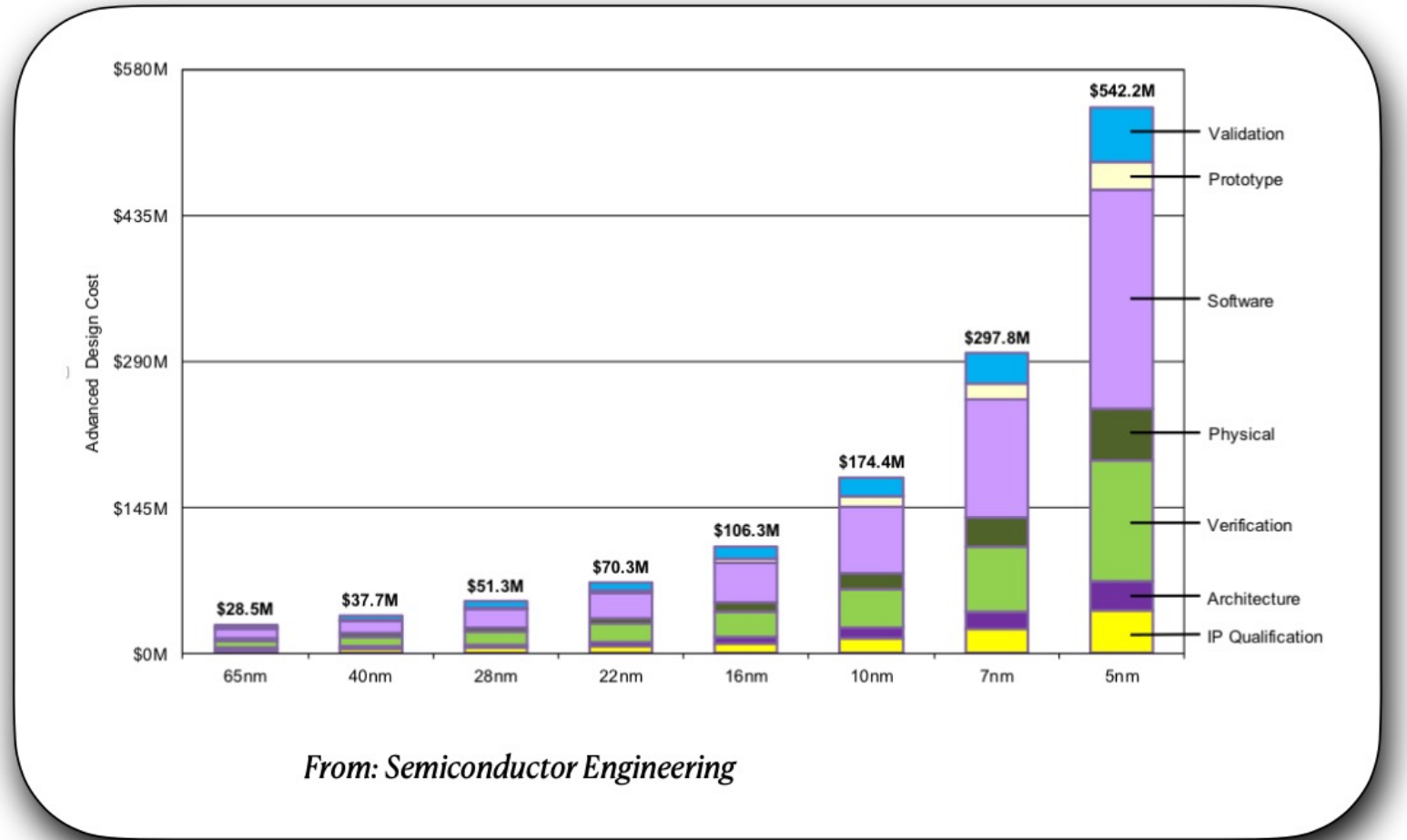
The increasing complexity in silicon manufacturing is expensive for low-volume ASICs





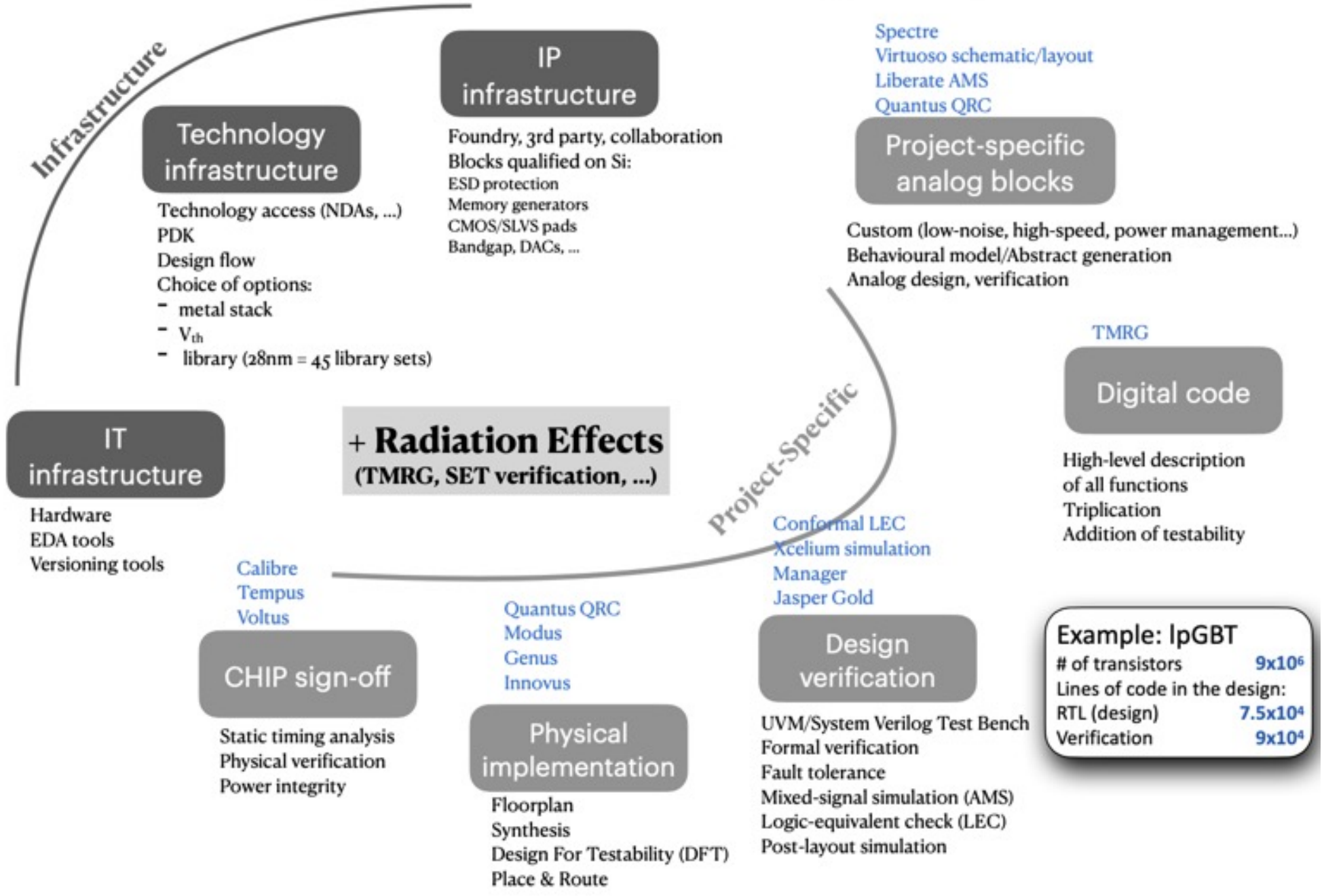
- But technology can coexist:
  - Two order of magnitudes in transistor gate length (and price): from 0.7 um (300 euro/mm^2) to 12 nm (26000 euro/mm^2)
- And Open source gradually emerge.

Silicon is not the only expensive item:
IC development requires trained people and advanced software



From: Semiconductor Engineering

The round of competences/toolsets needed to design a complex ASIC



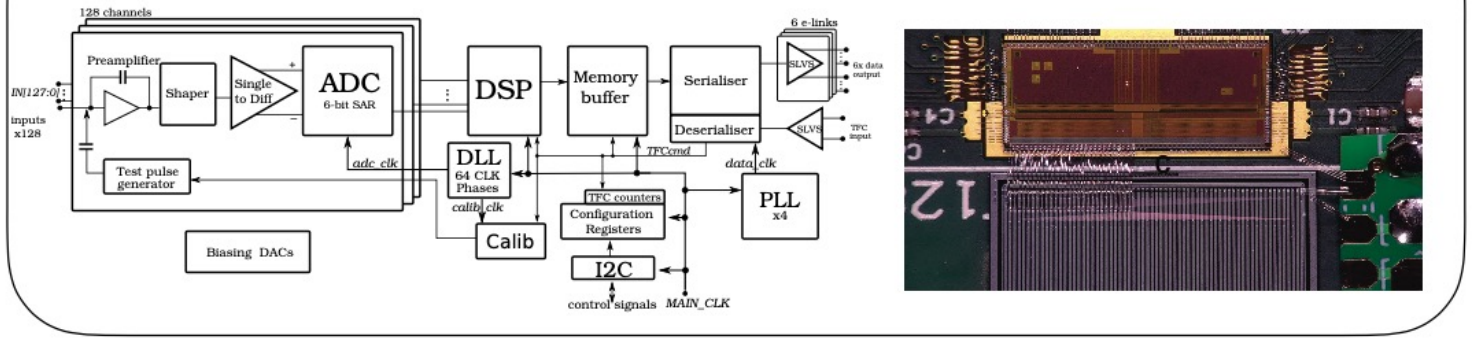
Wrap up on the available technology:

- Much more technology available than we can explore.
- Choose a technology is always a bet.
- No particular concern on performance achievable for key IP blocks.
- What you buy is density, speed and power.
- Key issue is to have enough engineers to work out the best to our needs.
- Not be in a hurry. What do you want to do with a chip with 20M transistor at a cost of 200k euros

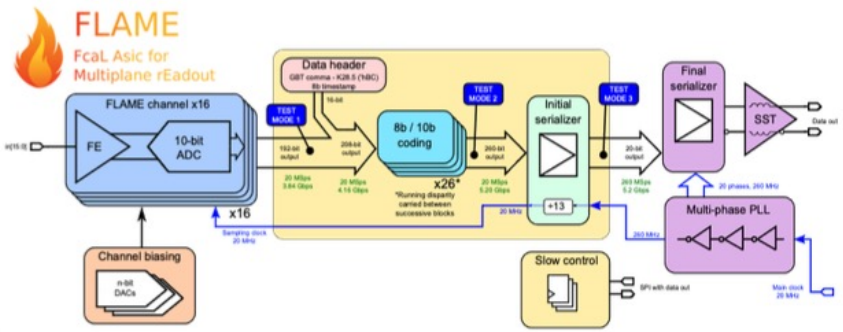
ASIC Developments within HEP

Present/near term

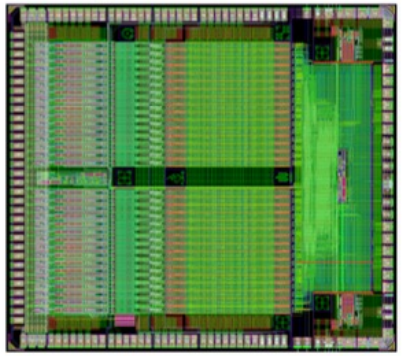
SALT: 128 ch. ASIC for strip readout in LHCb - M. Idzik, TWEPP 2019



FLAME for LumiCal



FLAME layout: the size is 3.7mm x 4.3mm



Trend:

- Include also TDC for timing
- Higher resolution, flexible ADCs
- Full fledge on board DSP
- High granularity on board power management

Question:

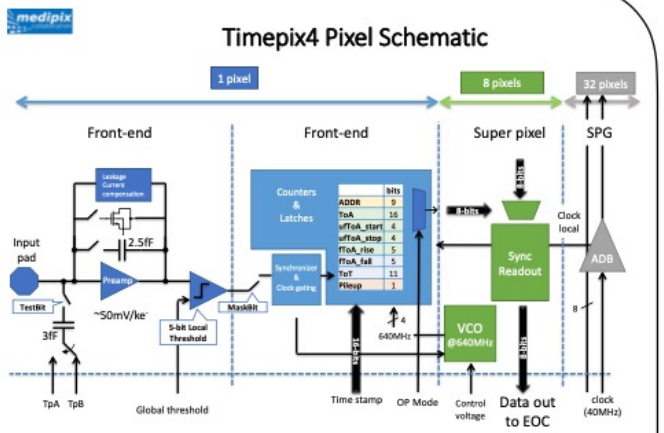
How much intelligence do we need on chip?

- Exact partitioning between on-board and off-detector signal processing may be determine with detailed detector studies.

Hybrid Pixel detector:

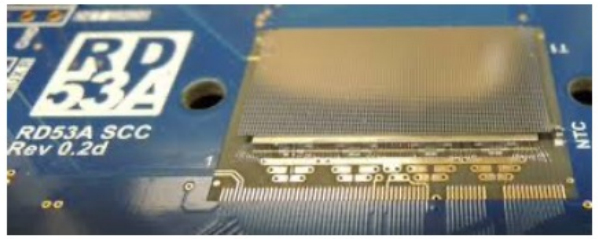
Present/near term

TimePix4



- Time resolution 200 ps
- 55 micron pixel pitch
- 4 sides buttable with TSV
- 3.5 MHit/mm²/s
- 65 nm CMOS

RD53 series



- Common baseline development
- Final chips customised in some details
- 50 x 50 um pixels
- > 1 GHz/cm2
- 65 nm CMOS

Trend:

- Reduce Pixel size towards 25um x 25um for FCC-hh
- Move to more scaled technology: 28nm?
- High time resolution per pixel (<100ps)
- New interconnection technology
- More processing on chip.

Summary on ASICs:

- Requirements in ASICs rather clear even for far future.
- In terms of technology, only FCC-hh inner detector is a problematic case – radiation.
- For the rest, it is mostly a question of budget.
- Need to profit more by latest advanced CAD tools, which have been tuned for more complex chips than we need.
- Collaboration rather than competition (avoid “parallel development”, multilateral funding)
- Include realistic ASIC description in detector simulation.
- Open IP
- Need a team of ASIC with different sizes.

Part B: Links, powering and interconnects

Links:

- Radiation-hard optical links
- Silicon photonics
- Co-packaging electronics and optics components
- Wireless links.

Powering

- Power distribution.
- All stages of DC-DC converters (input stage with large conversion ratio and on-chip power management
- Availability of powering know-how and technologies (for DC-DC and serial powering)
- GaN technology
- Power over data links.

Interconnect:

- Advanced packaging solution and high density interconnects
- Scaling to large-size stitched and tied assemblies
- Cooling technologies for very high-density electronics

In general, pay attention to extreme radiation and noisy environments

Power and links has conflicting requirements

1. Power and links takes up a lot of weight and service volume
   - Reduce power with new technology, but increased number of channels at the same time.
   - Reduce data volume by frontend intelligence, but possible higher power and increased complexity
   - Optics is good, but difficult to avoid electrical interconnections

2. Example:

HL-LHC pixel detetors:

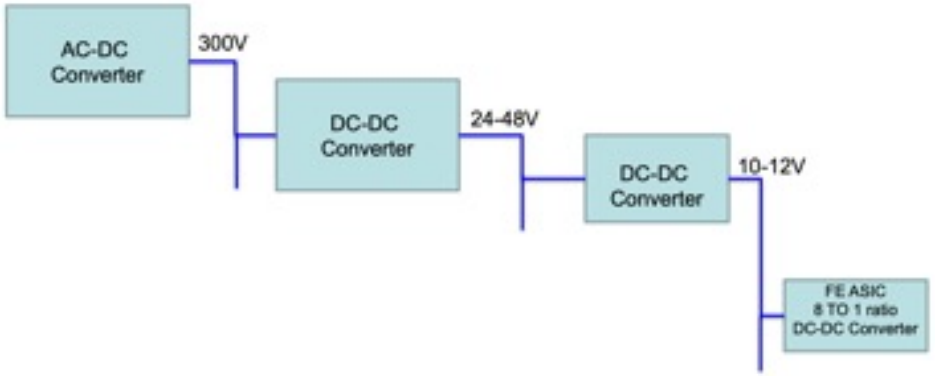
1. Power: ~7000 W/m^2
2. Links capacity: ~3000 Gbps/m^2.

HL-LHC outer tracker

1. Power: ~450 W/m^2
2. Links Capacity: 100 (600) Gbps/m^2

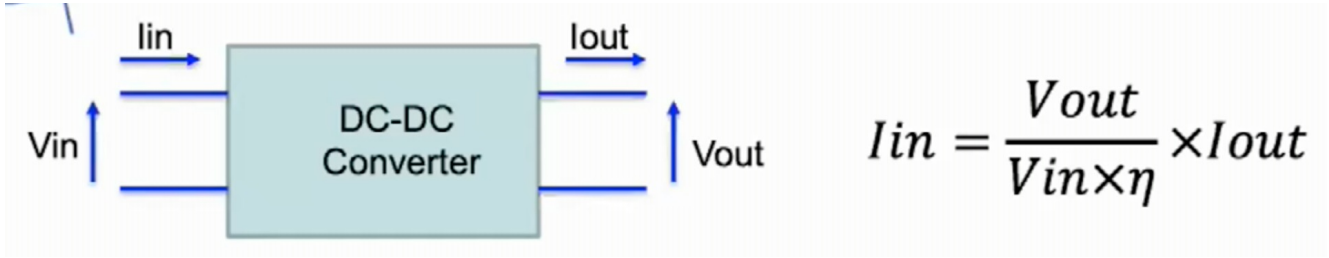
Future trend:

- More channels with additional information (e.g. timing)
- Should limit the power increase despite higher performance
- However, will need high current to the FE because Vdd decreases



R&D :

1. DC-DC converter: Larger V_{in} to the last point of load (POL) converter.

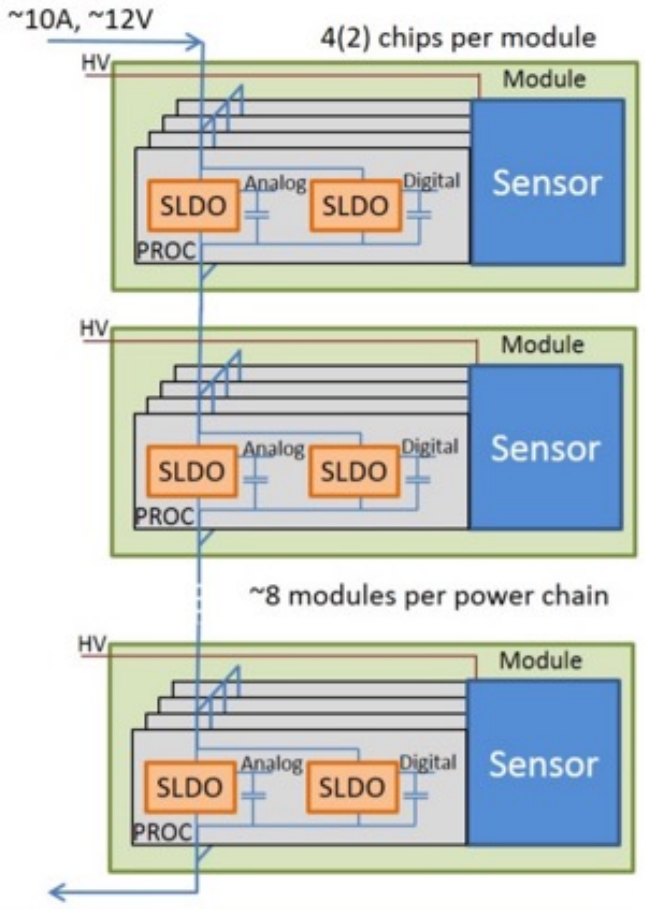


$$Iin = \frac{Vout}{Vin \times \eta} \times Iout$$

2. Last stage of conversion in the FE ASIC itself (to reduce material budget)
   - R&D on on-chip conversion with 8 to 1 voltage ratio.

3. Serial powering: up to 10-14 modules / chain

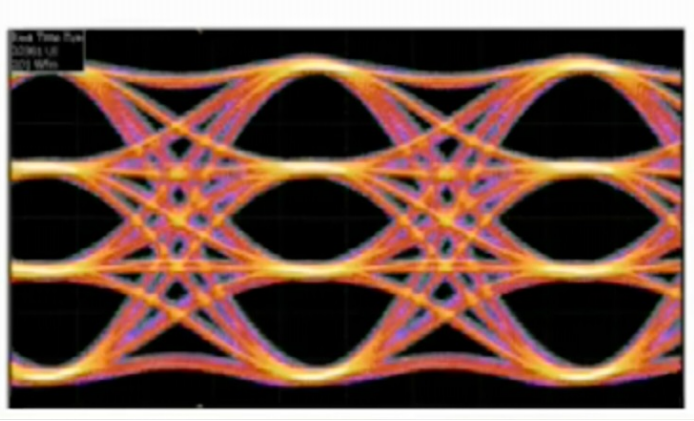
4. Pulsed power for colliders with large time gap between bunches.
5. ?? Power over fiber/ wireless power



Front-end Links:

Trend:

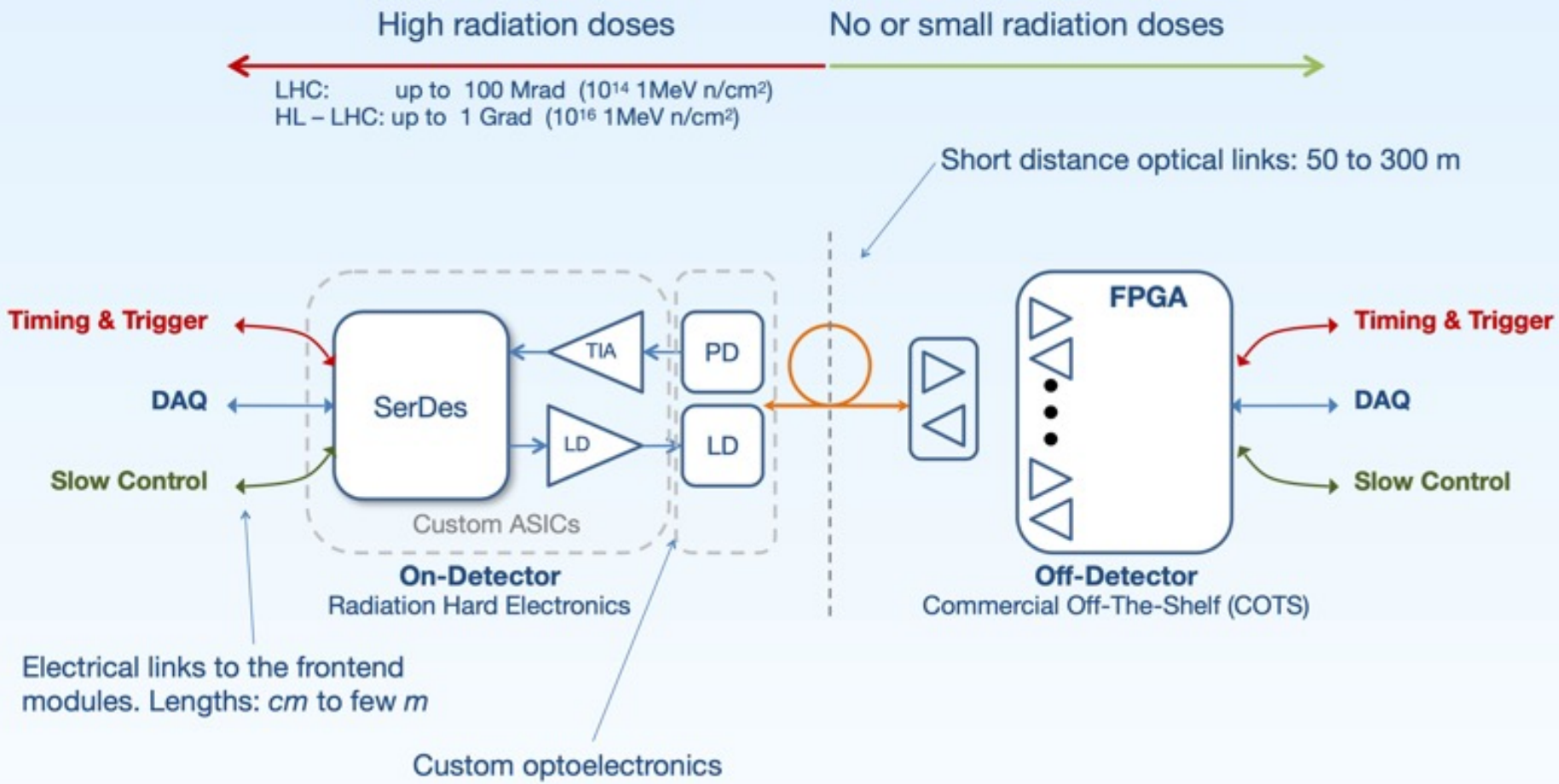
- Amount of data certainly increase
- May implement intelligence in FE ASICs, but
  - Increase power
  - Radiation induced errors
- Need to reduce size, power, voltage,



R&D

- Simplest: PAM-4 links: Need to be compatible with back-end COTS
- Silicon photonics: optical signals directly on FE
  - Benefits obvious (lower power, higher rates, small volume. Up to 25Gps/s today.
  - Also need to be compatible with COTS
- Faster optical links over copper:
  - Via low mass tape, but currently transmission quality not good.
- Wireless transmission.
  - Hard to go far in a dense detector (acting like a Faraday cage).
  - A few ten's cm wireless from pixel module to opto-device located a bit further could make sense.
- TTC (Tracking, telemetry, control) links:
  - Network to distribute timing signal to ~10ps, may need improvements.
  - May need large network to broadcast information to ever larger detector

HEP Link paradigm



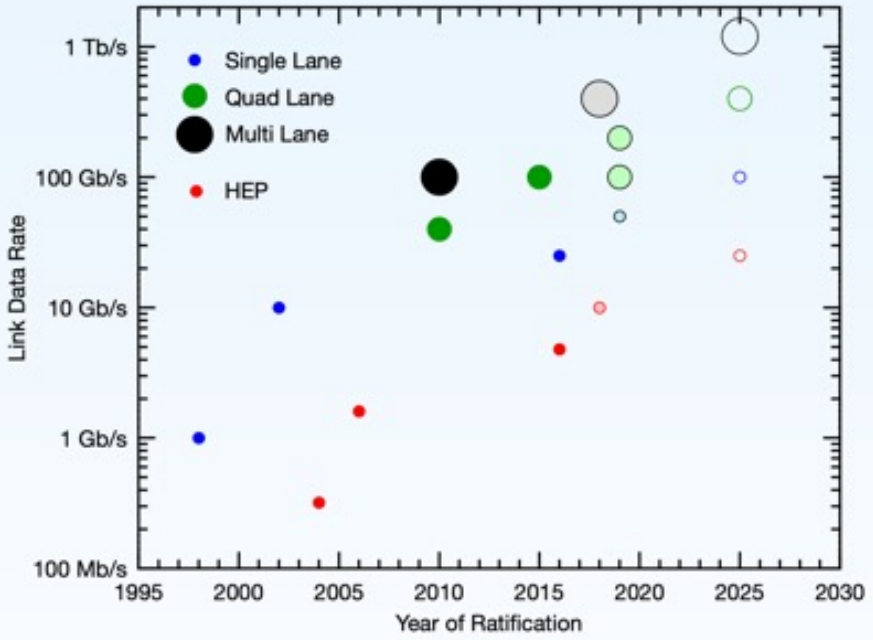
- Aggregate Data to exploit fibre bandwidth
- Custom front-end components interoperate with COTS for back-end

Speaker's Summary:

- Higher power and higher data volume to be readout
- Radiation ($10^{15}/cm^2$) and magnetic field to be assumed
- Needed developments for powering front-end
  - DC-DC converters with high input voltage (24 – 48 V)
  - Last stage of DC-DC in the front-end ASICs
    - Drop-inblocks
  - Increased compactness
- Needed developments for front-end links
  - Faster and more "integrated" optical links
    - Silicon Photonic seems the best choice
  - Faster SERDES to drive them
  - SERDES, line drivers, equalizers blocks for fast copper links

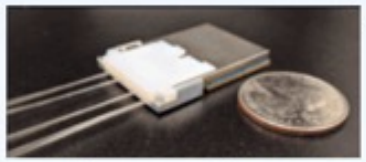
Silicon photonics

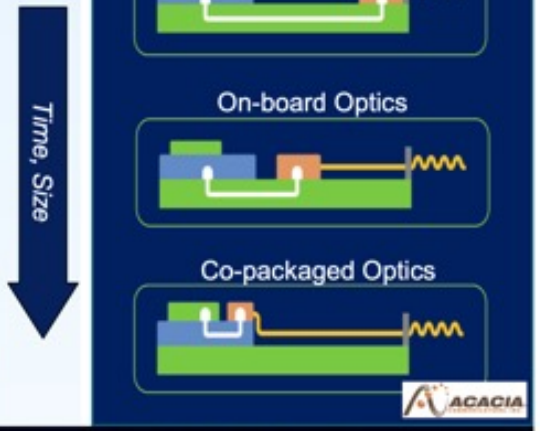
- If we want to interoperate with COTS components, instructive to see where things are heading
  - Speed and level of integration



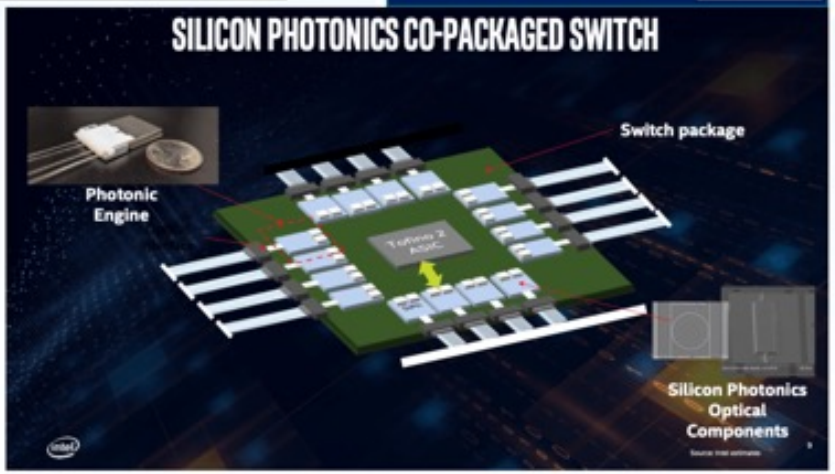
SerDes Speeds

Gb/s	10	28	56	112	256
	NRZ	*NRZ*	*PAM4*	*PAM4*	*PAM4*
				Now	***+2-3 yrs***





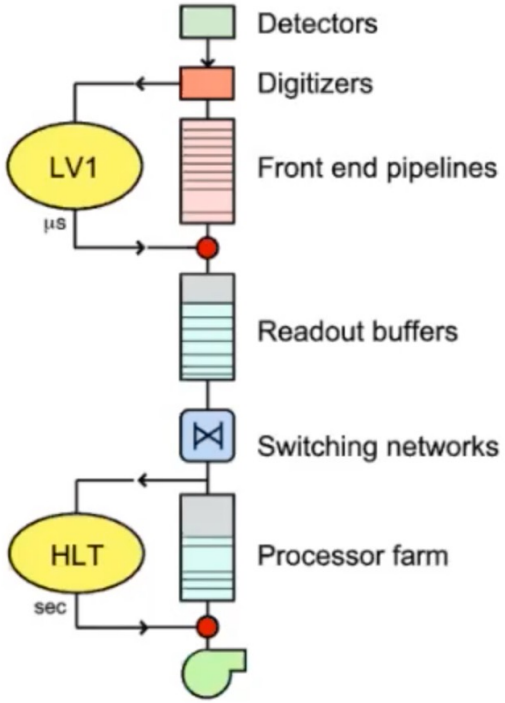
Time, Size



DAQ and Trigger

The focus is at whether we need to go to Triggerless DAQ, with as much as possible COTS networking.

- LHCb is doing it now.
- Still many unresolved problem in other detectors
- A debate on whether this is desired.



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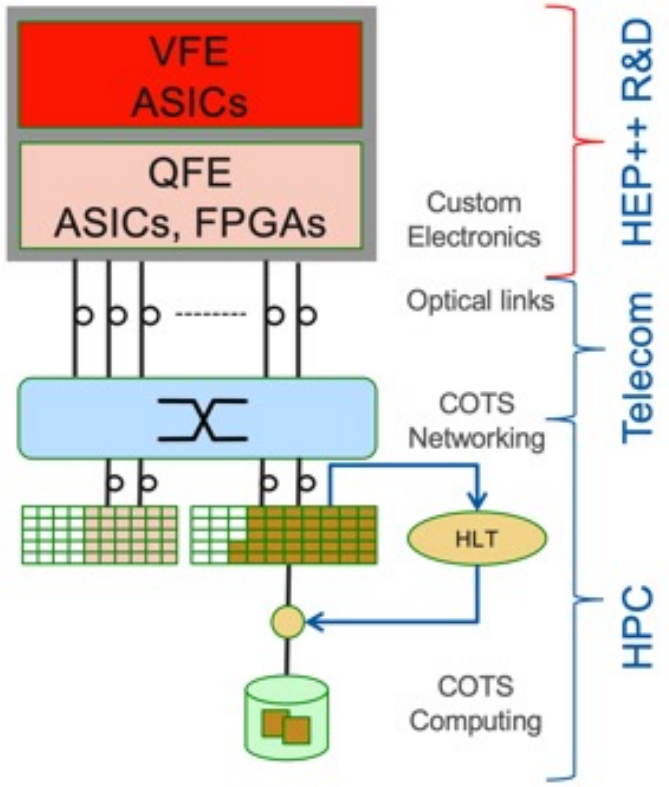
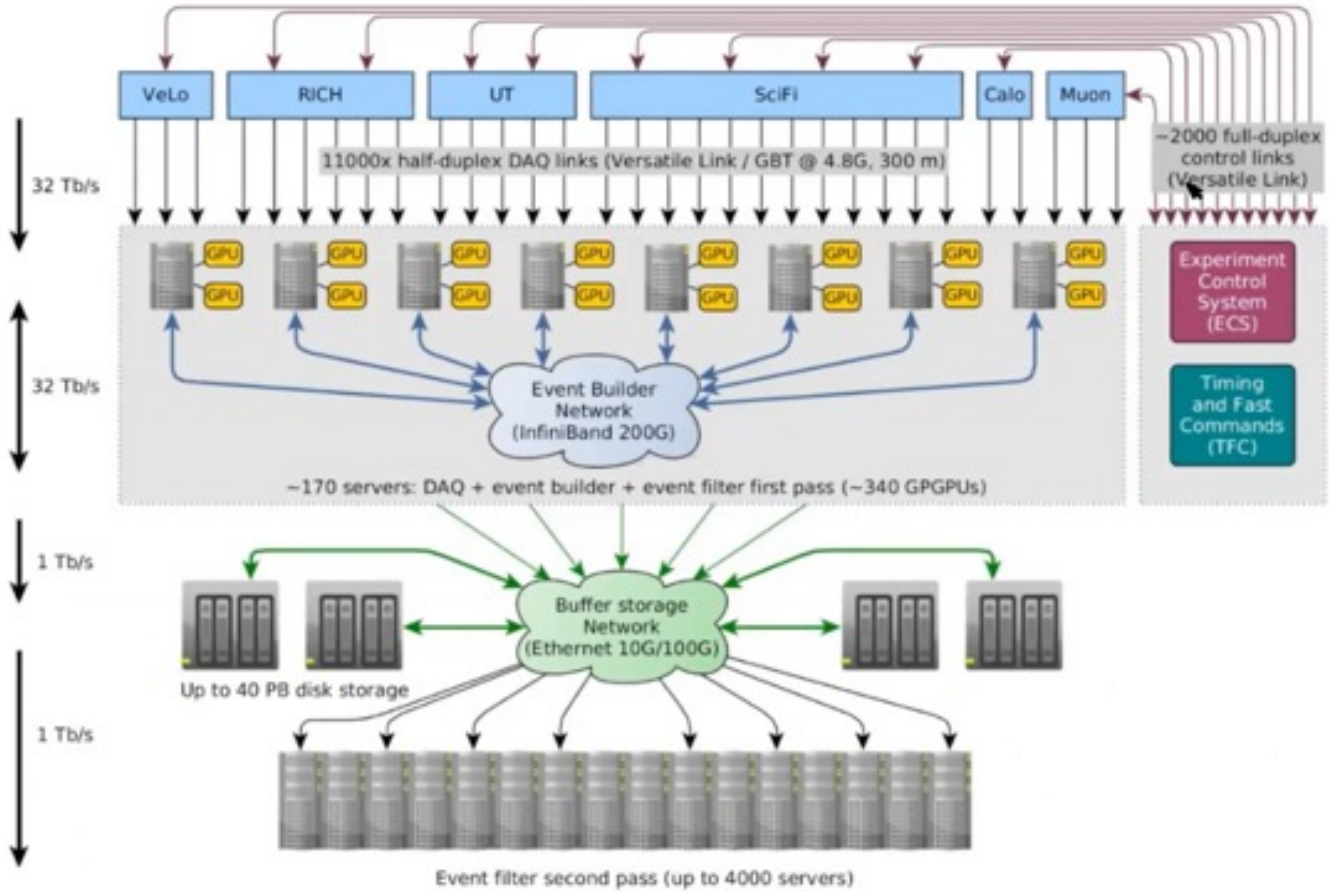


LHCb: A case study

- This is a challenge LHCb faces now (Run 3)
- Data rate reduction prior to event building would be no better than a prescale.
- Instead: Read-out and build events at 30 MHz



- Symmetric event building network is COTS (infiniband).
- EB nodes are low-cost COTS servers

The other extreme is to “Move the intelligence to the detector”

- On-chip algorithm
- AI-on-sensor
- Small data volume to send out
- Much lower processing requirement for upper stage.

- Lost the raw information, simulation has to include ASIC functionality
- Radiation induced error
- With high rate data links, this is not necessary

A word about TSMC

There was a (somewhat long) discussion about how to approach TSMC. Everybody is bothered by the legal issues and the accessibility of TSMC CAD design. Cost is a problem, and the HEP community is not viewed as a single legal entity, so every one need to pay to get access.

TSMC is not paying attentions to HEP, because of too small in quantity.

Can we demonstrate to TSMC that our work has industry mass production application?

TSMS is being criticized a lot! But TSMC seems to be the only large foundry that is capable of <28nm process, and willing to talk at least.

Not seriously discussed in this symposium:

1. Radiation issues.
2. Electronics for non-accelerator experiments.
3. Cold electronics. (Extremely low noise).