Development of DAQ system of ZDC-ECAL and AC-LGAD

Kai-Yu Cheng

Outline

1st & 2nd ZDC ECAL prototype

- GTM DAQ system
- CITIROC 1A ASIC
- DAQ system with multi-GTM readout boards

H2GCROC

- H2GCROC / HGCROC
- H2GCROC DAQ

AC-LGAD for EIC TOF

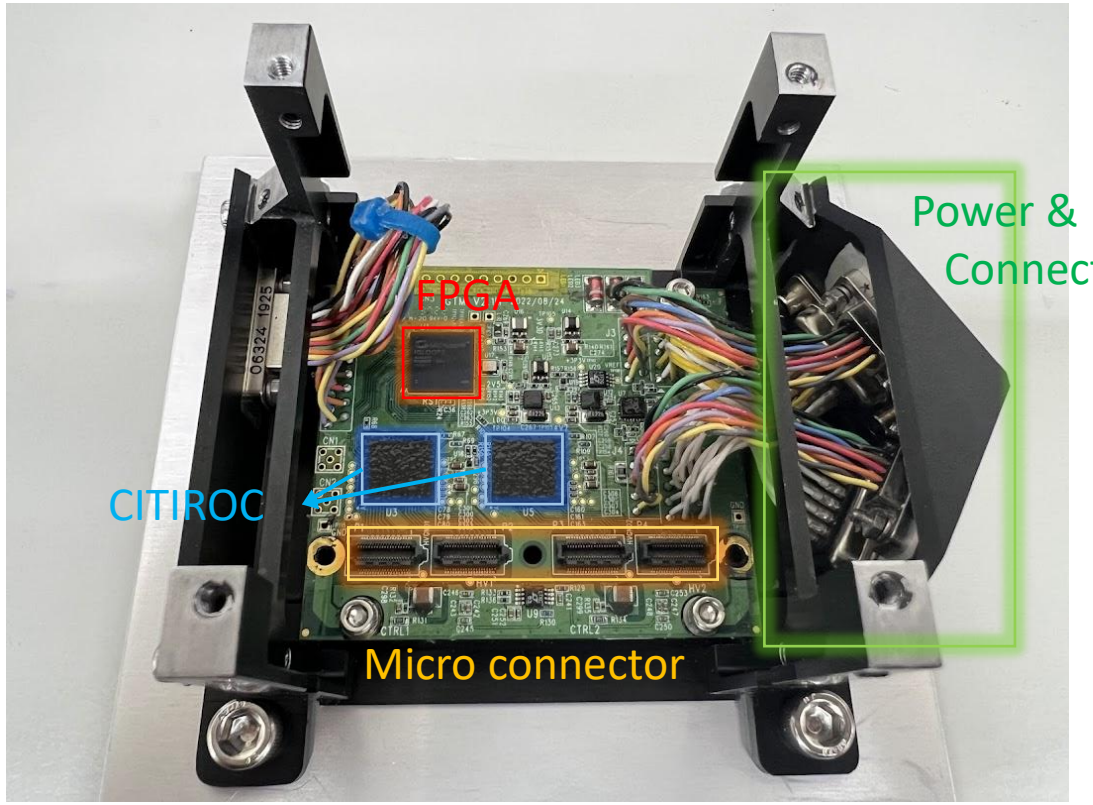
- The development progress of the EIC AC-LGAD
- The process progress of the AC-LGAD in Taiwan

GTM Readout Board

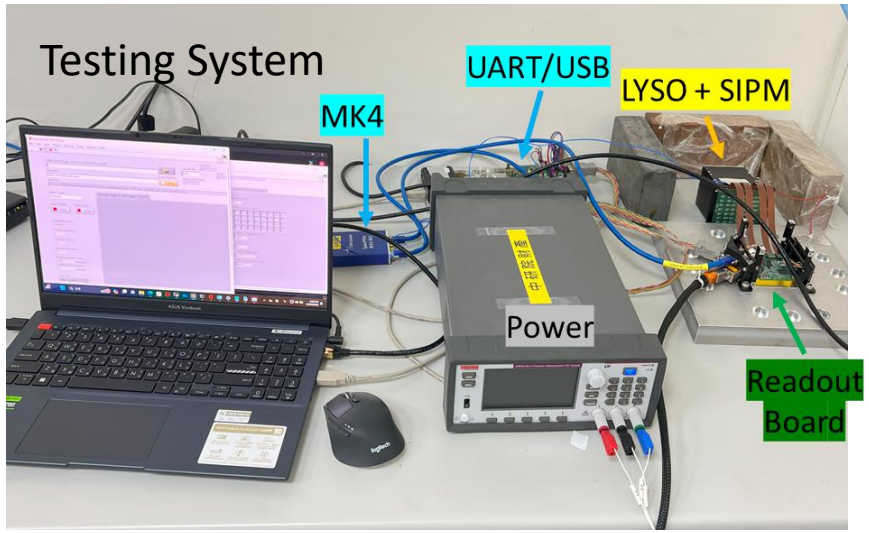
Gamma-ray Transients Monitor (GTM)

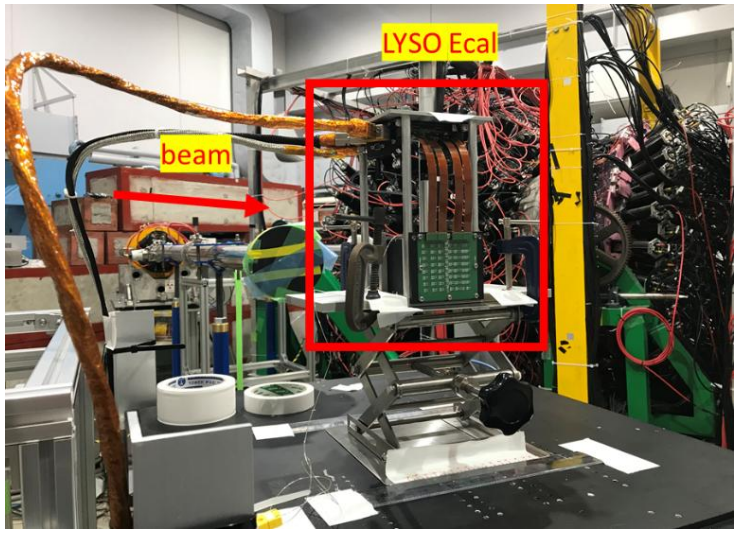
The SiPM array readout system for gamma-ray detector in other space experiment. It includes :

- FPGA chip
- 2 x CITIROC 1A ASIC = 2 x 32 channels
- 2 x High-voltage convertor for bias of SiPM
- Samtec Micro Blade & Beam connectors for SiPM interface (16 channels + HV + GND)
- SpaceWire data interface
- Self-Trigger mode
- Maximum taking rate : 40k Hz

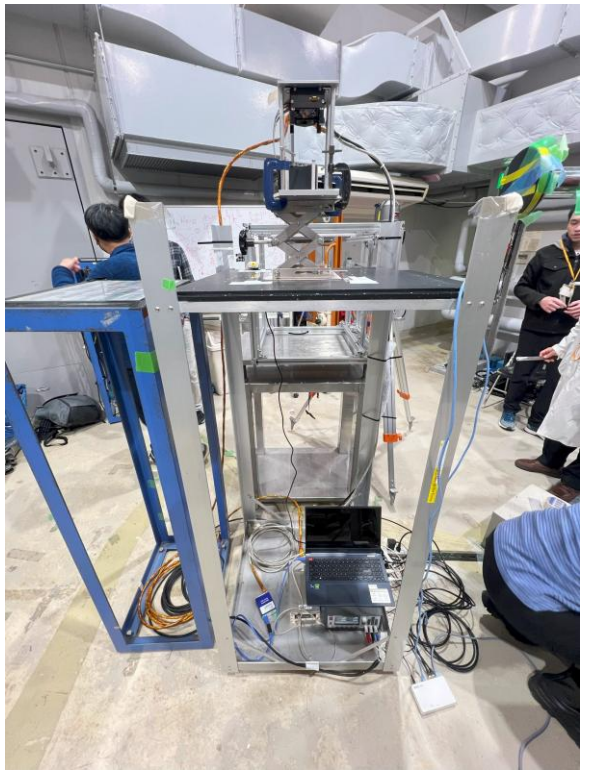


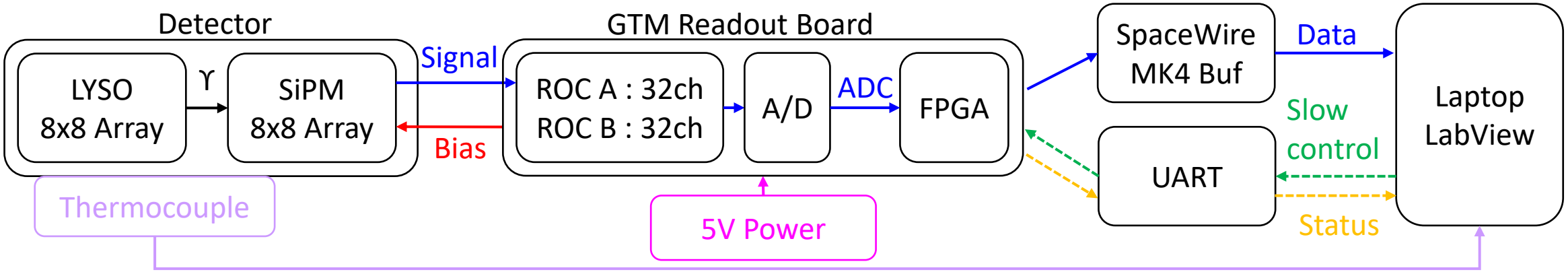
Setup of 1st ZDC ECAL Prototype





Setup @ ELPH





CITIROC 1A

- Dynamic Range : 160fC – 400pC (1-2500 photo-electrons @ 10^6 SiPM)
- Adjustable-voltage (0-4V, 8-bits) signal input port
  - ➢ Provides per-channel voltage adjustment for correcting SiPM gain.
- SiPM signals will be covered to voltage source

$$V_{SiPM} = V_{HV} - V_{DAC}$$

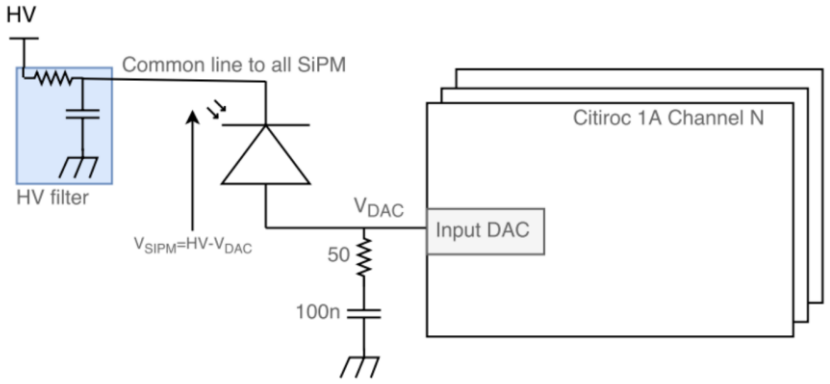


Figure 22 - SiPM connection scheme - DC bias

CITIROC 1A

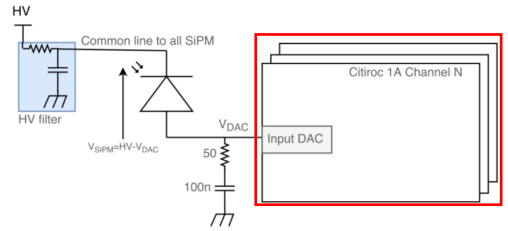


Figure 22 – SiPM connection scheme – DC bias

- High-Gain & Low-Gain pre-Amp
  - LG ratio : x1 ~ x60
  - HG ratio : x10 ~ x600
  - The HG mode provides finer resolution but a narrower dynamic range.

- Then, signal is split into two paths:
  - Fast shaper for trigger generation
  - Slow shaper for accurate signal readout (peaking time adjustable from 12.5 ns to 87.5 ns in 12.5 ns steps)

- CITIROC automatically selects gain mode based on the signal's dynamic range, or can be set to use the low-gain mode only.

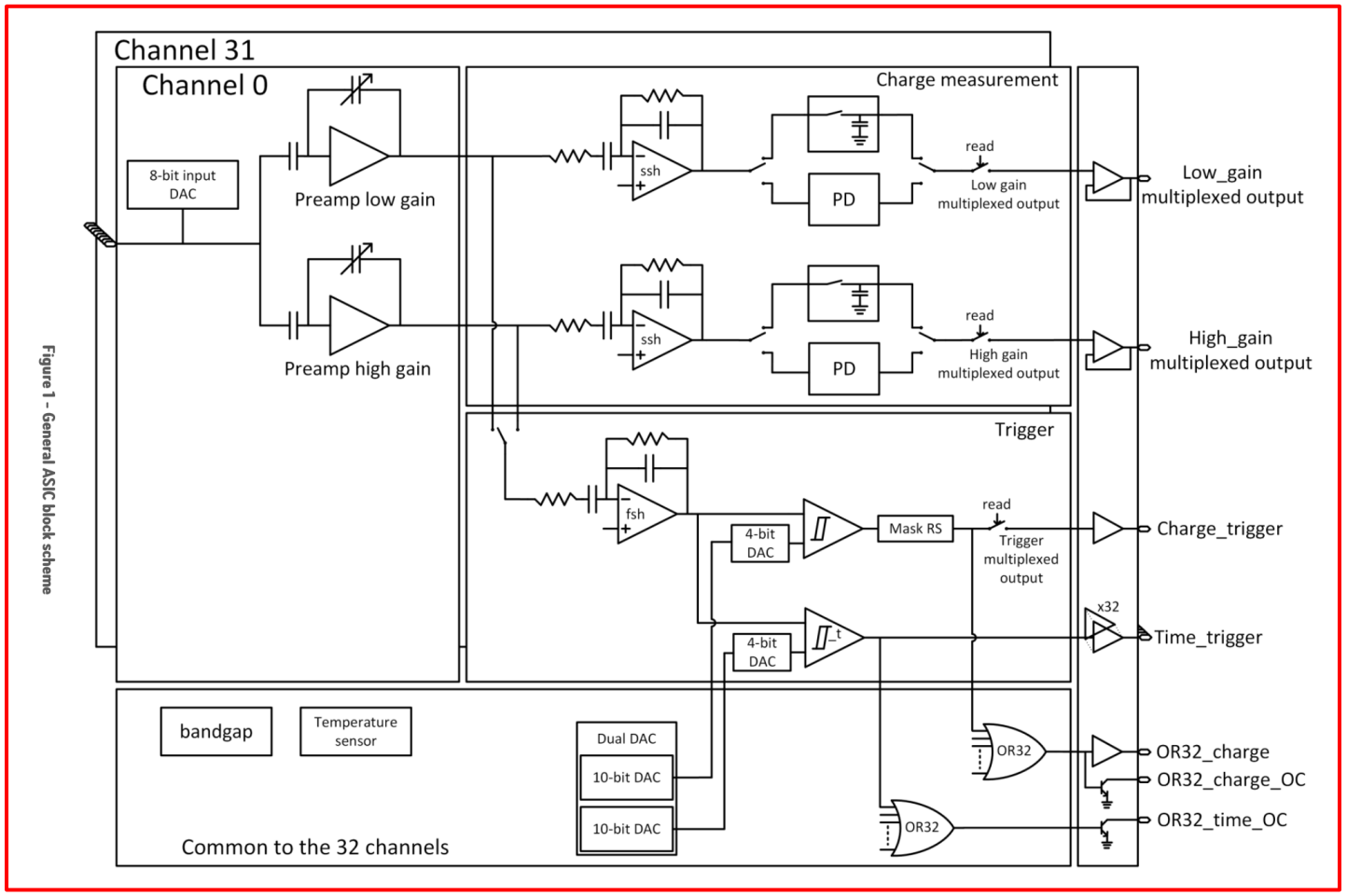


Figure 1 – General ASIC block scheme

Peak Detector

- Slow shaper + peak detector → CITIROC measures peak value, not charge integration.
- Trigger from fast shaper → CITIROC enters peak search to capture the slow shaper peak.
- After peak search, a hold signal is activated to latch the peak value and prevent changes from later signals until all channels are read.
- CITIROC can be configured to read out **only the triggered channels** or **all channels**.
- The peak signal output from CITIROC is sent to an A/D converter, where it is digitized into a 14-bit ADC value.

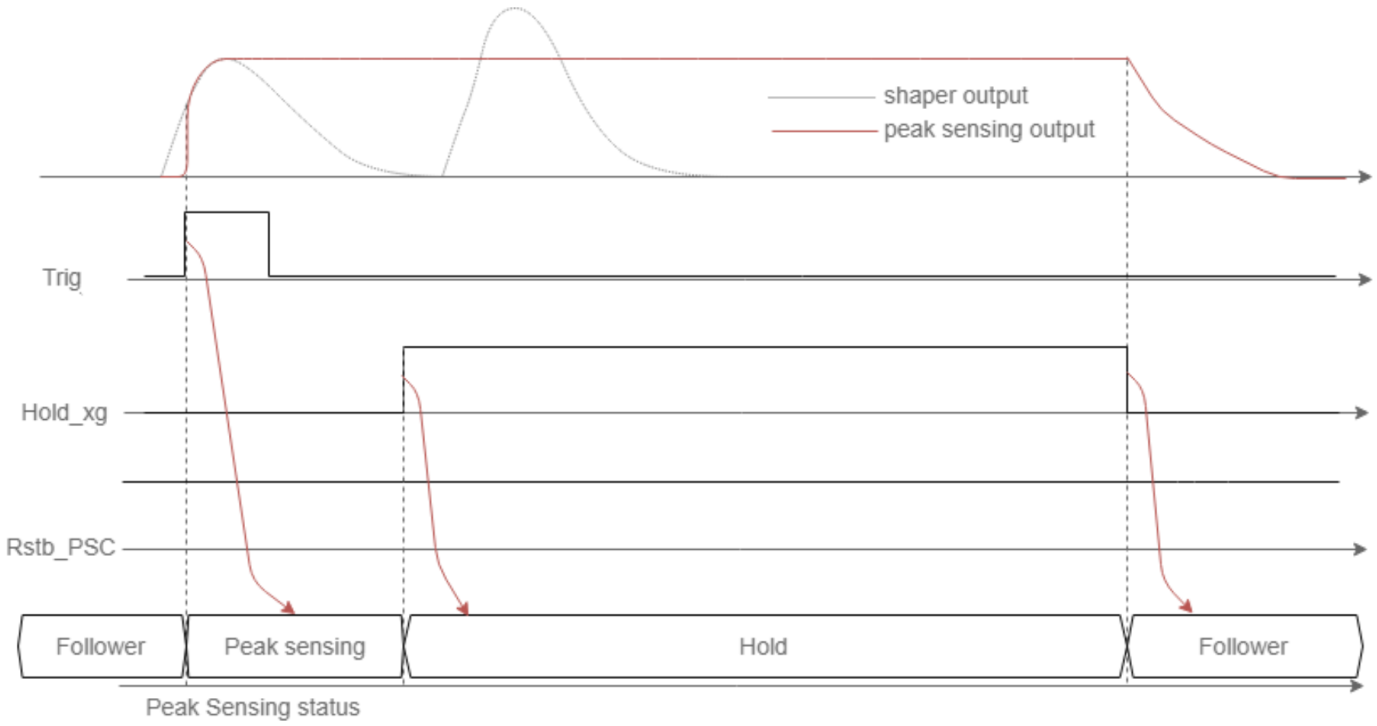
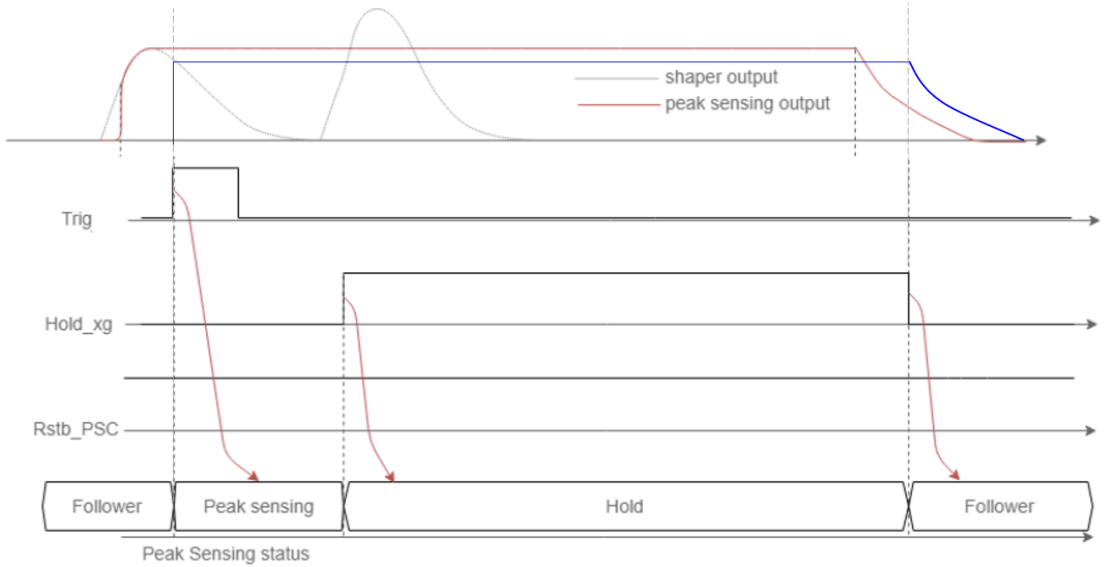


Figure 14 - Peak detector chronogram

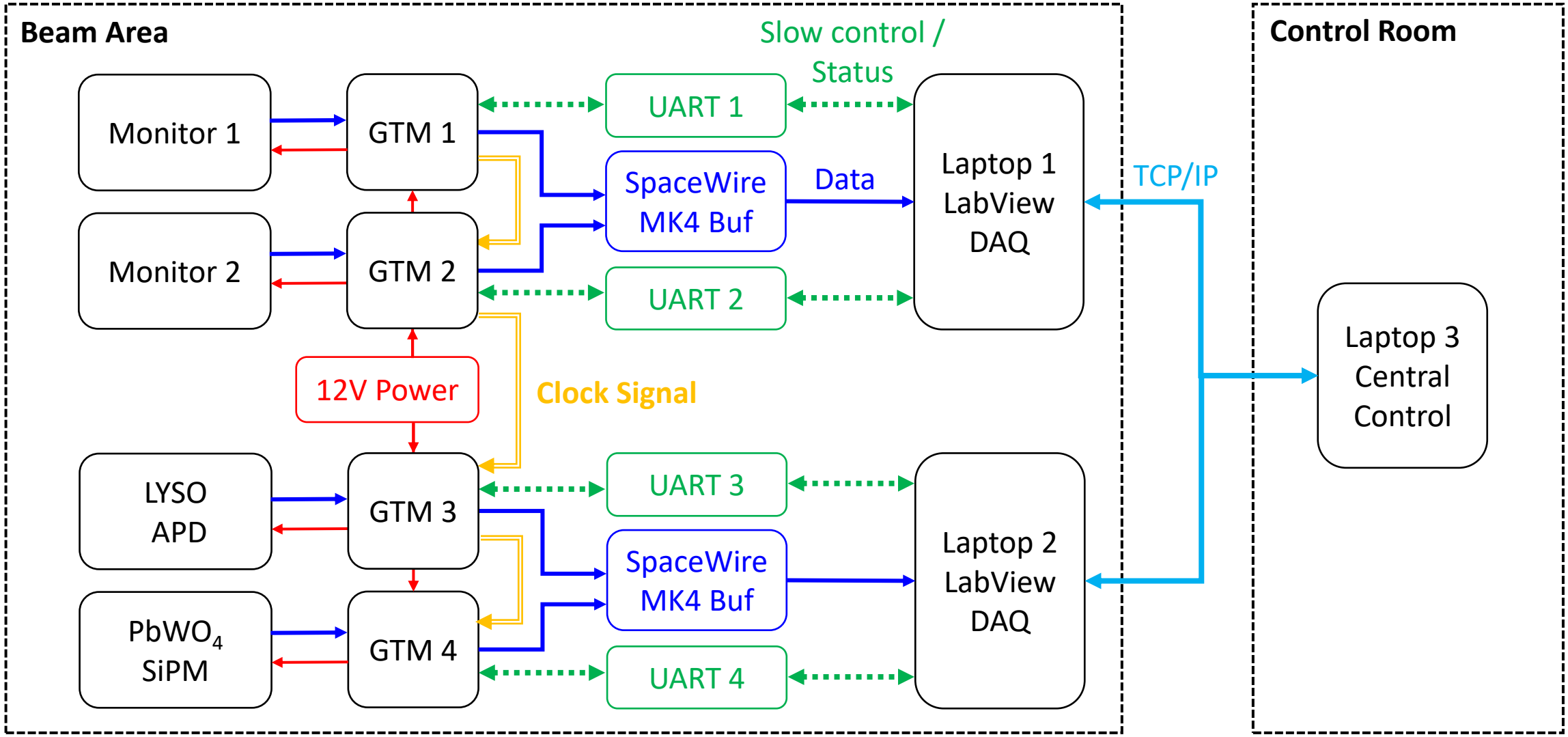
2nd ZDC ECAL Prototype

Modification of GTM module :

- High-voltage convertor for bias of APD
  - Voltage range : 0 - 500V (0.5V step)
  - The voltage fine-tuning still can be adjusted through **CITIROC**.
- Internal / ~~External~~ Trigger mode
  - Due to the shaper's maximum peaking time limit (87.5 ns), it is difficult to capture the correct peak when using external triggering.
- Single board trigger out available

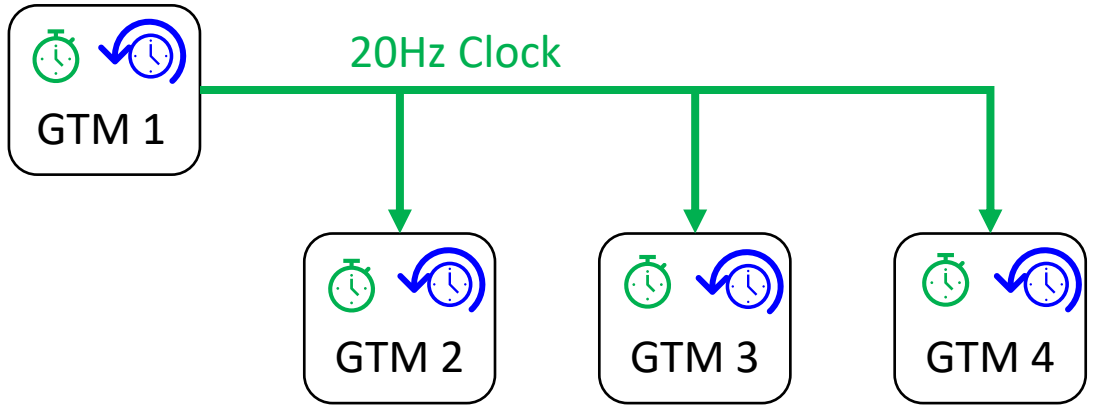


Setup of 2nd ZDC ECAL Prototype



Sync between GTM Modules

- All GTM modules operate in self-trigger mode.
- Each modules takes data independently.
- Data from all modules are **aligned using timestamps.**
- GTM module has two timing count : PCNT (50 ms) and TCNT (240 ns)
- The PCNT clock is generated from a single master module.
- When a board sends or receives a clock pulse, its TCNT value is reset, and the PCNT is increased by one.
- This mechanism ensures time alignment among all modules.



PCNT	TCNT
0	50
0	80
…	…
12	14
12	57
12	121
…	…
128	45
128	543
128	1055

PCNT	TCNT
0	0
12	0
12	14
12	100
…	…
128	543
128	1314
128	2000

PCNT	TCNT
0	15
0	169
…	…
12	14
12	51
…	…
128	12
128	543
128	555

PCNT	TCNT
0	100
0	321
…	…
12	14
12	87
…	…
128	100
128	300
128	543

HGCROC-series ASICs

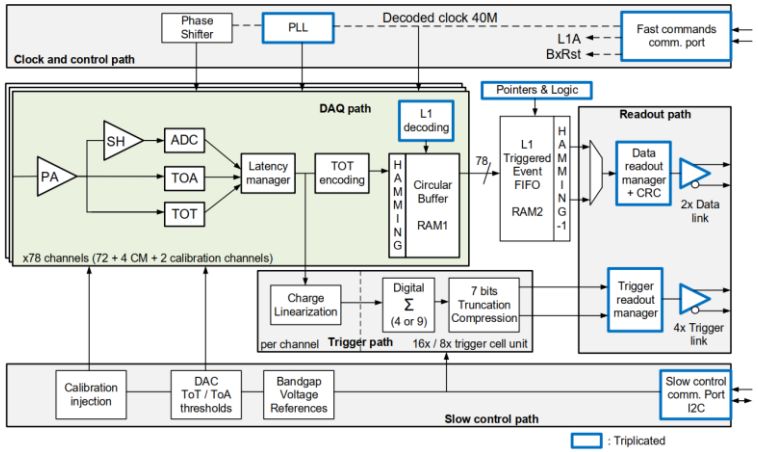
https://indico.cern.ch/event/1255624/contributions/5443779/attachments/2662292/4735427/H2GCROCv3_TWEPP_1_5.pdf

HGCROC 2/3/3a/3b/3c…

- **For Silicon pad sensors**
- Dynamic Range : **0.2fC – 10pC**
- 72 x channels + 4 x CM + 2 x Calib
- Compensation of the leakage : 50µA
- Radiation resistance up to 200 MRad

1 HGCROC3b: architectural overview

The overall block diagram is described as per below.

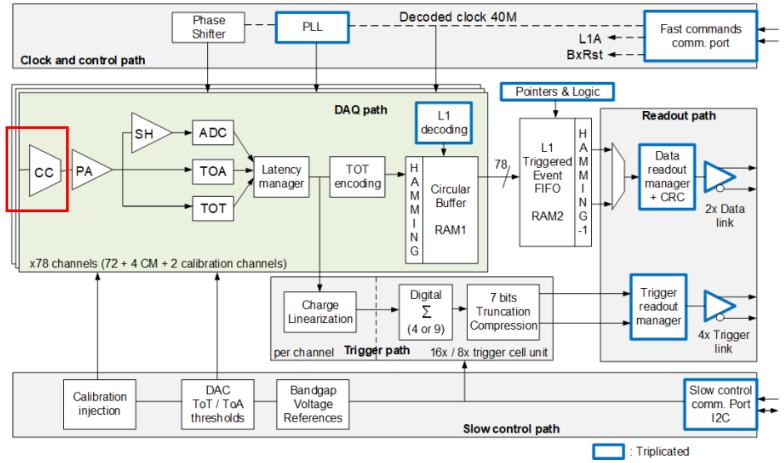


H2GCROC 3b…

- **For SiPM Readout**
- Dynamic Range : **160fC – 320pC**
- 72 x channels + 4 x CM + 2 x Calib
- Compensation of the leakage : 1mA
- Radiation resistance up to 300 kRad

1 H2GCROC3b: architectural overview

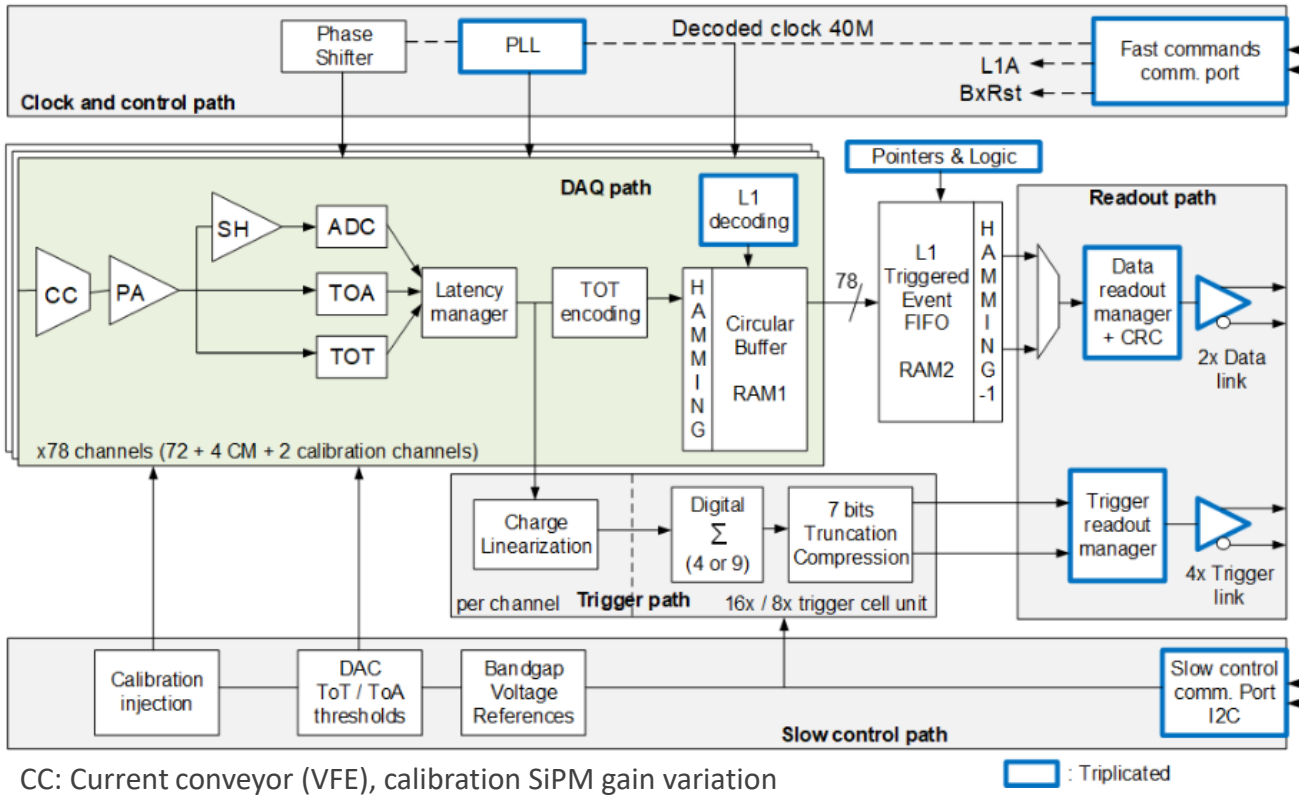
The overall block diagram is described as per below.



- 10-bit ADC with 40MHz sampling rate
- 12-bit TOA measurement (TDC 24 ps)
- 12-bit TOT measurement (TDC 50 ps)
- The ADC output represents the **integrated charge** of the input signal.
- H2GCROC operates in **current-input mode**
- When the **ADC becomes saturated**, the **TOA** and **TOT** measurements are used to **extend the dynamic range**.
- The current conveyor (CC) provides fine adjustment to calibrate SiPM variations.

1 H2GCROC3b: architectural overview

The overall block diagram is described as per below.



320MHz Clock input
Command link (L1A is trigger input)

Two lane for data output:
Speed 1.28Gbps
Charge info, Time info…

Four lane for trigger generation
1.28Gbps x4

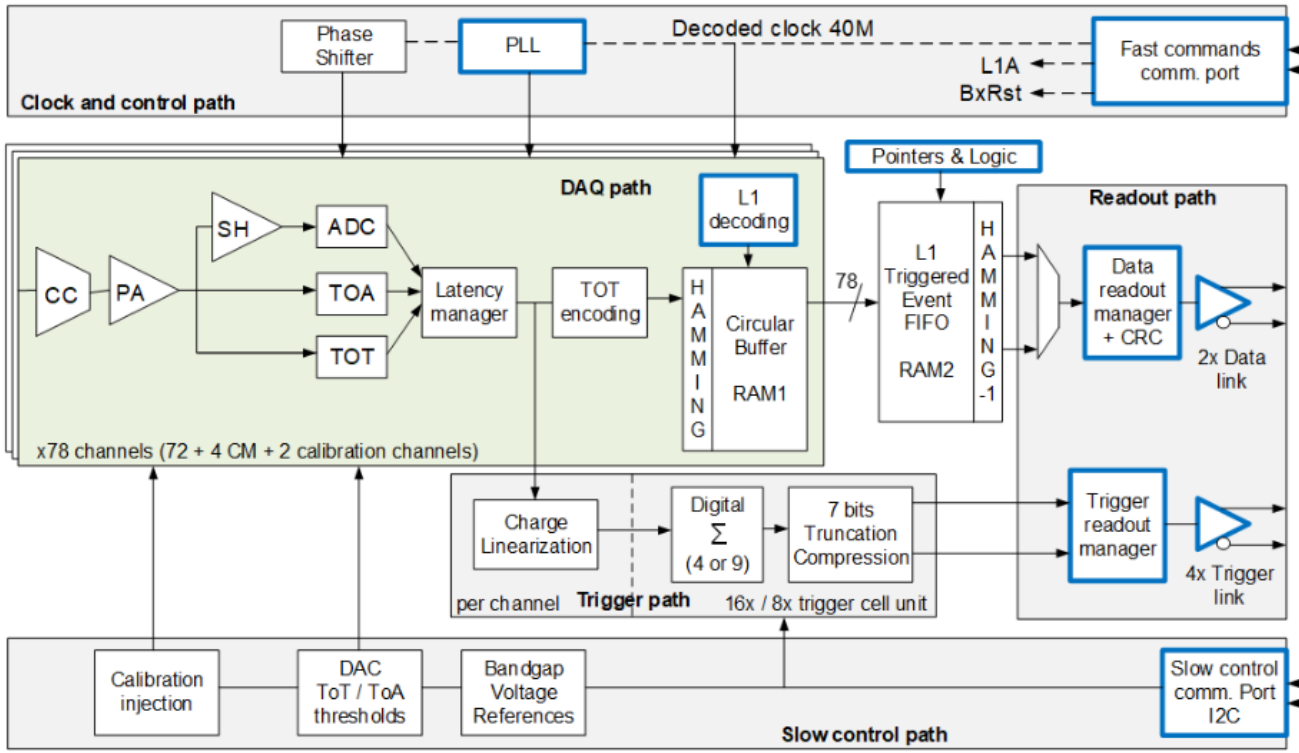
I2C interface read/write 7900 parameters

CC: Current conveyor (VFE), calibration SiPM gain variation
PA: Preamplifier
TOT: Time Over Threshold, dedicated discriminator and TDC (50ps), 12 bit
TOA: Time Of Arrival, dedicated discriminator and TDC (24ps), 12 bit
SH: Shaper
ADC: 10bit 40MHz SARADC

- H2GCROC operates in self-trigger mode, but includes an **internal buffer** that stores data until an external trigger is received to read out the corresponding events.
- Each internal trigger in H2GCROC generates a **compressed event packet** that is sent to the FPGA.
- The FPGA can either use these packets for **self-trigger operation**, or ignore them and run in **external-trigger mode**.
- **2 data output links**, each running at **1.28 Gbps**
- **4 trigger output links**, each running at **1.28 Gbps**

1 H2GCROC3b: architectural overview

The overall block diagram is described as per below.



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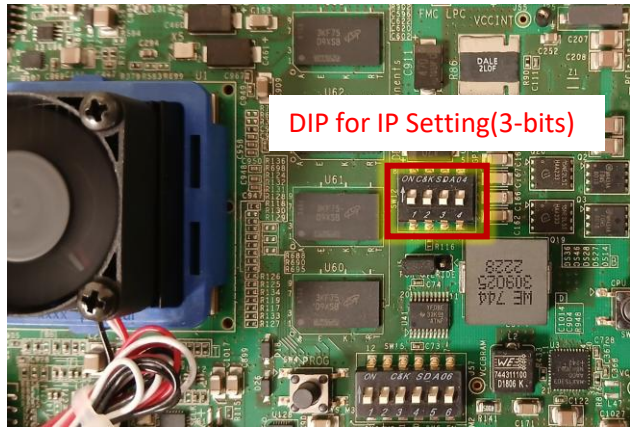
H2GCROC Protoboard



Protoboard:

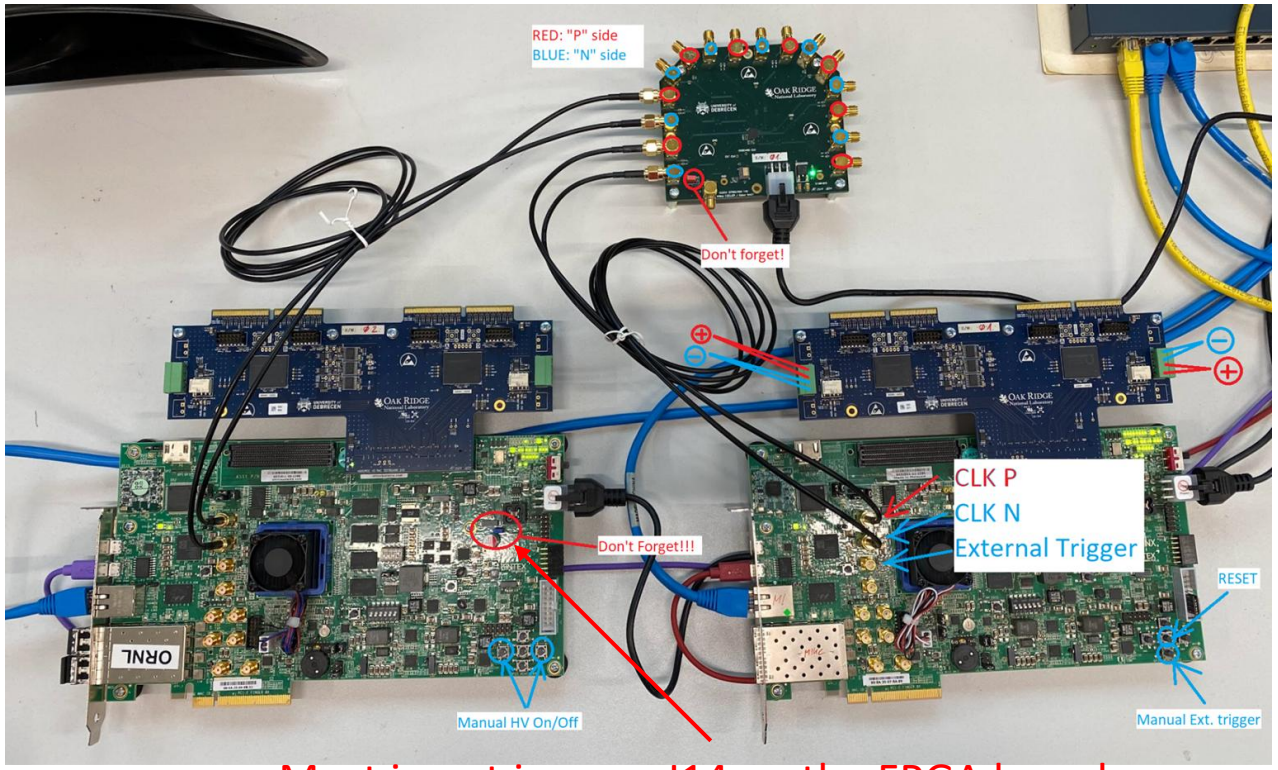
2 x H2GCROC = 2 x (64+8) channels

Requires KCU105 (Xilinx) evaluation board with provided firmware.

Requires an external power supply to provide the SiPM bias voltage.

The protoboard uses a 170-pin 0.8mm high-speed edge card connector. It requires an adapter board to interface with the detector.

Multi-board operation requires IP setup and a common LVDS clock source (SMA).



Must insert jumper J14 on the FPGA board

DAQ Software :

H2GConfig + H2GCDAQ

H2GCalib

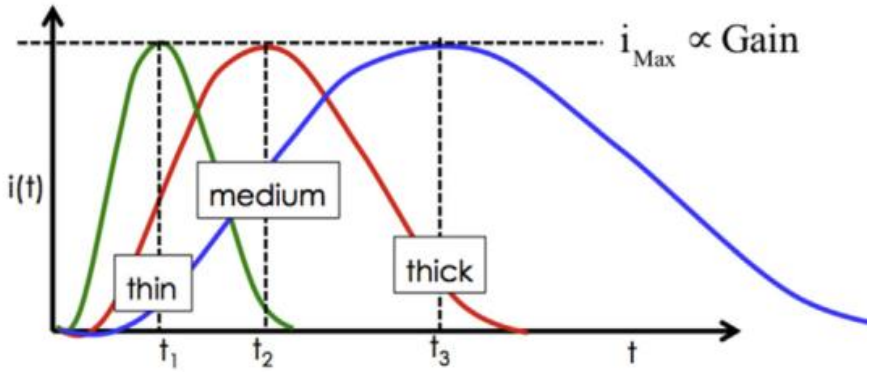
Different ASIC options were discussed at the ZDC workshop (still under consideration).

- **HGCROC series**
  - 64 channels, ~10mW/ch
- **CALOROC**
  - 64 channels, ~10mW/ch
  - Event taking rate : 50kHz
  - CALOROC1A : ADC/TOT + TOA (Based on H2GCROC)
  - CALOROC1B : Switched gain(4) + ADC + TDC
- **EICROC**
  - Designed for AC-LGAD
  - 32 x 32 pixel readout, < 2 mW/ch
  - 50Hz/ch ?
  - EICROC0A : ADC + TOA
  - EICROC0B : Peak sensing, Wilkinson ADC (TOT)

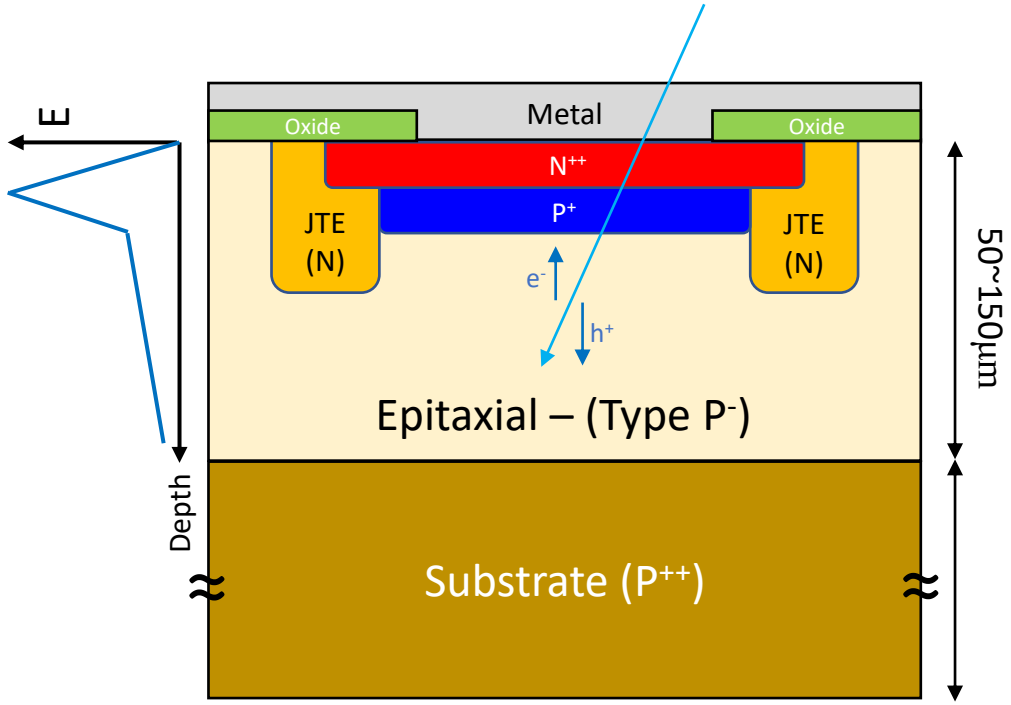
Low Gain Avalanche Diode

- **Ultra-fast Silicon Detector**
  - High time resolution (~30ps)
  - Higher doped p^+ gain layer
  - Thinner bulk

$$\frac{dI}{dt} \propto \frac{G}{d}$$



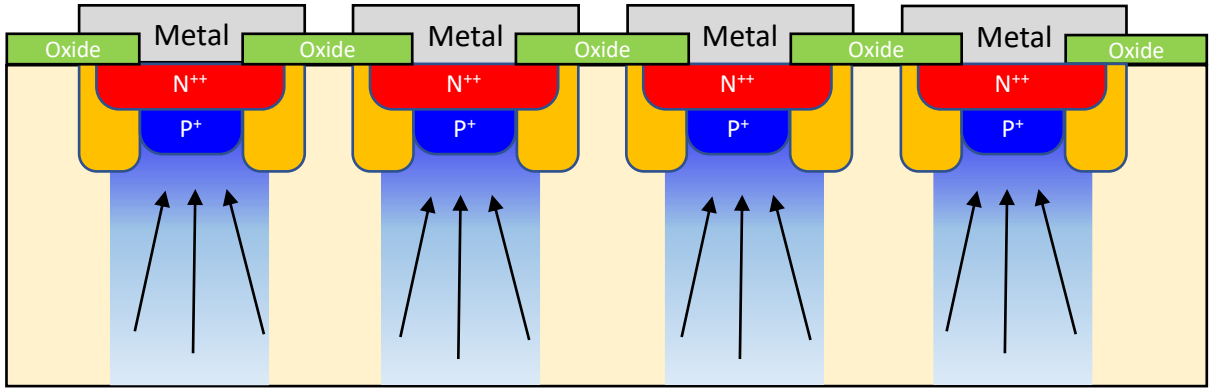
[1] : N. Cartiglia, et al., http://dx.doi.org/10.1016/j.nima.2015.04.025i

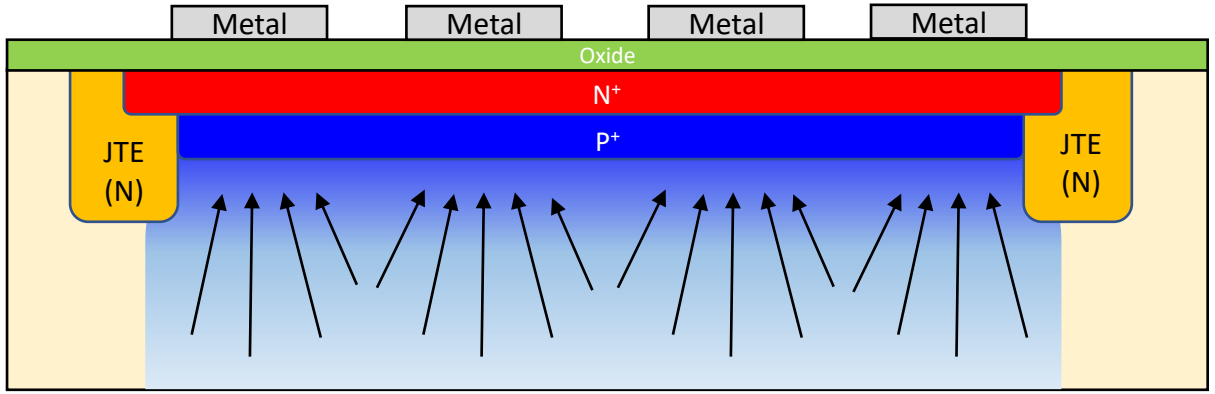


DC & AC Readout

- **DC-LGAD**
  - Simple structure
  - Lager signal
  - Lower p^+ doping
  - Higher n^{++} doping
  - Lower fill factor

- **AC-LGAD**
  - 100% fill factor
  - Higher spacing resolution
  - Consistent and accurate n^+ sheet resistance
  - Higher p^+ doping





AC-LGAD TOF

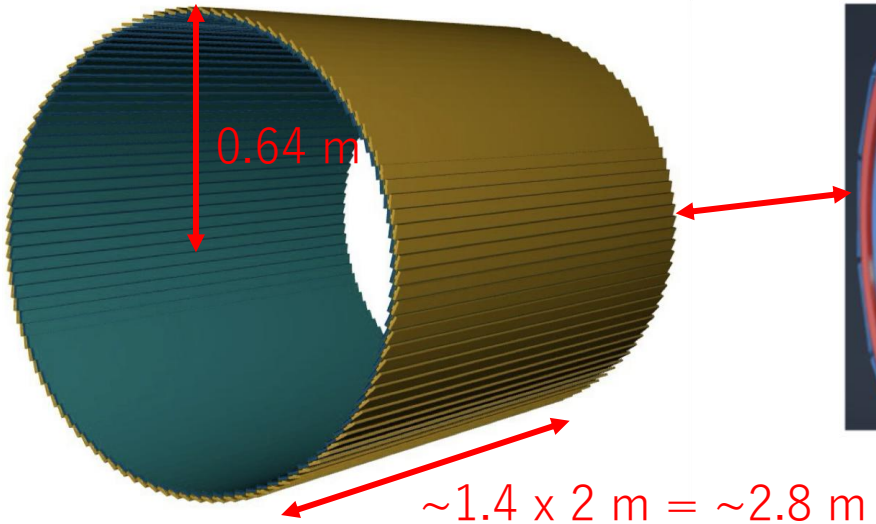
https://indico2.riken.jp/event/5370/contributions/26971/attachments/14228/21657/1027_ZDC.pptx

- AC-LGAD TOF is used for PID, Tracking and background rejection at mid-rapidity and forward-rapidity
- **Timing resolution of 35ps** and **spatial resolution of 30um** with installing in <8 cm thickness space are required

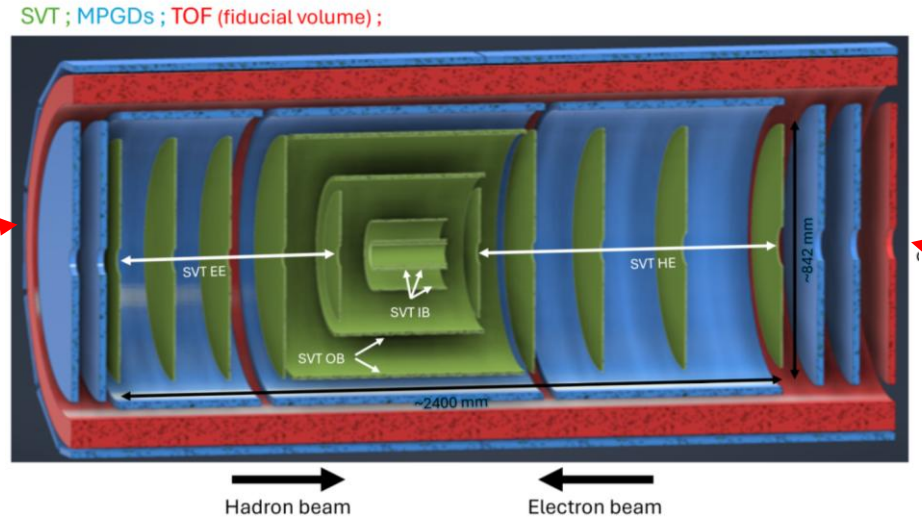
Barrel-TOF (BTOF)

Strip Type AC-LGAD

$-1.33 < \eta < 1.74$



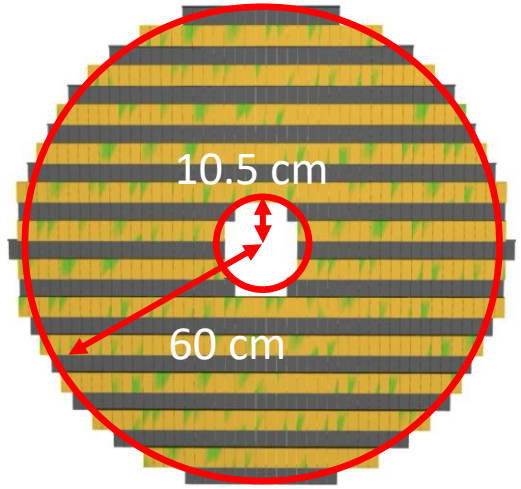
ePIC Tracking System



Forward-TOF (FTOF)

Pixel Type AC-LGAD

$1.84 < \eta < 3.61$



TOF AC-LGAD

https://indico2.riken.jp/event/5370/contributions/26971/attachments/14228/21657/1027_ZDC.pptx

BTOF Strip-Type AC-LGAD

"*Baseline*" sensor fundamental parameters

- Size: 32x20 mm^2
- Strip-size : 10x0.05 mm^2
- Pitch : 500 um
- Strip geometry: 64x2=128 ch
- Active thickness: 50 um
- Sheet resistance: 1600Ω/ □
- Coupling capacitance: 240 pF/mm^2

Current best performance

- eRD112 FY23 sensor
  - 5x10 mm^2, 10x0.05 mm^2 / 500 um
- The sensor was tested at FNAL 120 GeV proton
  - Timing resolution: 35 ps
  - Spatial resolution: 15~20 um

FTOF Strip-Type AC-LGAD

"*Baseline*" sensor fundamental parameters

- Size: 16x16 mm^2
- Pixel-size : 0.15x0.15 mm^2
- Pitch : 500 um
- Pixel geometry: 32x32=1024 ch
- Active thickness: 20 um
- Sheet resistance: 400Ω/ □
- Coupling capacitance: 600 pF/mm^2

Current best performance

- eRD112 FY23 sensor
  - 2x2 mm^2, 0.15x0.15 mm^2 / 500 um
- The sensor was tested at FNAL 120 GeV proton
  - Timing resolution: ~20 ps
  - Spatial resolution: 20~35 um

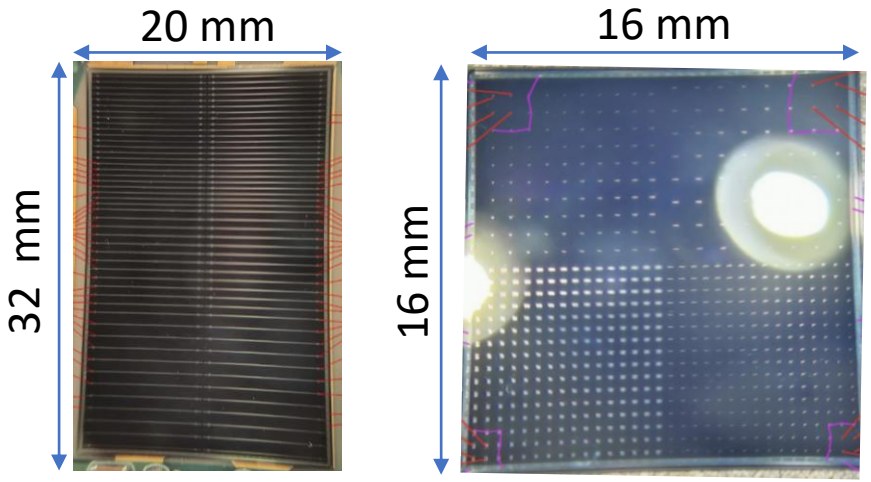
Current progress of TOF AC-LGAD

https://indico2.riken.jp/event/5370/contributions/26971/attachments/14228/21657/1027_ZDC.pptx

First full-size sensors (eRD112 FY24)

- Including different pitches strip and pixel design.
- The beam test at JLab has been completed. (awaiting analysis results)

eRD112 FY24

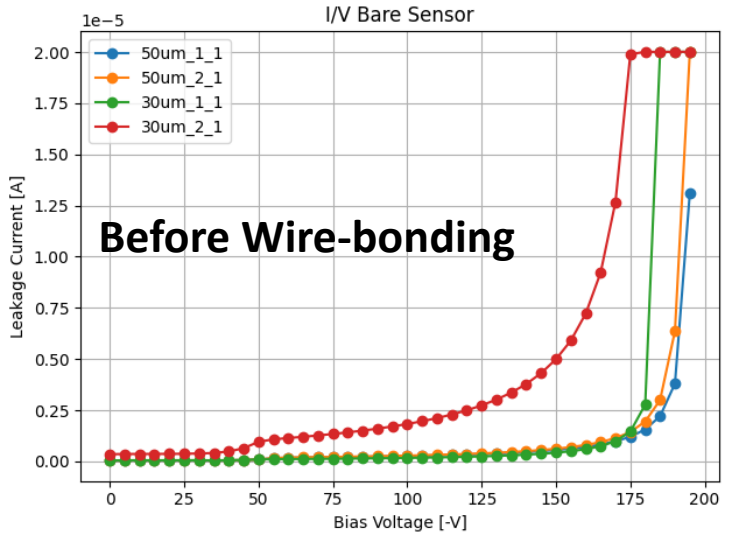


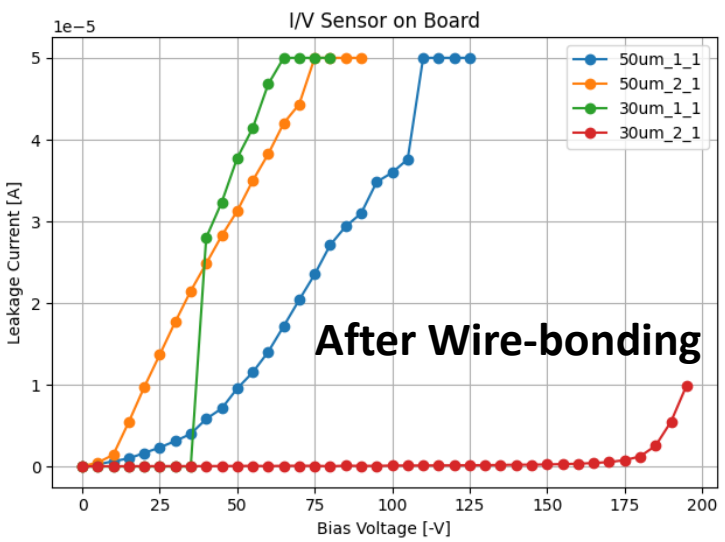
Real full-size strip AC-LGAD

- Received this September
- Test beam at DESY and RARiS is scheduled in December-2025 and March-2026

Wire-bonding damage

- Oxidization film damage by wire-bonding is suspected
- Coating bonding pad design will be used for the next production
- HPK suggested us to use ball-bonding instead of wedge-bonding





ASIC for Strip Type AC-LGAD

https://indico2.riken.jp/event/5370/contributions/26971/attachments/14228/21657/1027_ZDC.pptx

Analog block of FCFD

FCFDv0: 2021

- 10 ps jitter @ 20 fC (Ch. Inj.)

FCFDv1: 2024

- 10 ps jitter @ 20 fC (Ch. Inj.)
- 35 ps timing resolution w/ DC-LGAD
- 52 ps timing resolution w/ AC-LGAD

Unexpected parasitic capacitance

FCFDv1.1

- Fixed input capacitance to fit ~10 pF
- 31 ps timing resolution is expected (by simulation)

CFDROC (FCFD+digital block)

available in early 2026

TOA (10bit) + ADC (9bit)

Requirement

- Measure ADC and TOA
- # channels: 2x64 = 128 ch
- Detector capacitance: ~10 pF
- Dynamic range:10 - 70 fC
- Signal MPV : 25 fC
- Jitter at MPV : around 20 ps
- Signal occupancy: O(1) Hz per sensor
- Power consumption: <4 mW/ch

Summary

- **CITIROC 1A - SiPM**
  - 2 Gains + Peak sensing (14-bit ADC convertor in GTM board)
  - Taking rate : 40k Hz
  - ZDC ECal prototype readout system during 2024 and 2025 ELPH beam test.
  - Limited by the slow shaper, GTM could not run in external-trigger mode.
  - Further study may be required to understand the impact of APD signal input.
- **H2GCROC 3b (SiPM ver.)/ HGCROC 3c (Si ver.)**
  - 10-bit ADC / 50ps TOT + 24ps TOA
  - The system supports both external and self-trigger operation.
  - FoCal is in the process of setting up the HGCROC3c DAQ system.
  - We are building a test system for the H2GCROC3b and plan to perform a beam test with a prototype detector next year.
- **CALOROC - SiPM**
  - CALOROC1A : ADC/TOT + TOA
  - CALOROC1B : Switched gain(4) + ADC + TDC
  - Taking rate : 50k Hz
- **EICROC – AC-LGAD**
  - EICROC0A : ADC + TOA
  - EICROC0B : Peak sensing, Wilkinson ADC (TOT)

Summary

- **TOF AC-LGAD**
  - Test results for the test structure already satisfy the TOF specifications.
  - The beam test of the full-size sensor at JLab has been completed.
  - The first real sensor will be tested in 2026.
  - In the full-size sensor tests, wire bonding is suspected to have caused damage to the oxide dielectric layer, resulting in performance degradation.
  - Bonding pads will be included in the next version of the design.
- **AC-LGAD progress in Taiwan**
  - Preliminary parameter testing at Tyntek has been completed.
  - The first AC-LGAD test structure will be fabricated following BNL's process in next year.
  - We are in discussions with another company, Mosel Vitelic, to make sure we have enough options for making the product.
  - We plan to use double metal for the bonding pad design in the first production.

Back up

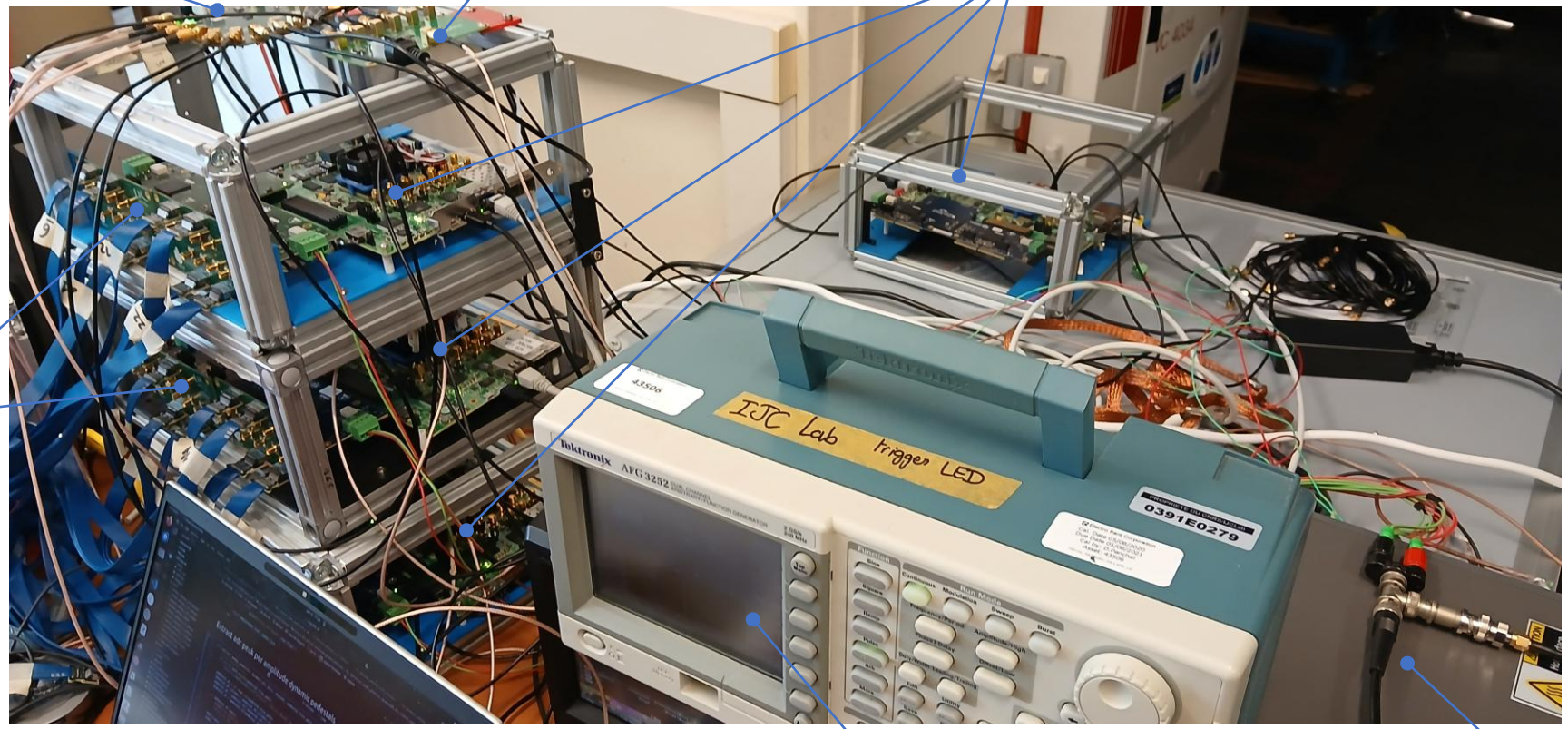
Hardware

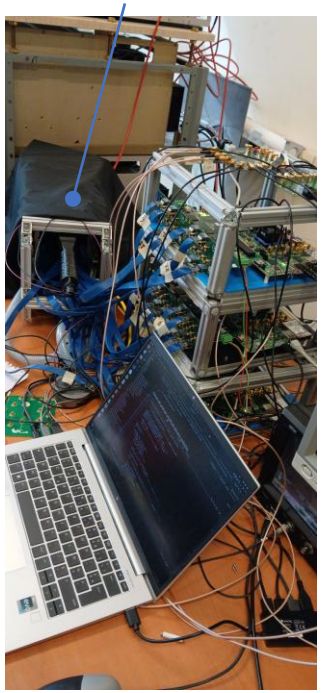
Common clock board

Trigger fan out board

KCU105 & protoboard x4

Crystal





Adapter board

Signal generator x1

High Voltage Supply

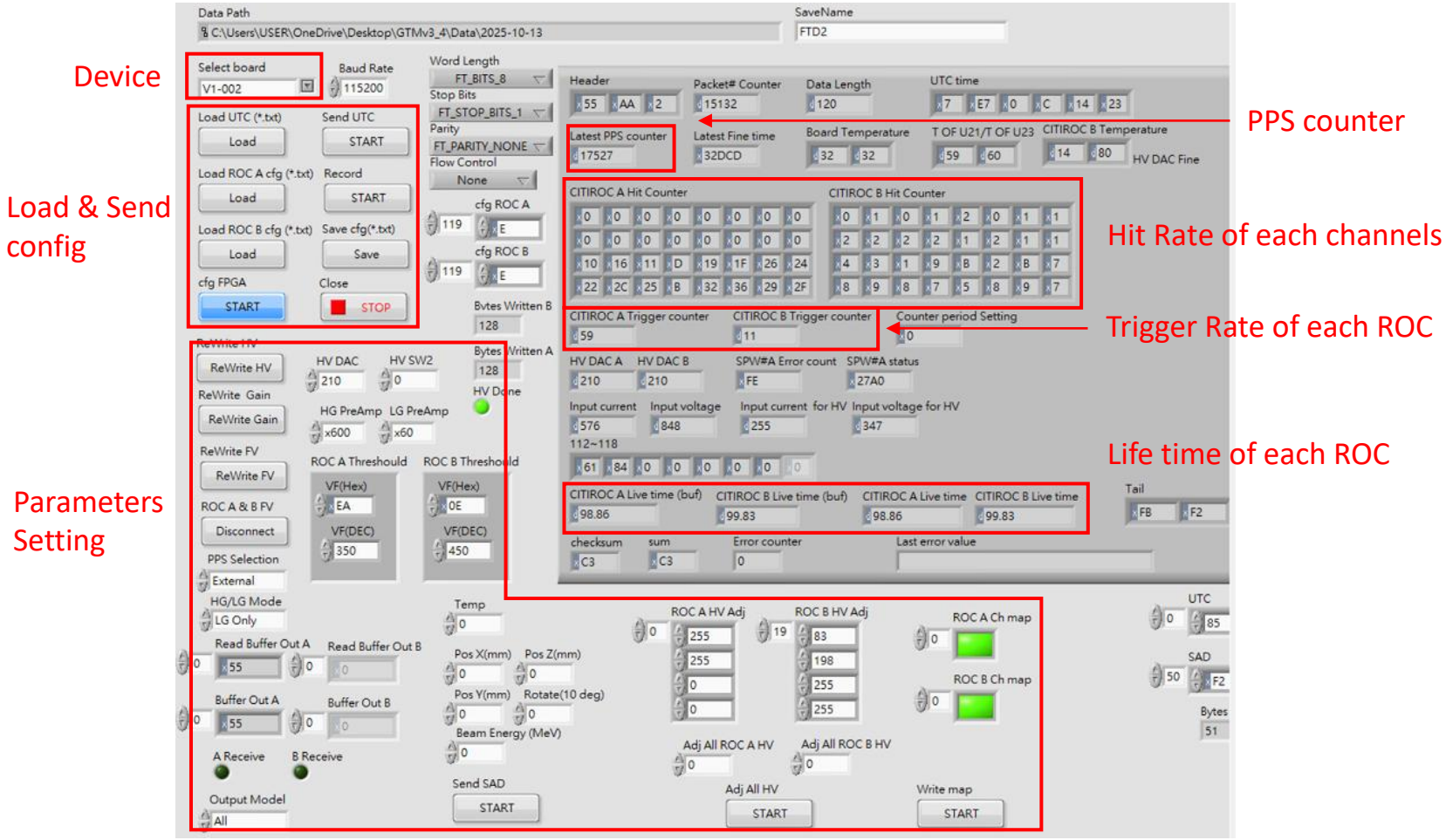
LabView DAQ Config

Setting

- Load & Send CMD list to FPGA
- HV setting
- Threshold setting
- Pre-amplifier gain
- Operation mode

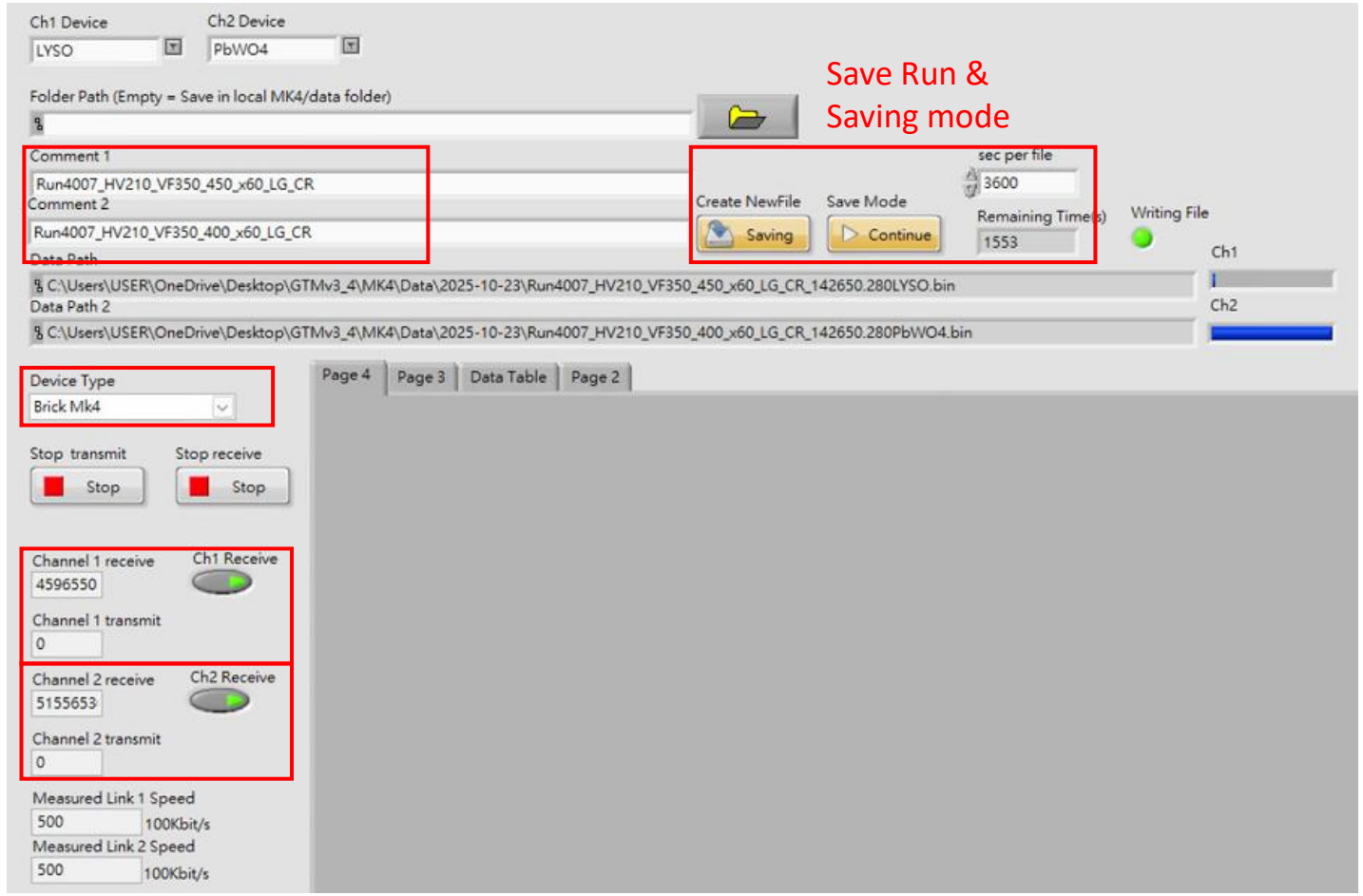
Status Monitor

- PPS count
- Hit rate of channels
- Trigger rate of ROCs
- Life time



LabView DAQ Data Taking

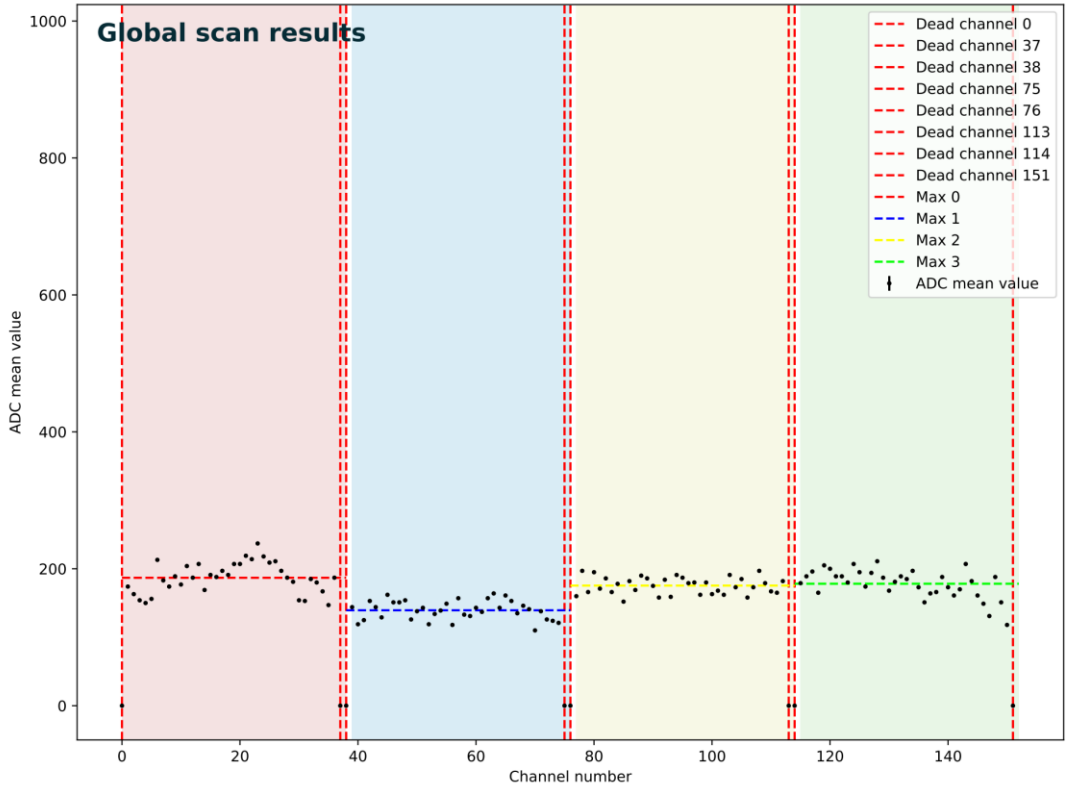
- Each SpaceWire MK4 module has two channels
- The program continuously reads data from the MK4 module (read-only).
- When Save is pressed, the acquired data are written to a binary file.
- The recording time can be adjusted.
- Supports both single-shot and continuous saving modes.
- Sent copy data to the online display for real-time monitoring.



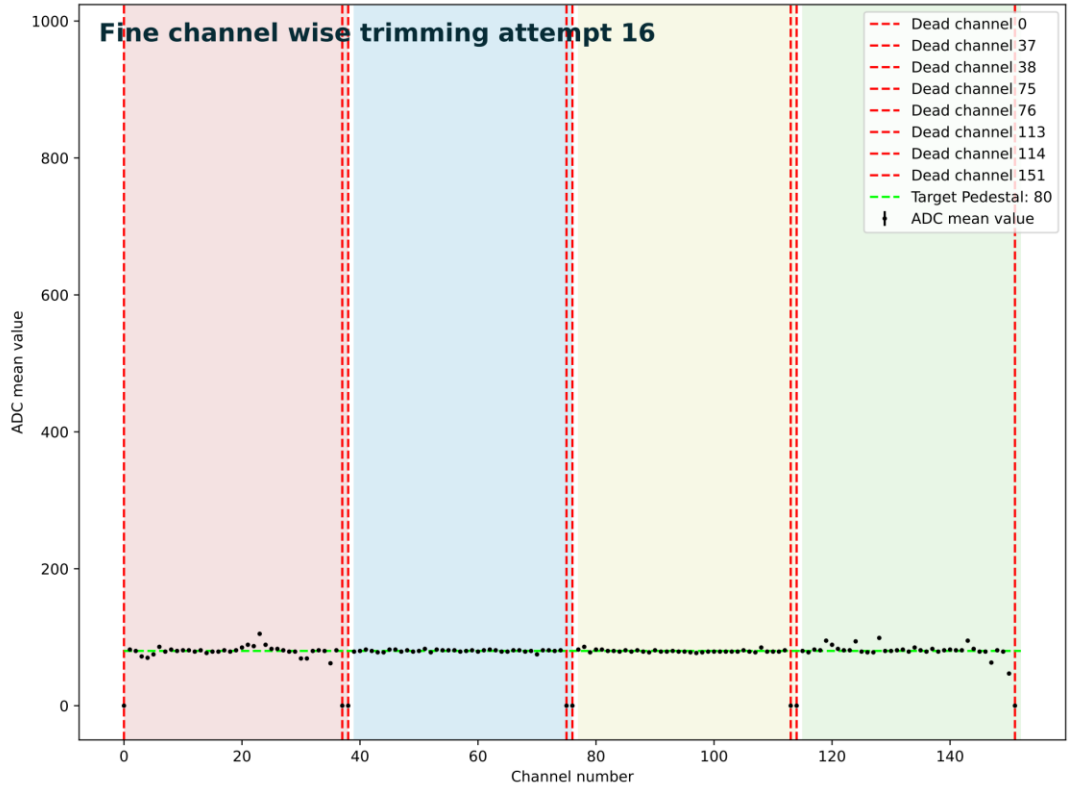
ADC Pedestal Calibration

- python H2GCalib_3B/ 000_SocketPool.py
  - ➢ This program maintains multiple network connections, and other calibration programs use this as a relay, keep this program running in the background
- python H2GCalib_3B/005_PedestalCalib.py

Before Calibration



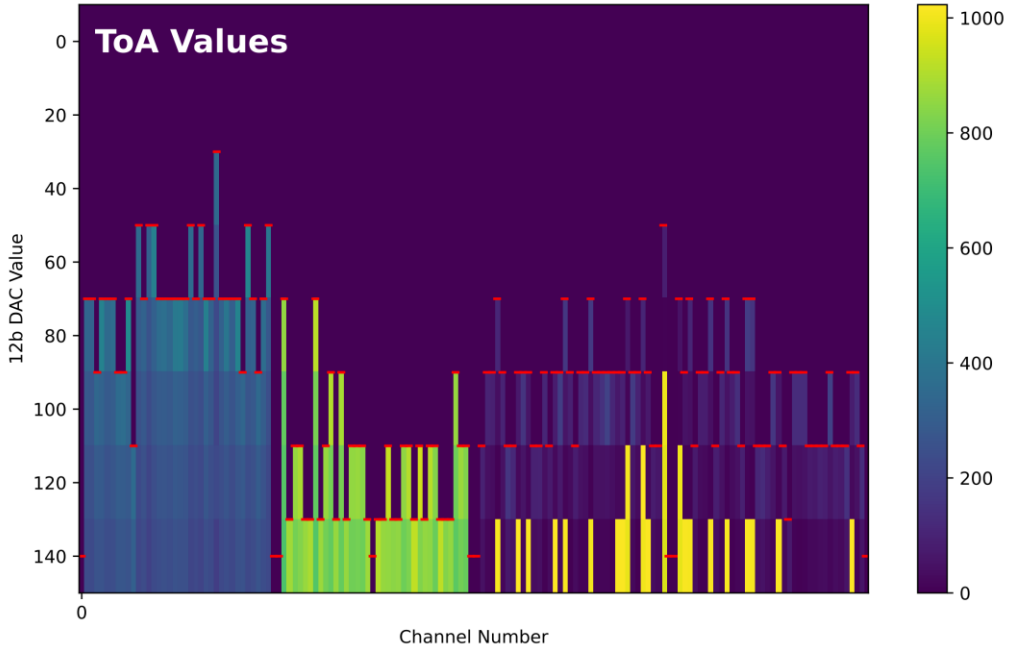
After Calibration



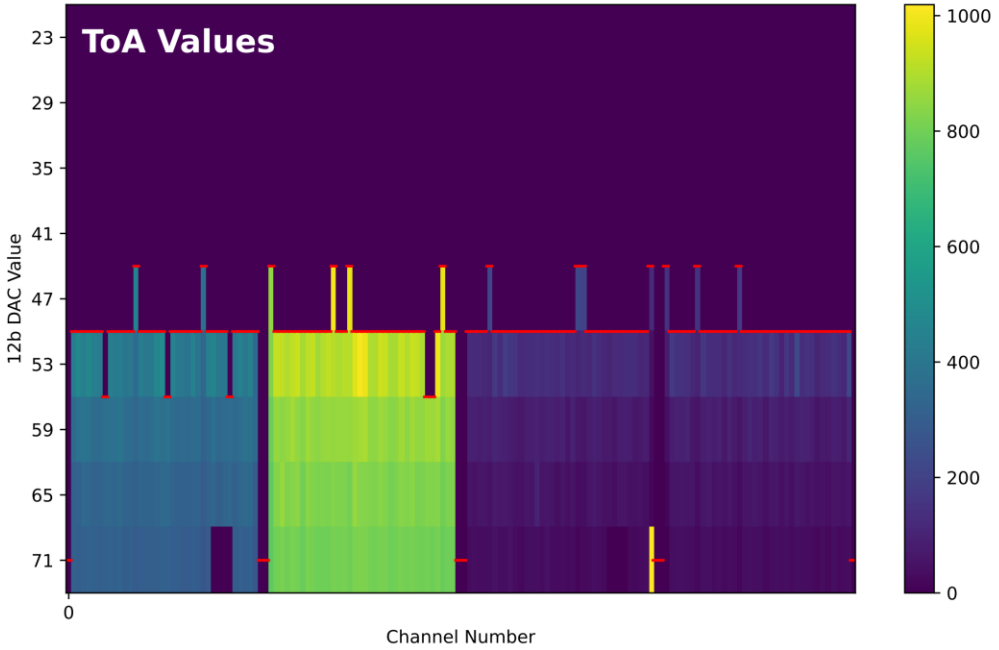
TOA Calibration

- python H2GCalib_3B/006_ToACalib.py -t 50 -i ./{a0 pedestal conifg file},./{a1 pedestal conifg file}
- a0 : dump/005_PedestalCalib_data_20250618_183209/config_pede_a0_20250618_183343.json
- a1 : dump/005_PedestalCalib_data_20250618_183209/config_pede_a1_20250618_183343.json

Before Calibration



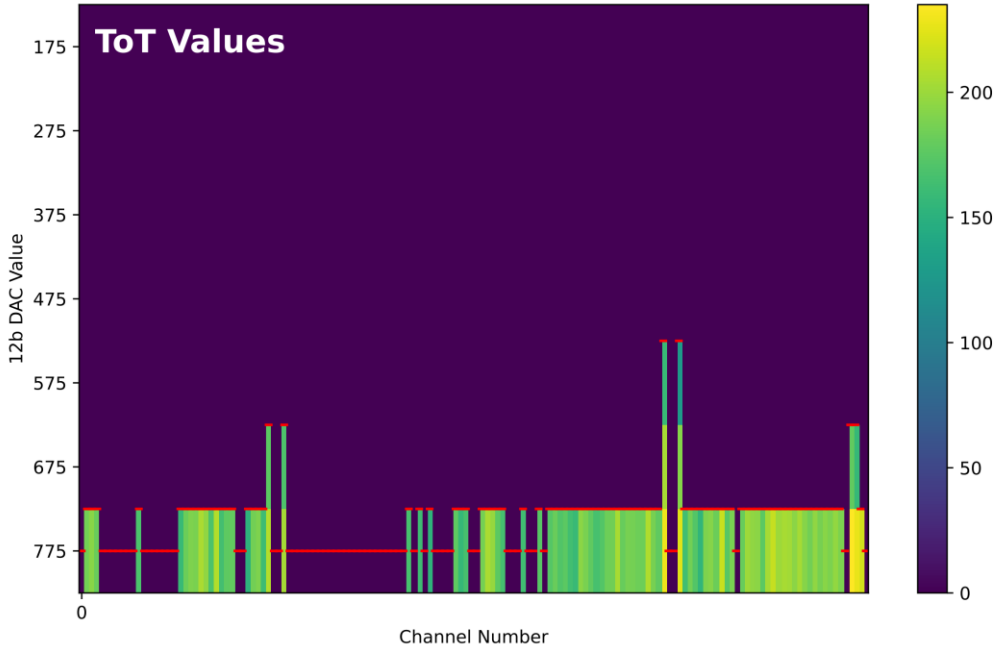
After Calibration



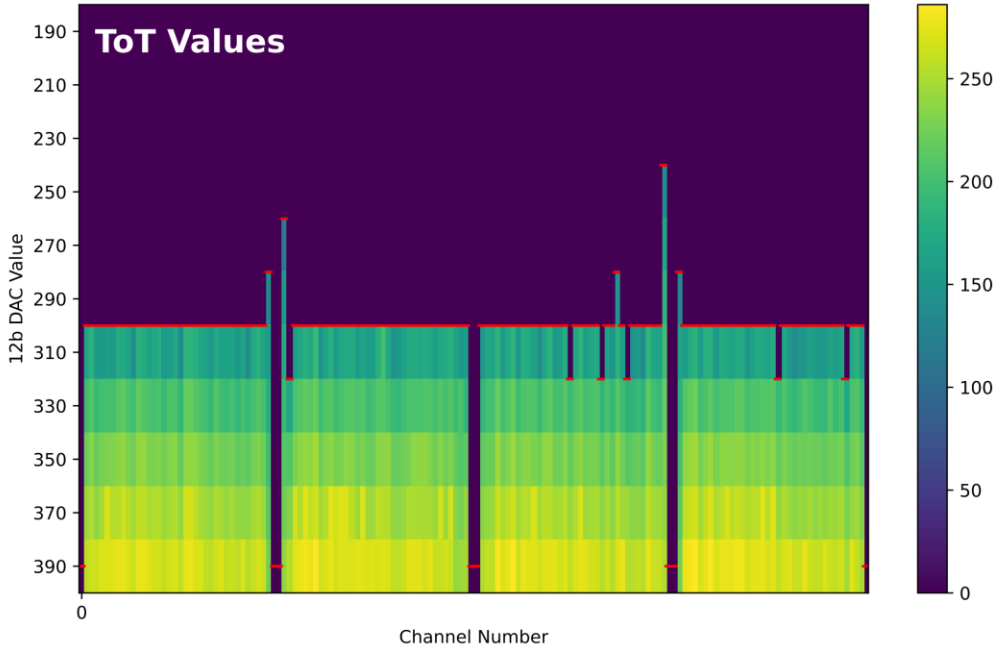
TOT Calibration

- python H2GCalib_3B/010_ToTCalib.py -t 300 -i ./{a0 TOA conifg file},./{a1 TOA conifg file}
- a0 : dump/006_ToACalib_data_20250618_205115/config_toa_a0_20250618_212606.json
- a1 : dump/006_ToACalib_data_20250618_205115/config_toa_a1_20250618_212606.json

Before Calibration



After Calibration

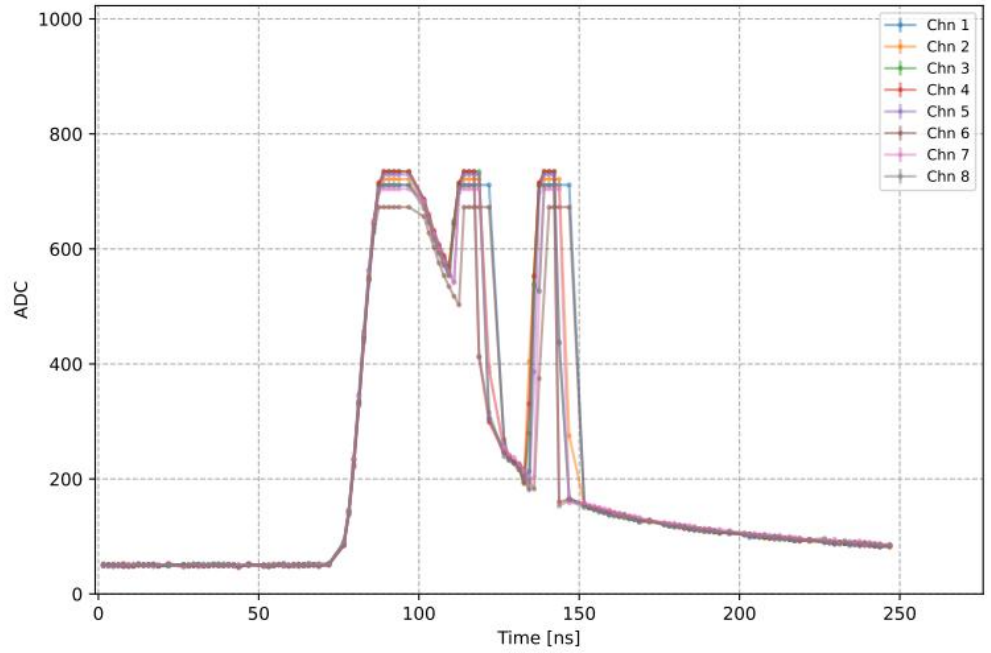


Inject 2.5V Signal Test

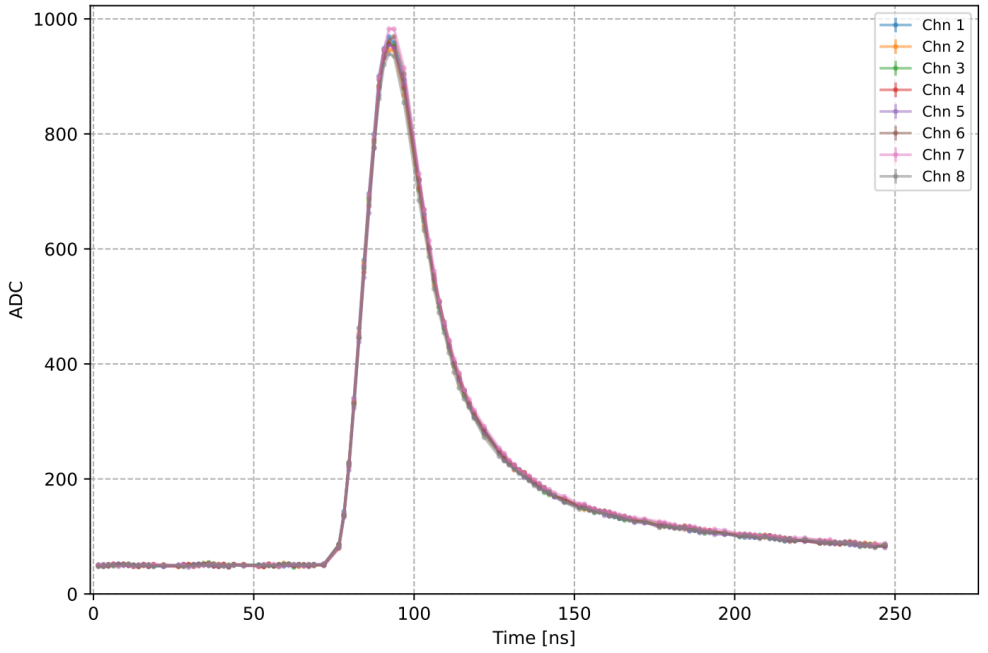
H2GCROC can generate an internal 2.5 V test signal for calibration purposes.

- python.exe ./009_IntInjection_2V5.py -i ./{a0 TOT conifg file},./{a1 TOT conifg file}
- a0 : dump/010_ToTCalib_data_20250618_213759/config_tot_a0_20250618_221027.json
- a1 : dump/010_ToTCalib_data_20250618_213759/config_tot_a1_20250618_221027.json

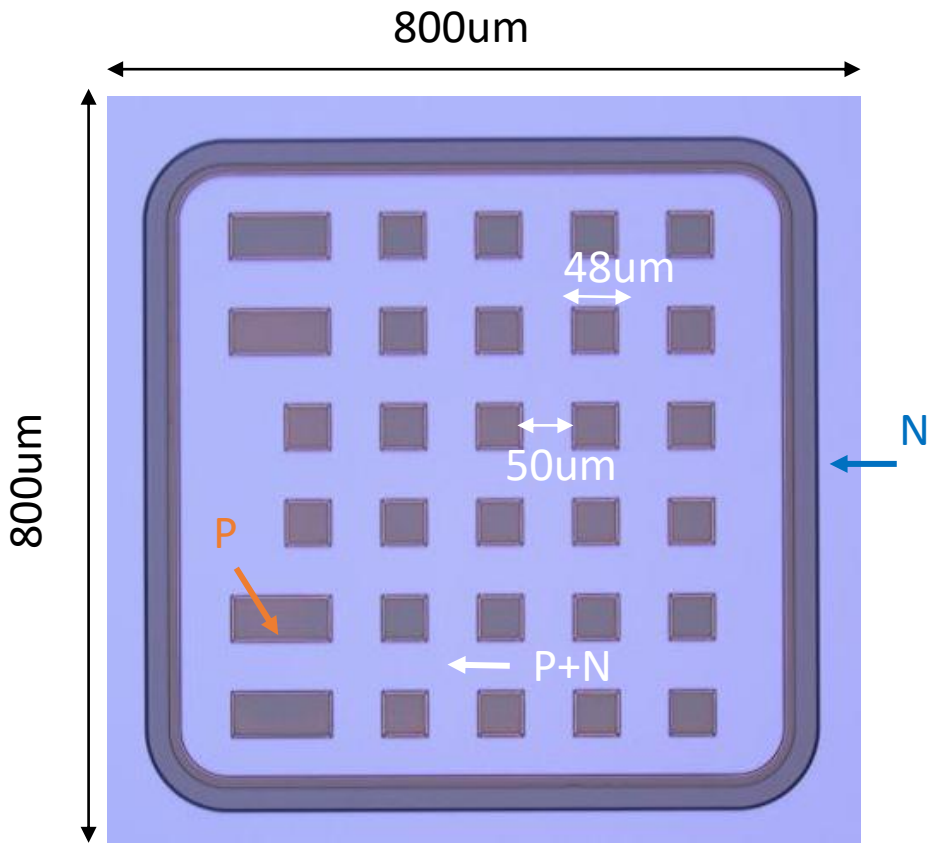
Before Calibration

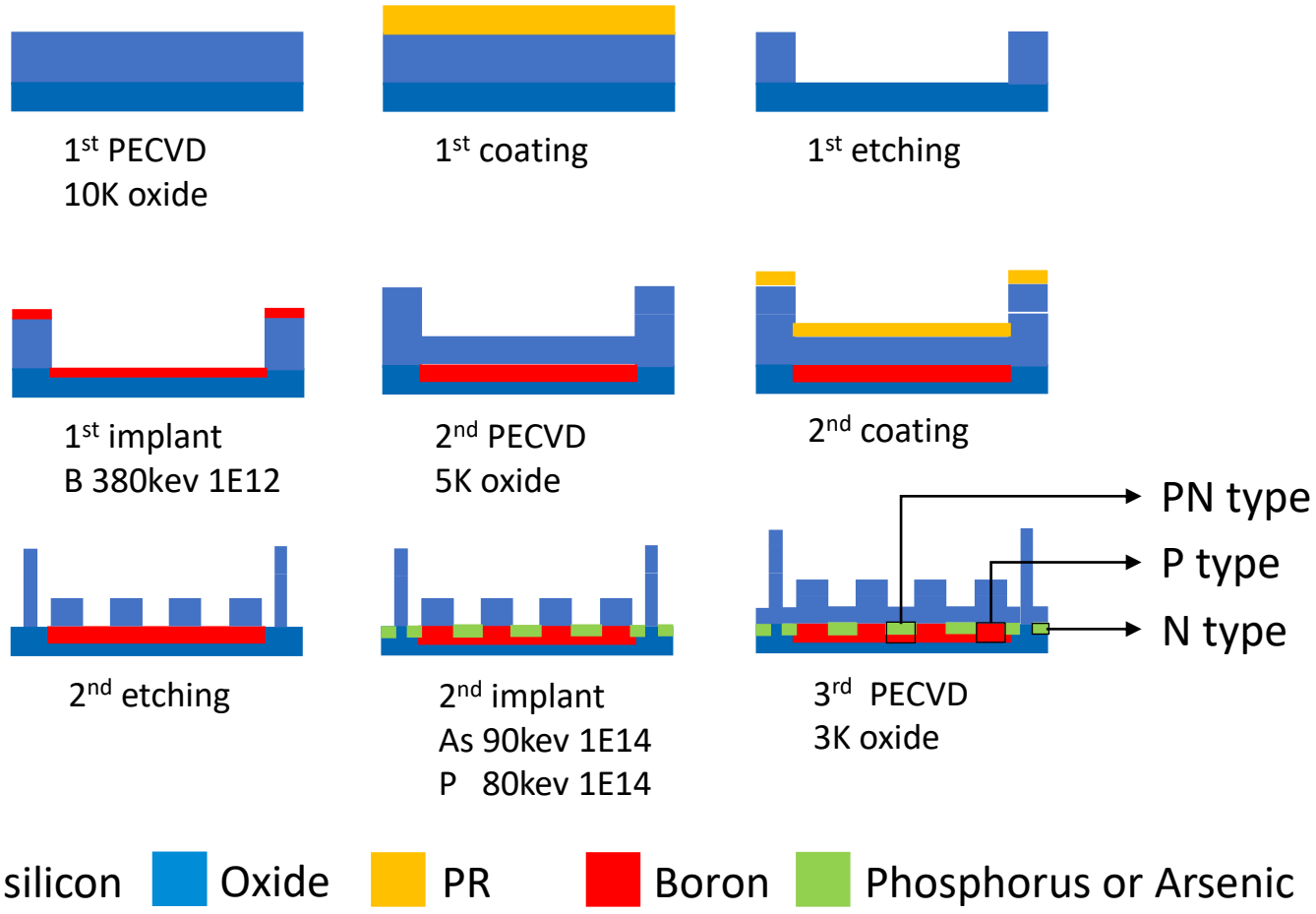


After Calibration



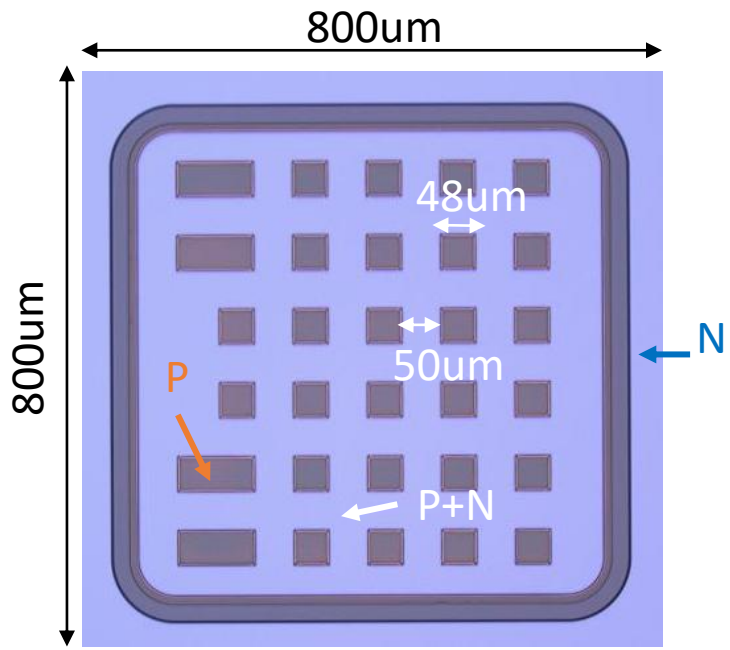
Try Run Structure

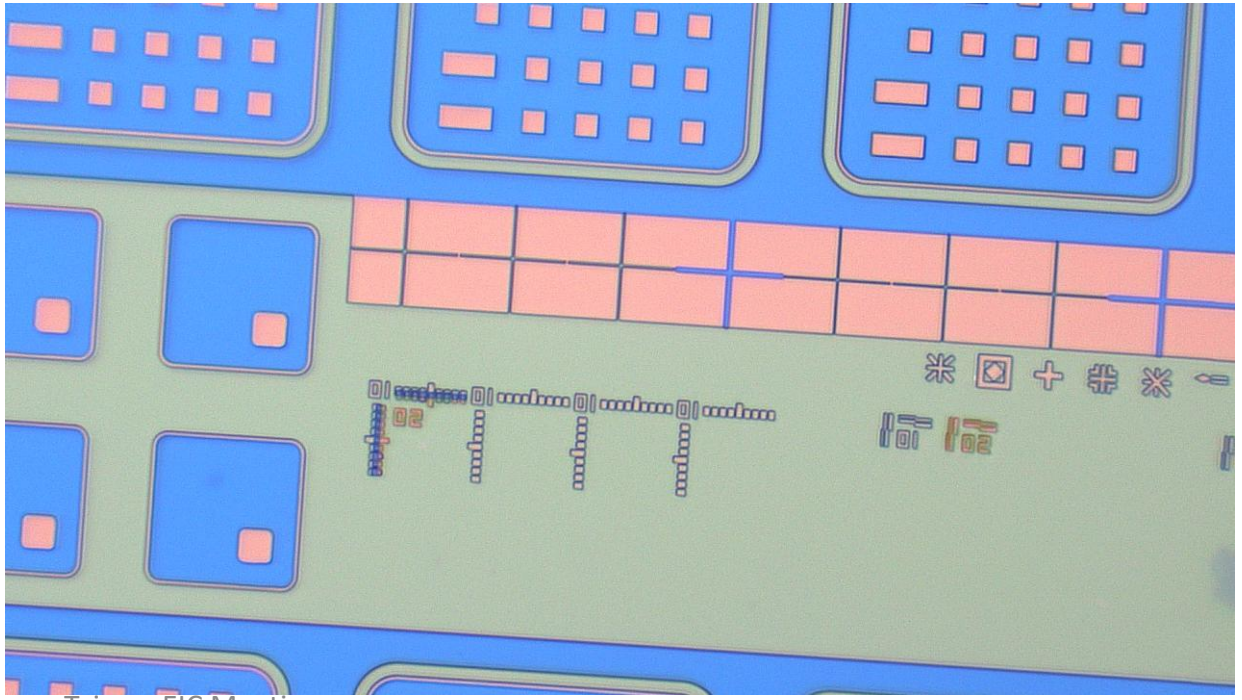




Pattern Resolution

- Among the 8 test wafers fabricated in this run, the photomask pattern showed good clarity and uniformity.
- However, further improvement is needed in photoresist baking to prevent minor exposure defects in localized areas.
- The recommended photomask size for the stepper tool is 2.8 cm × 1.2 cm.

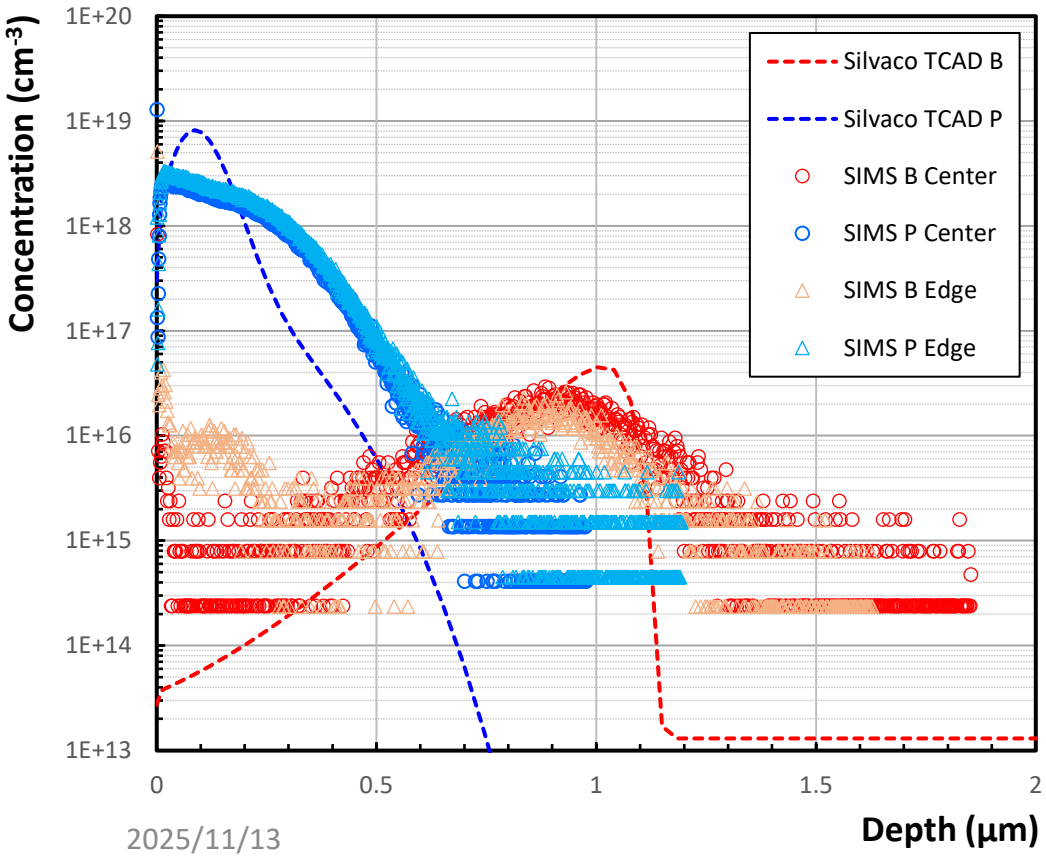




TCAD Simulation

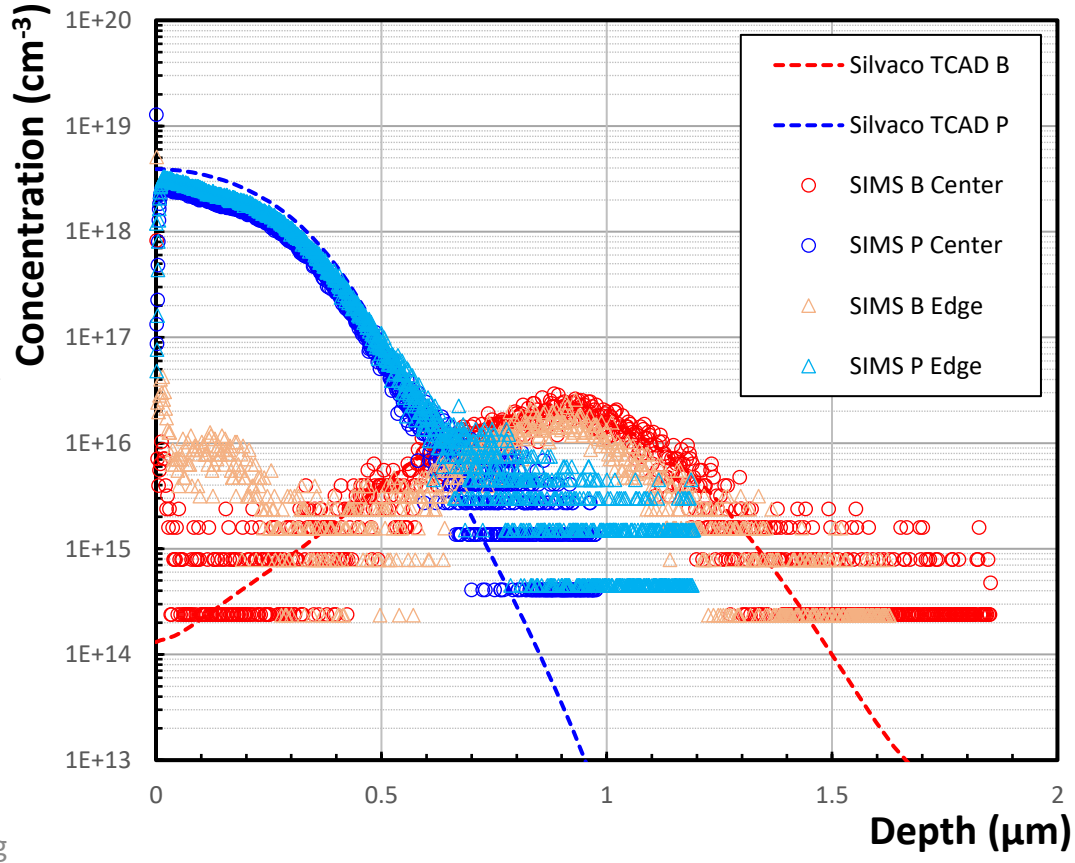
- In the simulation, adding a certain level of damage during the implantation resulted in good agreement with the SIMS data.

Simulation before fabrication



Imp. damage

Simulation after fabrication



SIMS & TCAD with Calibration

	Implant 1			Diffusion 1		Implant 2			Diffusion 2	
	impurities	Dose(cm^{-2})	Energy	°C	min	impurities	Dose(cm^{-2})	Energy	°C	min
#04	B	1.00E+12	380keV	800	20	As	1.00E+14	90keV	800	20
#10						P	1.00E+14	80keV