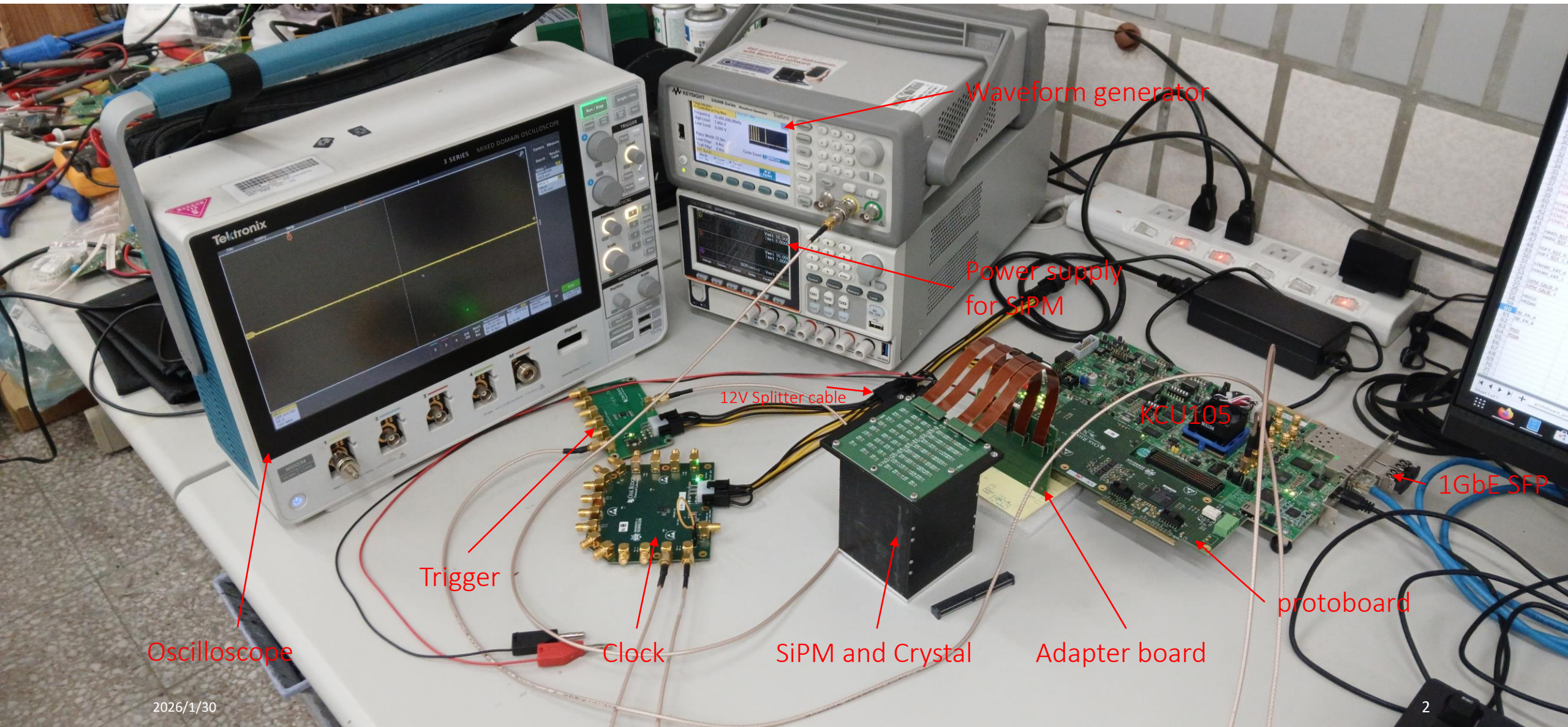


Prepare to use H2GCROC for beam testing

2025-2026

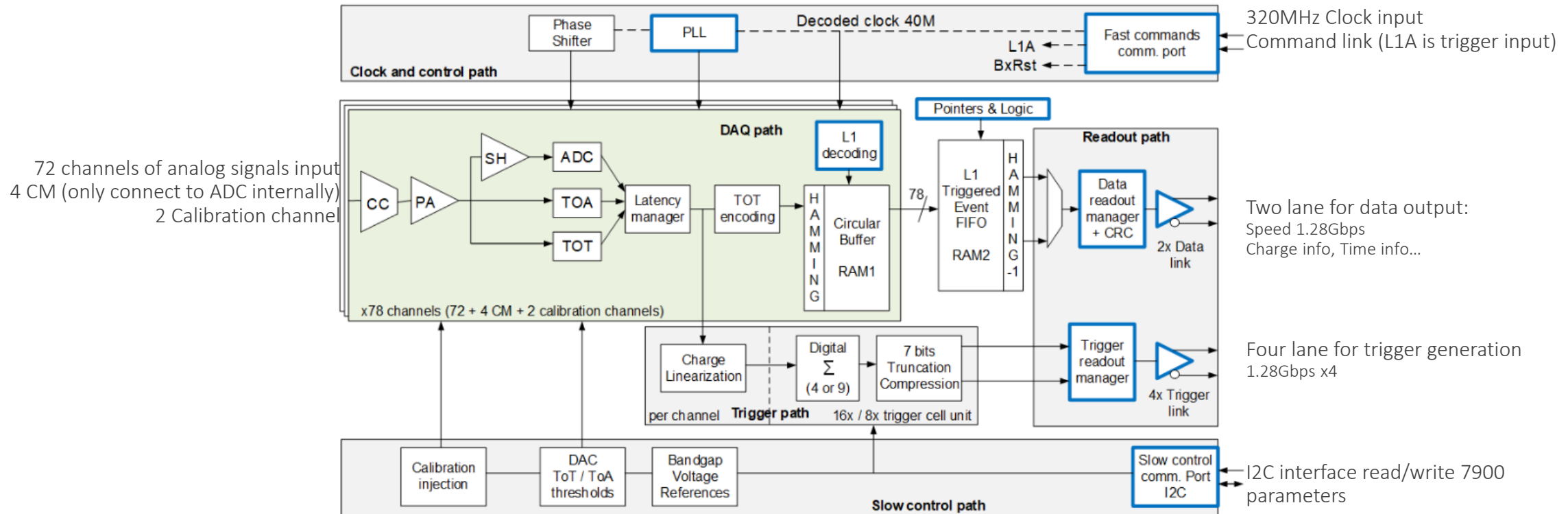
Current environment



Architectural

1 H2GCROC3b: architectural overview

The overall block diagram is described as per below.



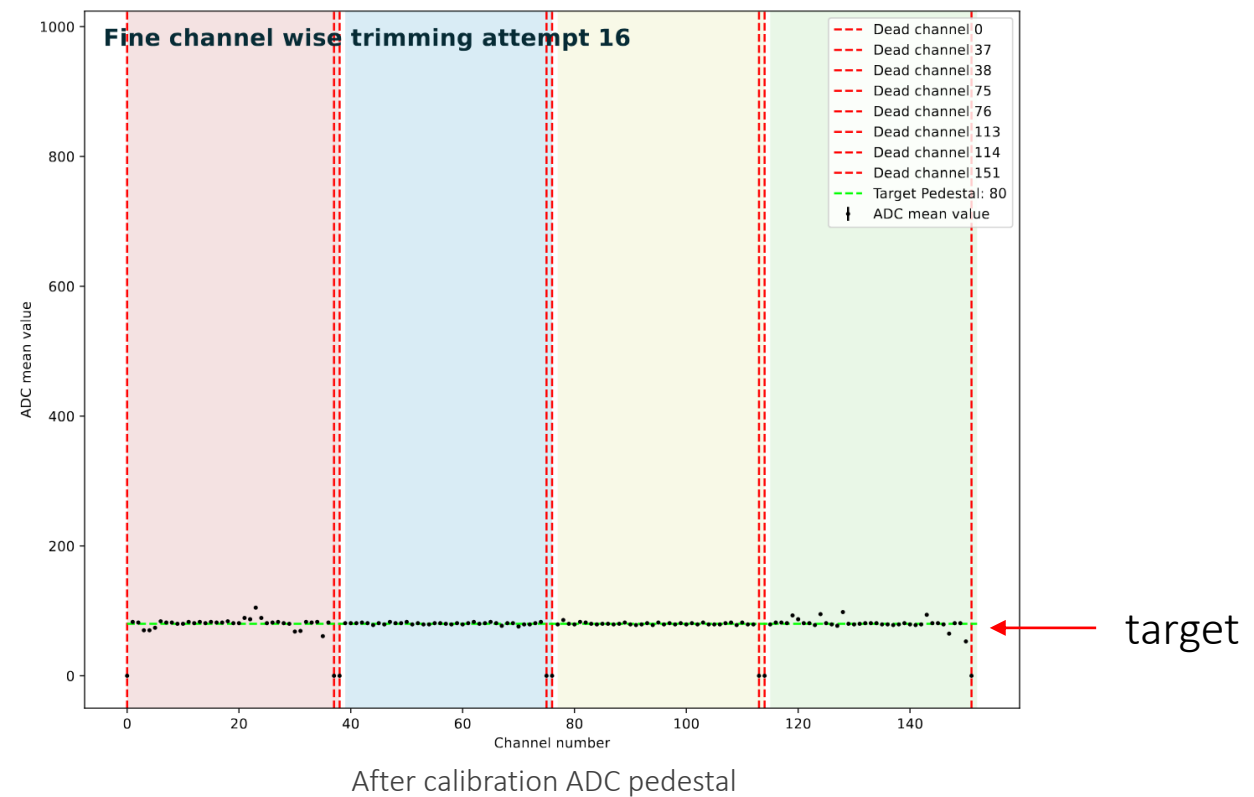
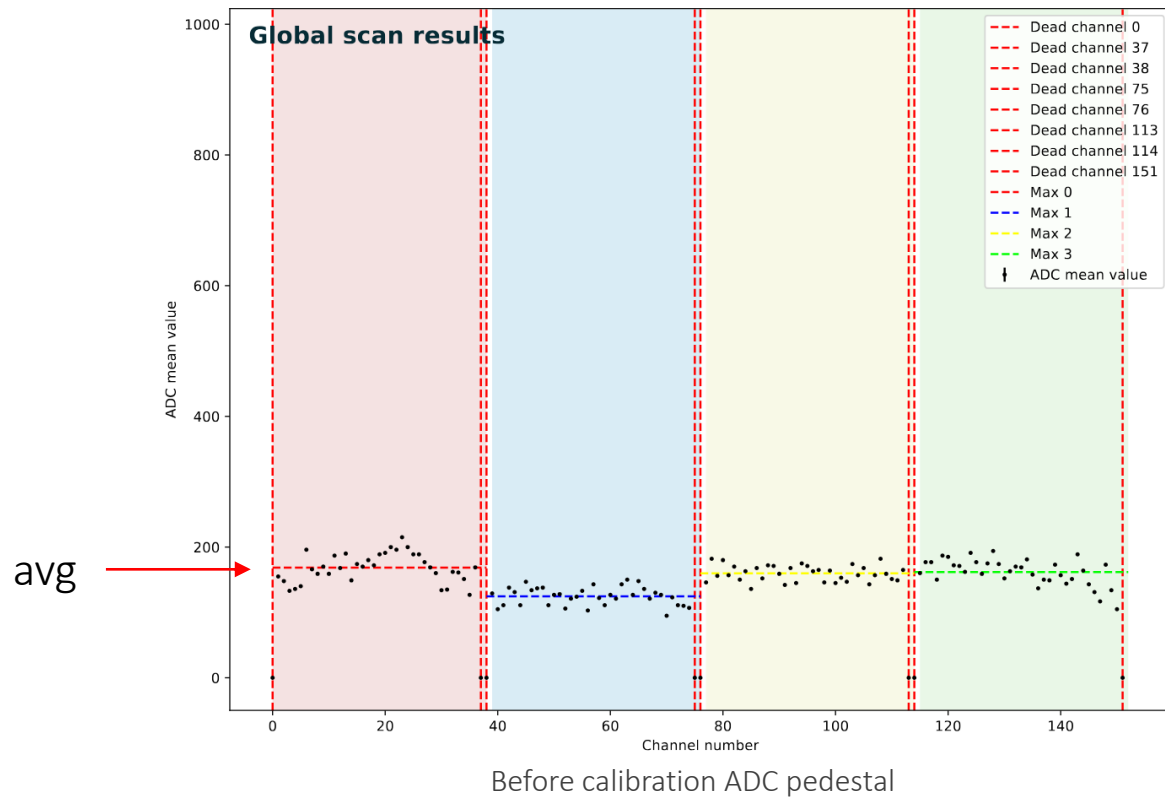
CC: Current conveyor (VFE), calibration SiPM gain variation
PA: Preamplifier
TOT: Time Over Threshold, dedicated discriminator and TDC (50ps), 12 bit
TOA: Time Of Arrival, dedicated discriminator and TDC (24ps), 12 bit
SH: Shaper
ADC: 10bit 40MHz SARADC

□ : Triplicated

H2GCalib_3B – ADC pedestal calibration

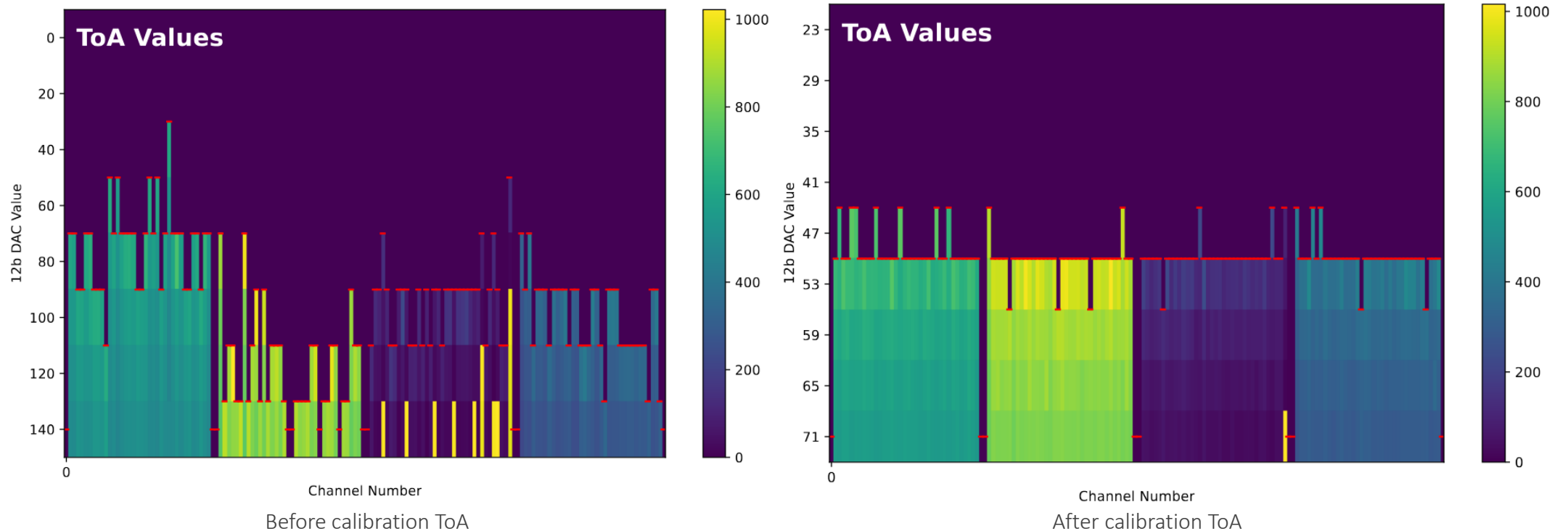
◇ This program try to get the best pedestal value, it start from config “default_2024Aug_config.json”

◇ python 005_PedestalCalib.py



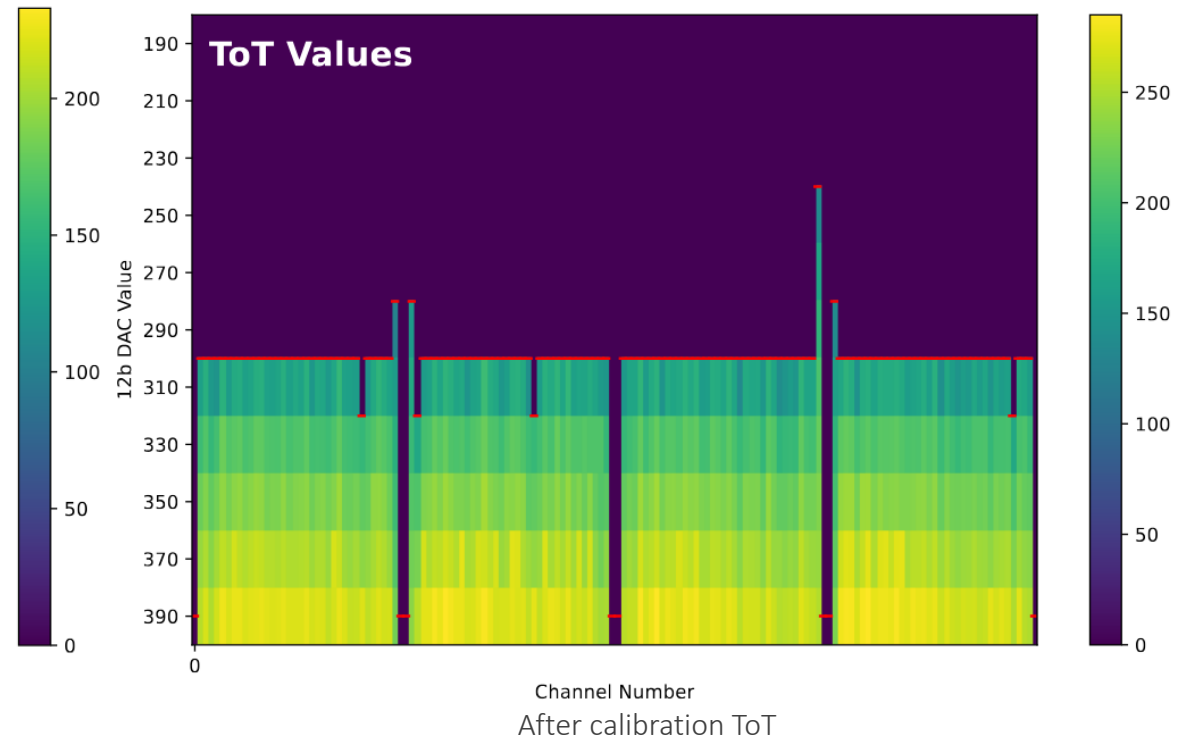
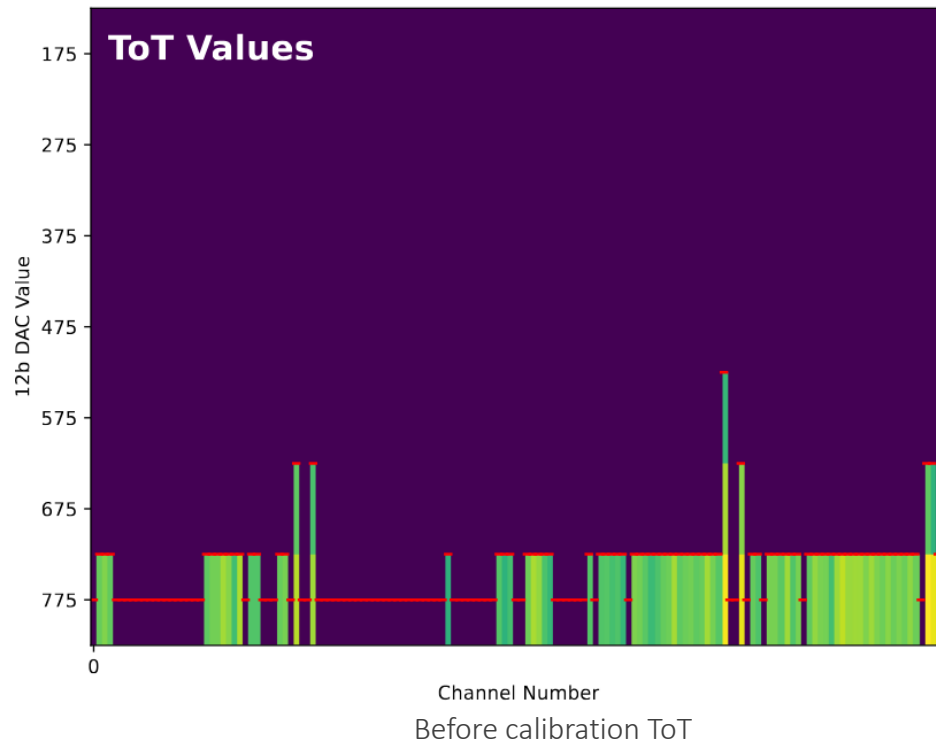
H2GCalib_3B – ToA Calibration

◇ `python 006_ToACalib.py -t 50 -i
dump/005_PedestalCalib_data_20250625_135655/config_pede_a0_20250625_135817.json,dum
p/005_PedestalCalib_data_20250625_135655/config_pede_a1_20250625_135817.json`



H2GCalib_3B – ToT Calibration

◇ python 010_ToTCalib.py -t 300 -i
dump/006_ToACalib_data_20250625_143708/config_toa_a0_20250625_151028.json,dump/006_
ToACalib_data_20250625_143708/config_toa_a1_20250625_151028.json



Operation Procedure - Config

◇ H2GConfig

- ◇ The GUI can read the configuration file and display it graphically. It allow you to modify register bit by bit
- ◇ It can upload configuration to the ASIC
- ◇ There is also a Ping FPGA button for you to test the ethernet connection

The screenshot displays the H2GConfig application window. On the left, a sidebar contains three modes: Robot Mode, Human Mode, and Calibration. The main area is divided into several sections: Top Register, Global Analog Registers, Reference Voltage Registers, Master TDC Registers, Digital Half Registers, and Channel Wise Registers. Each section contains a list of registers with corresponding buttons to view their content. On the right, there are three panels: Current Config, Register Selection, and Config File Info. The Current Config panel shows FPGA selection (FPGA 0) and ASIC selection (ASIC 0). The Register Selection panel has checkboxes for 'Use half-wise registers' (unchecked) and 'Use channel-wise registers' (checked). The Config File Info panel shows the file path 'D:/workspace/h2gc/H2GConfig/config_tot_a0_20250618_221027.json' and a 'Synced to File' button. Below these panels are buttons for 'Load', 'Save', and 'Save As'. At the bottom right, there are buttons for 'Readback', 'Ping FPGA', 'Send Current ASIC Config', and 'Send All Configs'. Red circles and arrows highlight specific features: (2) points to the FPGA/ASIC selection buttons; (3) points to the 'Load' button; (4) points to the 'Send All Configs' button; and blue arrows point to the 'Ping FPGA' button (labeled 'Test network connection') and the 'Send All Configs' button (labeled 'Upload to ASIC').

2

3

4

Load configuration

Test network connection

Upload to ASIC

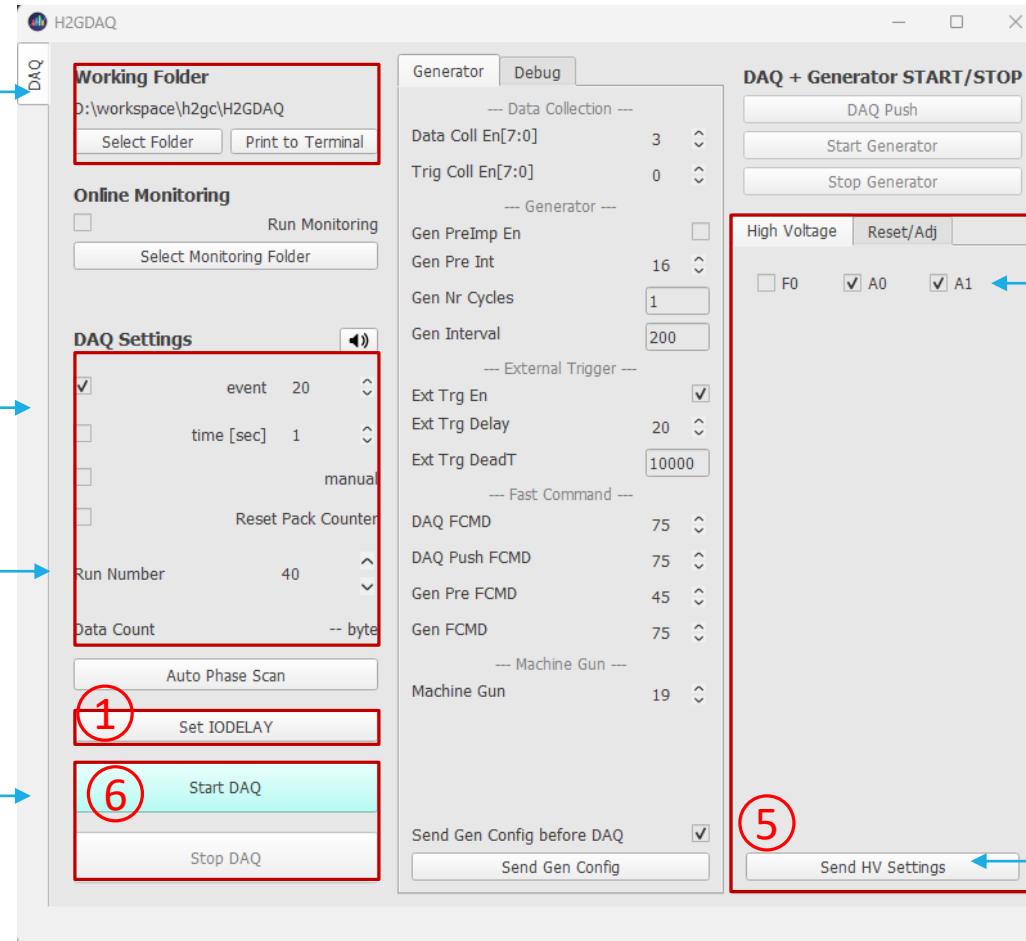
Operation Procedure - DAQ

Directory to store data

DAQ stop condition: By event count, by time or manual

Output Run040.h2g

Start/Stop DAQ button



high voltage relay setting
A0 = ASIC 0 only
A1 = ASIC1 only
F0 = ASIC0 and ASIC1 both

Send command to turn On/Off the relay base on the settings above. You also need to turn on your power supply

Operation Procedure - online_monitoring

◇ Apply 28V

ROOT online server

JSROOT version 7.9.1 19/05/2025

Hierarchy in json and xml format

☐ Monitoring

[expand all](#) | [collapse all](#) | [reload](#) | [clear](#)

ROOT

QA Plots

Spectra

FPGA Summaries

Waveform

fpga0

fpga2

fpga3

waveform_fpga_0_asic_0

waveform_fpga_0_asic_1

waveform_fpga_1_asic_0

waveform_fpga_2_asic_0

waveform_fpga_2_asic_1

waveform_fpga_3_asic_0

waveform_fpga_3_asic_1

DAQ Performance

EEEMCal

16 Individual

16 Parallel

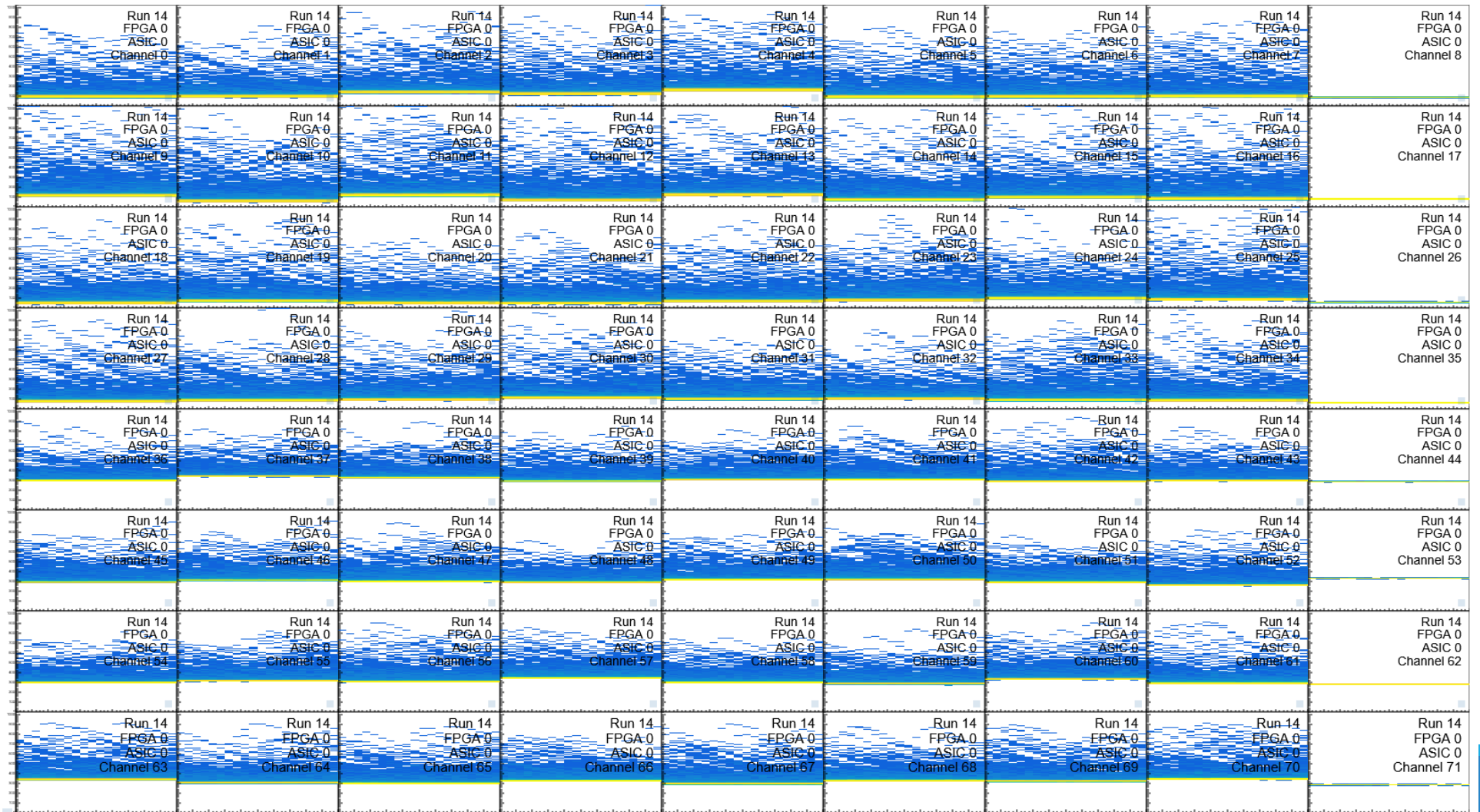
4x4 Readout

Clear_Histograms

```
$ cd ~/workspace/h2g_online_monitoring; make
```

```
$ export DATA_DIRECTORY=~/workspace/H2GDAQ; export MONITORING_PORT=12345
```

```
$ root -q -b -x -l RunMonitoring.c((RunNumber\))
```

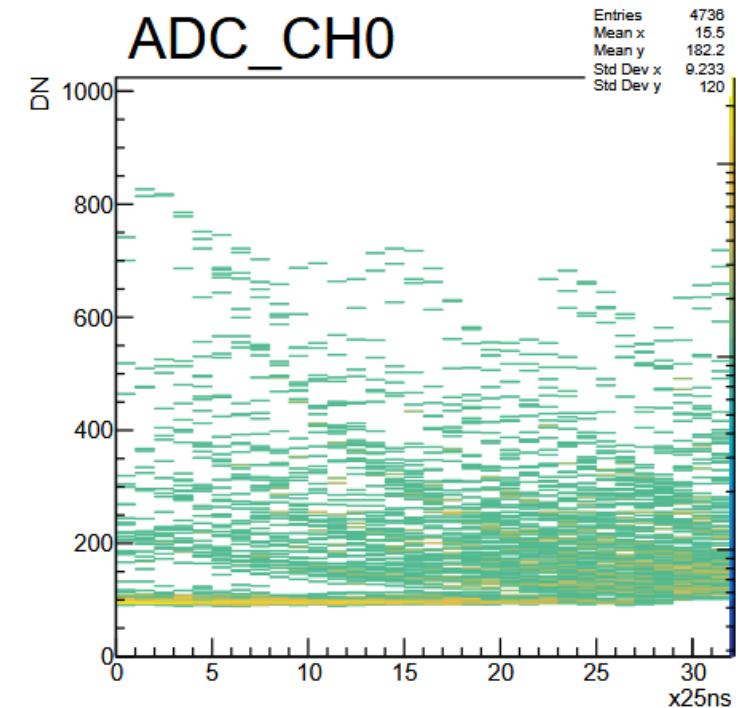


Operation Procedure - decode

- ◆ Convert raw data to root file for future analysis.

```
$ ./build/h2g_run -r 14 -d 0 -n 1
$ root
Tfile f("Run014.root")
root [1] events->Print()
*****
*Tree   :events   : Events
*Entries :    98258 : Total =    7360953537 bytes File Size =    492028194 *
*        :         : Tree compression factor =    14.96
*****
*Br    0 :event_number : event_number/i
*Entries :    98258 : Total Size=    395183 bytes File Size =    138994 *
*Baskets :     18 : Basket Size=    51200 bytes Compression=    2.84 *
*.....*
*Br    1 :timestamps : timestamps[1]/i
*Entries :    98258 : Total Size=    395145 bytes File Size =    114179 *
*Baskets :     18 : Basket Size=    51200 bytes Compression=    3.45 *
*.....*
*Br    2 :num_samples : num_samples/i
*Entries :    98258 : Total Size=    395161 bytes File Size =     4019 *
*Baskets :     18 : Basket Size=    51200 bytes Compression=   98.15 *
*.....*
*Br    3 :adc         : adc[144][32]/i
*Entries :    98258 : Total Size=  1811620311 bytes File Size =   408563585 *
*Baskets :    5745 : Basket Size=   7088128 bytes Compression=    4.43 *
*.....*
*Br    4 :toa         : toa[144][32]/i
*Entries :    98258 : Total Size=  1811620311 bytes File Size =   22647543 *
*Baskets :    5745 : Basket Size=   7088128 bytes Compression=   79.99 *
*.....*
*Br    5 :tot         : tot[144][32]/i
*Entries :    98258 : Total Size=  1811620311 bytes File Size =    8514786 *
*Baskets :    5745 : Basket Size=   7088128 bytes Compression=  212.75 *
*.....*
*Br    6 :hamming     : hamming[144][32]/i
*Entries :    98258 : Total Size=  1811643307 bytes File Size =    8529147 *
*Baskets :    5745 : Basket Size=   7089664 bytes Compression=  212.39 *
*.....*
*Br    7 :hit_max     : hit_max[144]/i
*Entries :    98258 : Total Size=    56630819 bytes File Size =   21343750 *
*Baskets :     353 : Basket Size=    221184 bytes Compression=    2.65 *
*.....*
*Br    8 :hit_pedestal : hit_pedestal[144]/i
*Entries :    98258 : Total Size=    56632604 bytes File Size =   22016214 *
*Baskets :     353 : Basket Size=    221696 bytes Compression=    2.57 *
*.....*
* 2026/1/30
```

ADC waveform
x-axis: time
y-axis: amplitude



Status

- ✓ Test under FPGA firmware V4.11 - V4.12
- ✓ Set up the testing environment and prepare the software and hardware in parallel.
- ✓ Tested ASIC calibration, apply high voltage to SiPM and run data acquisition.
- ✓ Studied the DAQ program, data format. Decode and plotting the waveform has been tested.
- ◇ Next studies:
 - ◇ internal trigger, LED injection, SiPM calibration, gain...
 - ◇ ASIC parameters...

Q/A

◇ WWW