LGADs in US

DC-LGAD for HL-LHC
AC-LGADs at EIC
- eRD112 for EIC R&D

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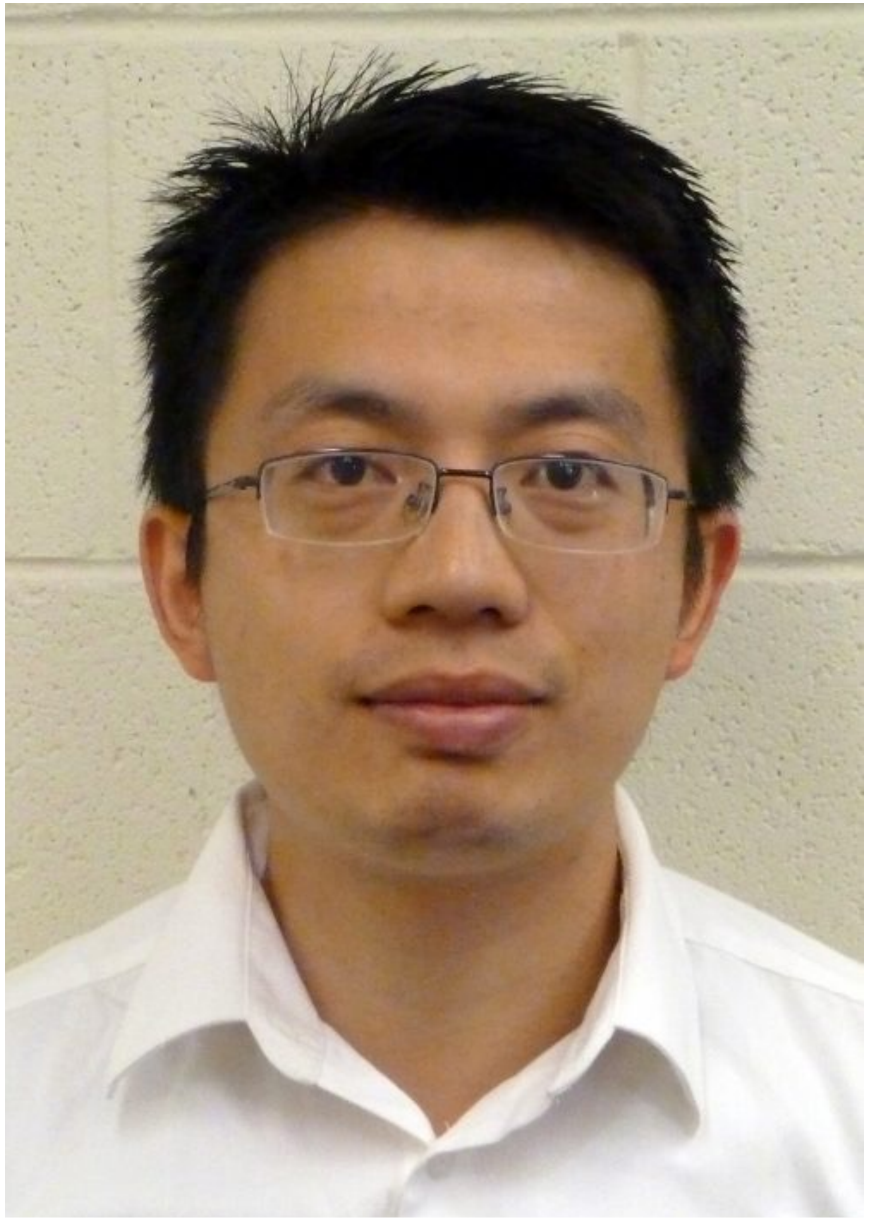
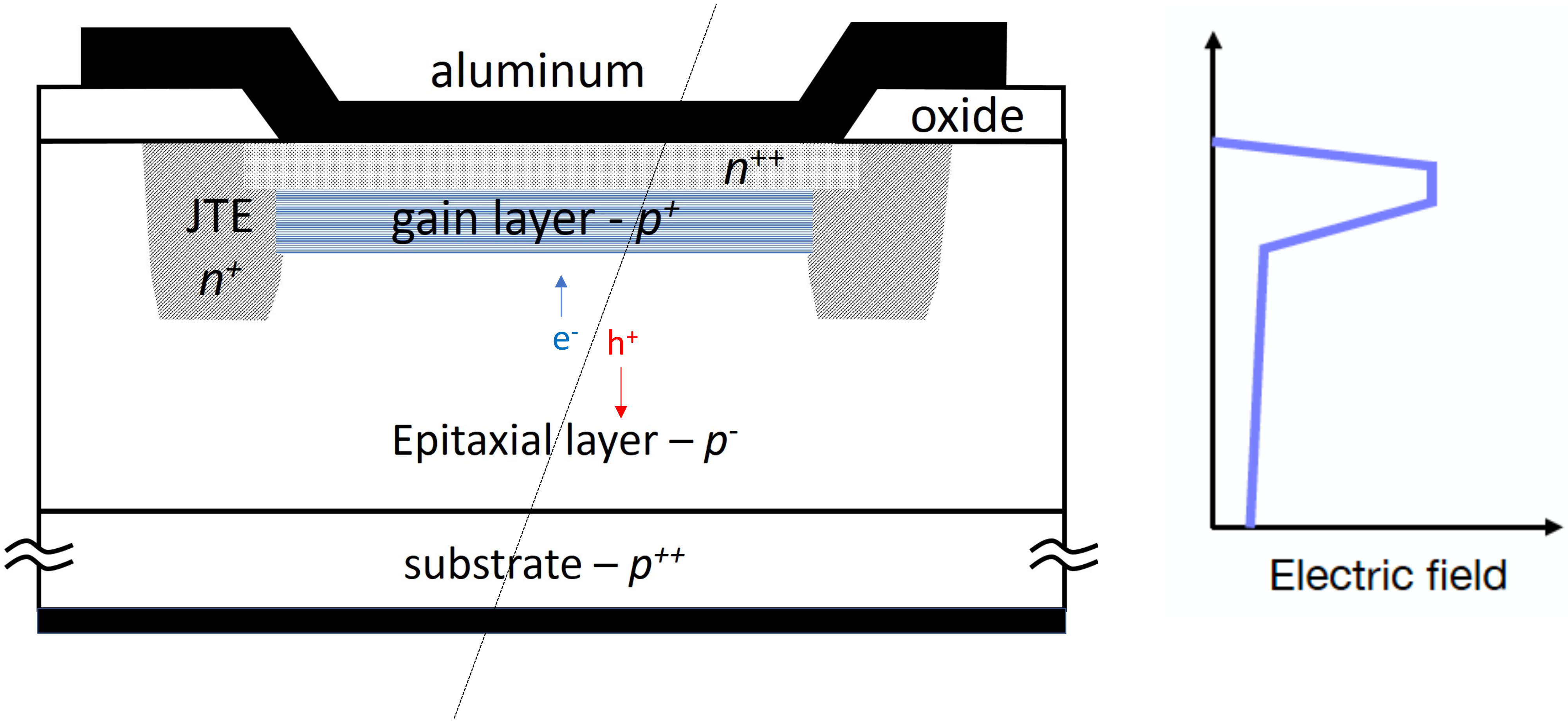
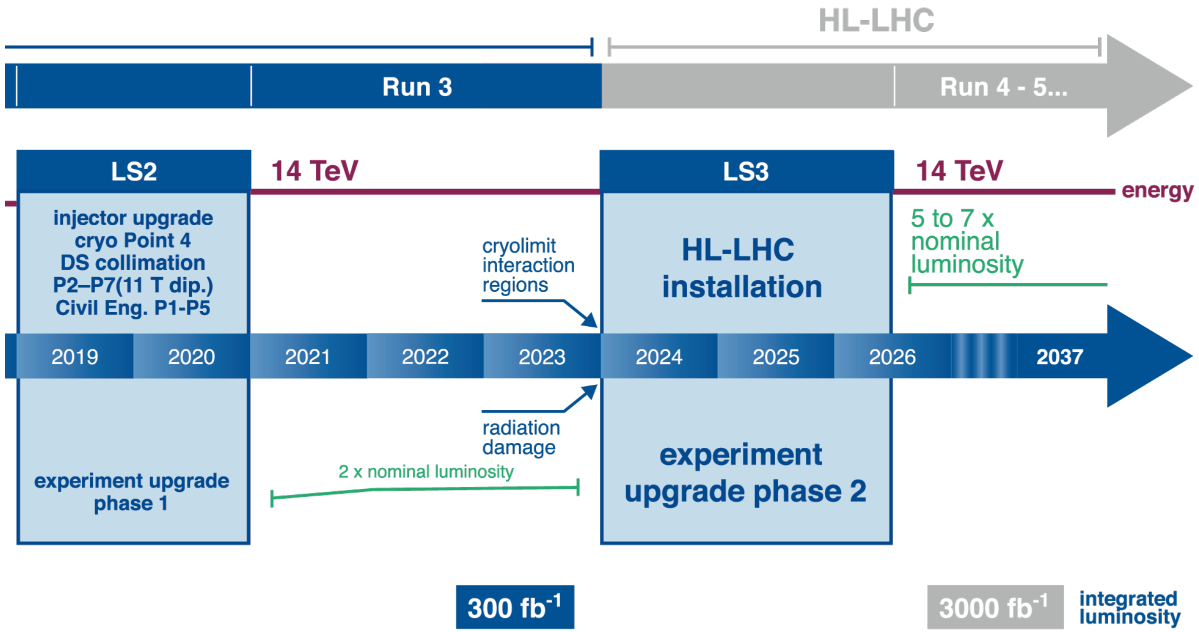


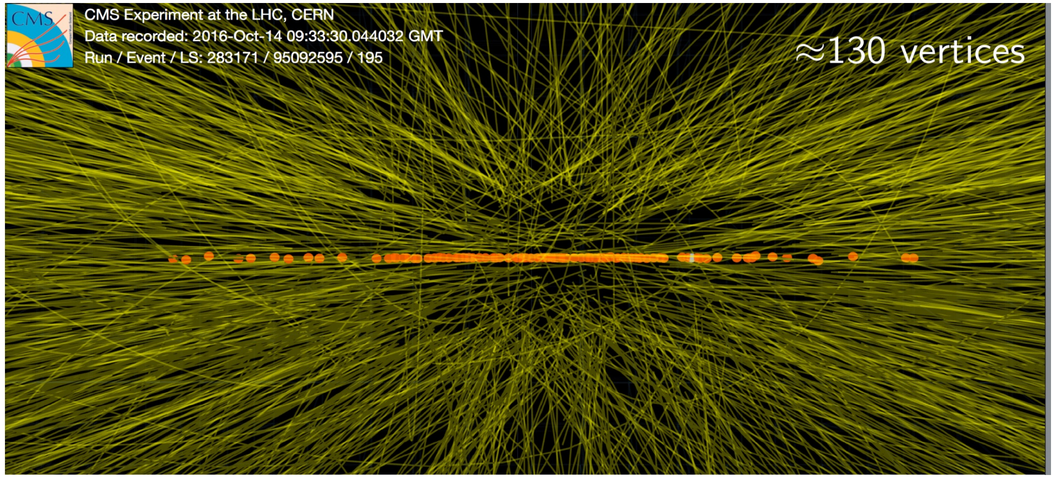
Low Gain Avalanche Detector (LGAD)

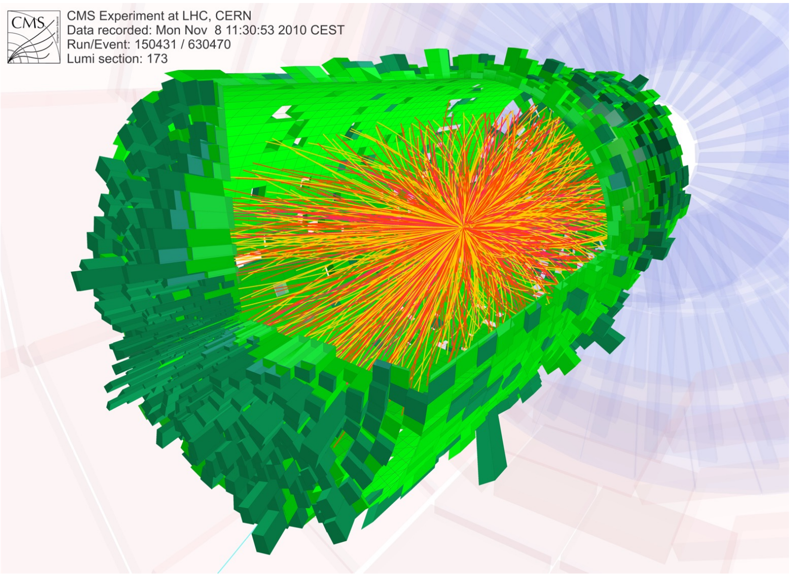


Ultra-fast silicon detectors with a highly doped p+ gain layer
Moderate internal gain : 10-30

High Luminosity LHC Era

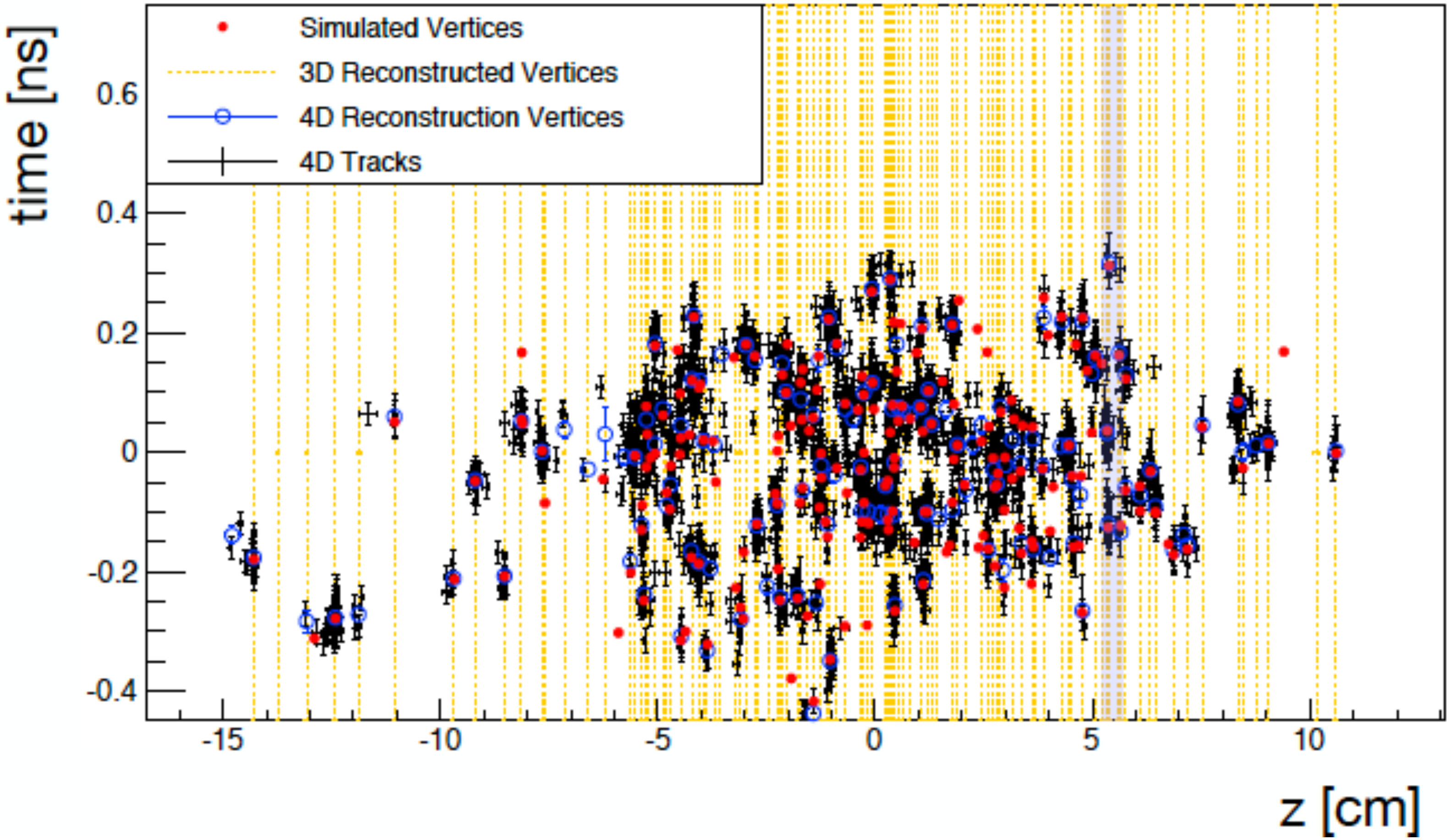






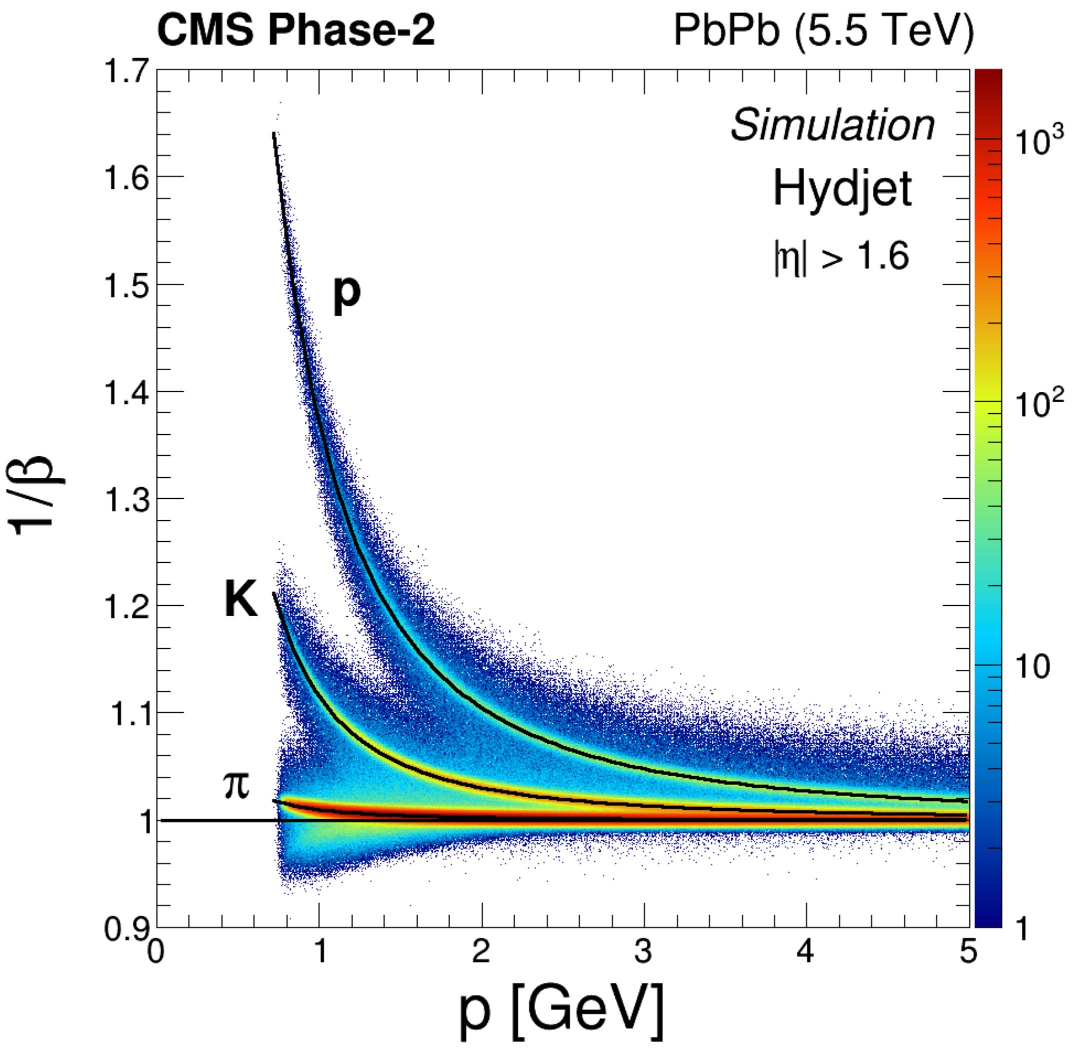
- **Dealing with the effects of pileup interactions in pp collisions will be a major challenge of the HL-LHC era.**
- **Sharping the tools for new discoveries as well as better measurement precision.**

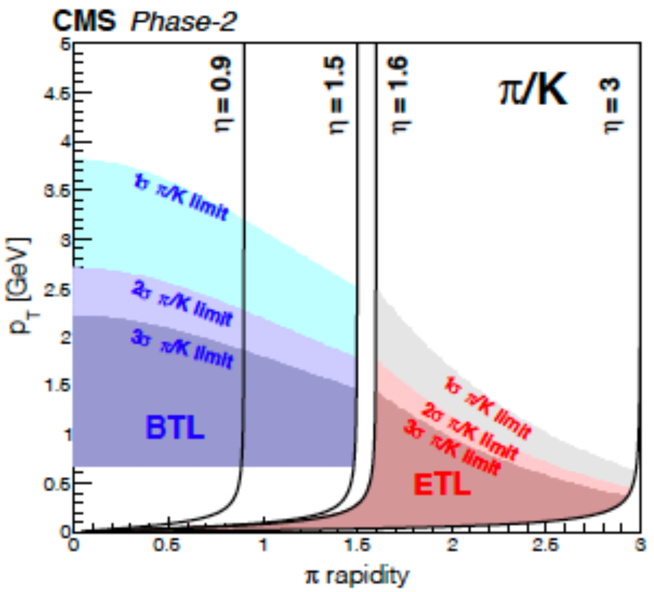
Precise Timing for HL-LHC

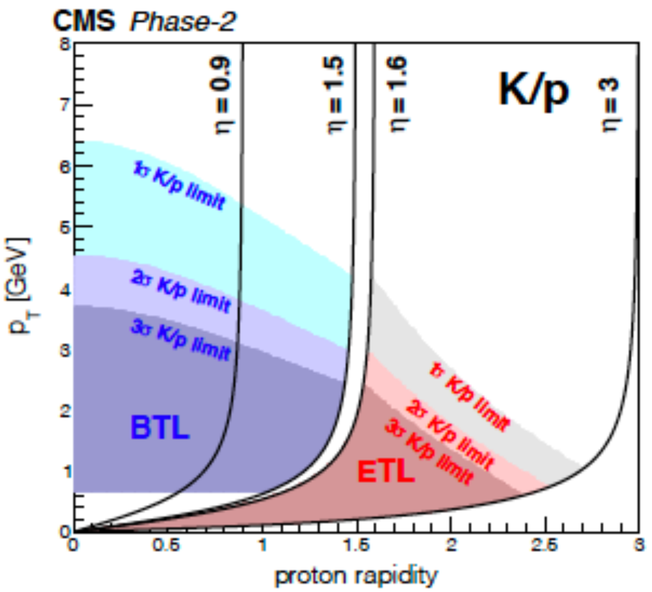


- PU interactions significantly overlap in space but are more separable in space + time.
- Per-particle timing allows 4D track and vertex reconstruction
  - PU reduced in each time slice; every object reconstruction is improved
  - Significant benefit to CMS pp physics program

Precise Timing for CMS Heavy Ion Physics







- **Precise timing provides particle ID for low p_T hadrons and thus new physics capabilities for Heavy Ion Physics.**
- **The CMS MTD will offer unique opportunity because of its excellent timing resolution and wide rapidity coverage.**

CMS Phase-2 Upgrades for HL-LHC (2028+)

Trigger/HLT/DAQ &

- Track information in L1-Trigger
- L1-Trigger: 12.5 ms latency – output 750 kHz
- HLT output 7.5 kHz

Barrel ECAL/HCAL

- Replace FE/BE electronics
- Lower ECAL operating temp. (8 °C)

Muon Systems

- Replace DT & CSC FE/BE Electronics
- Complete RPC coverage in region $1.5<h<2.4$
- Muon tagging $2.4<h<3$

New Endcap Calorimeters

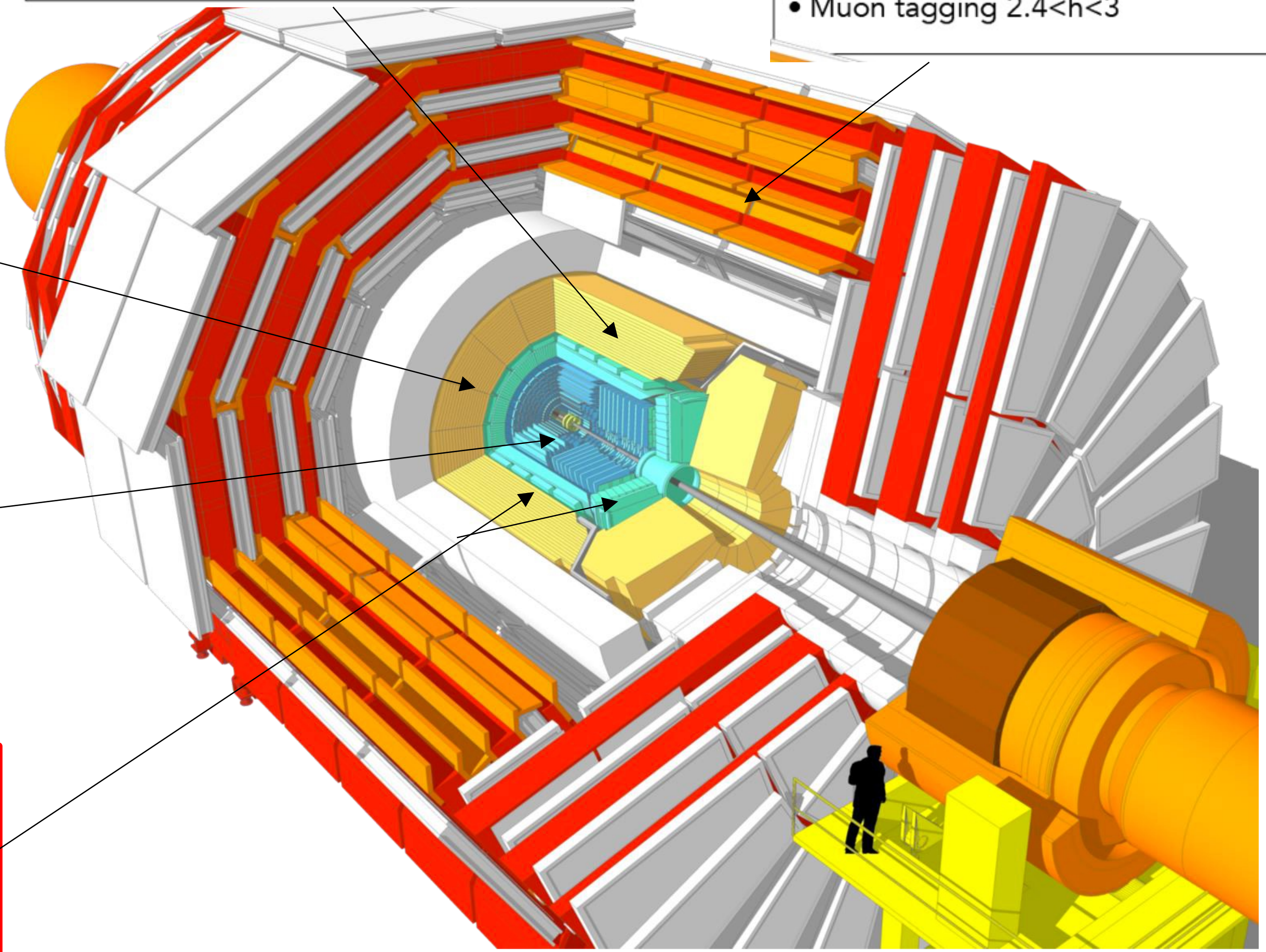
- Rad. tolerant – high granularity
- 3D capable

New Tracker

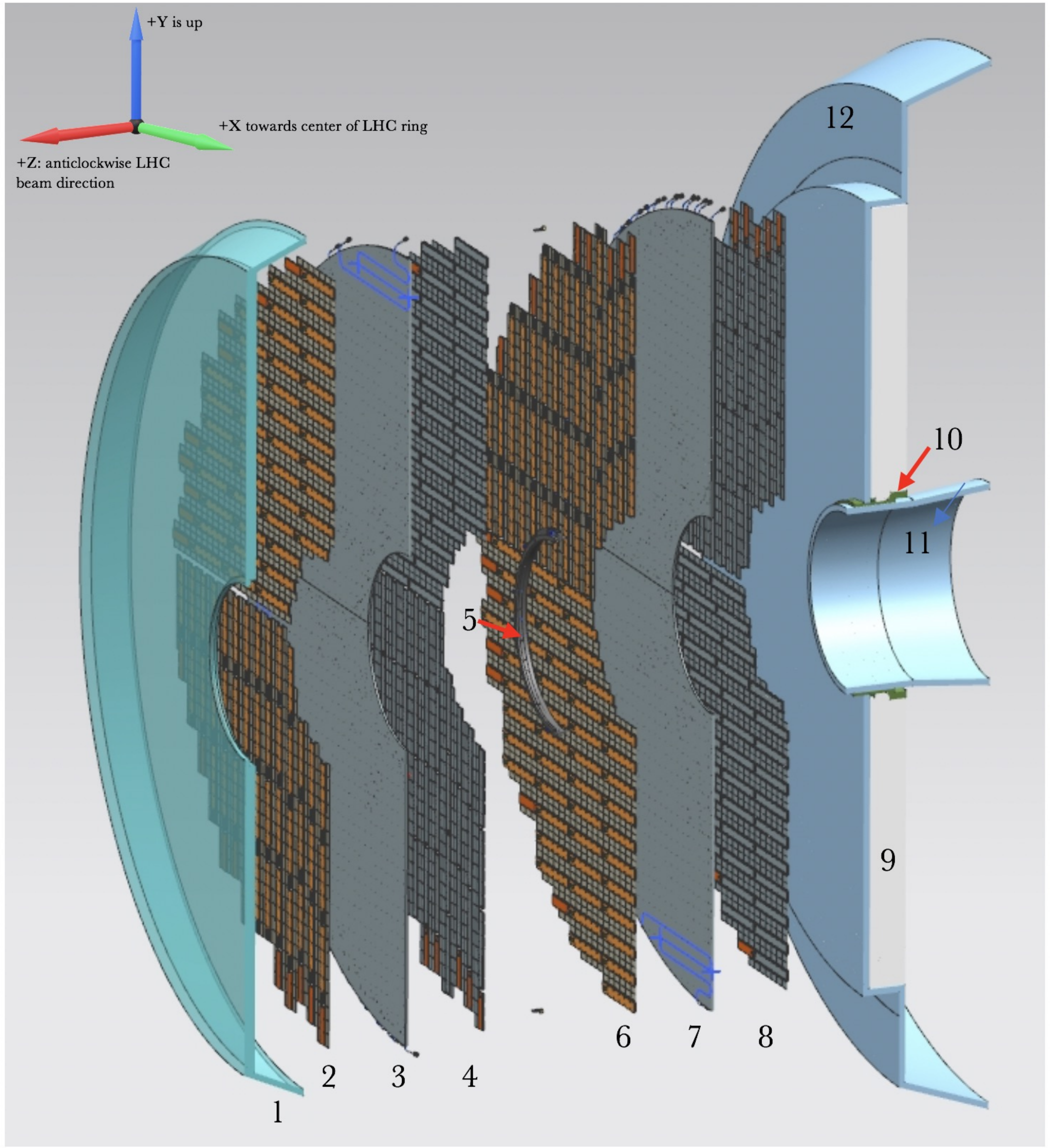
- Rad. tolerant – high granularity – significant less material
- 40 MHz selective readout (pT>2 GeV) in Outer Tracker for L1 -Trigger
- Extended coverage to h=4

MIP Precision Timing Detector

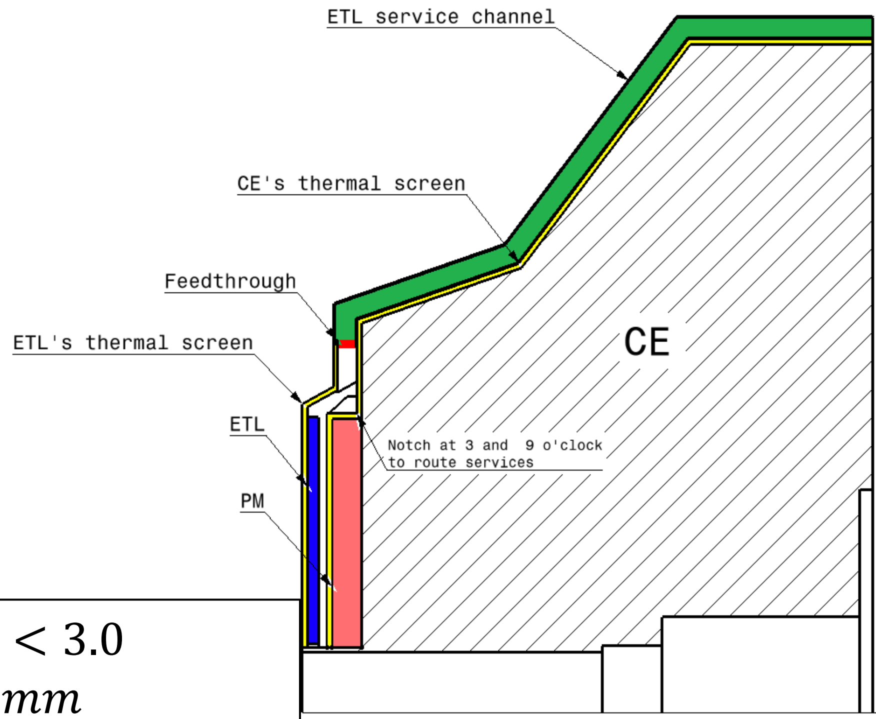
- Barrel: Crystal +SiPM
- Endcap: Low Gain Avalanche Diodes



CMS MTD - Endcap Timing Layer



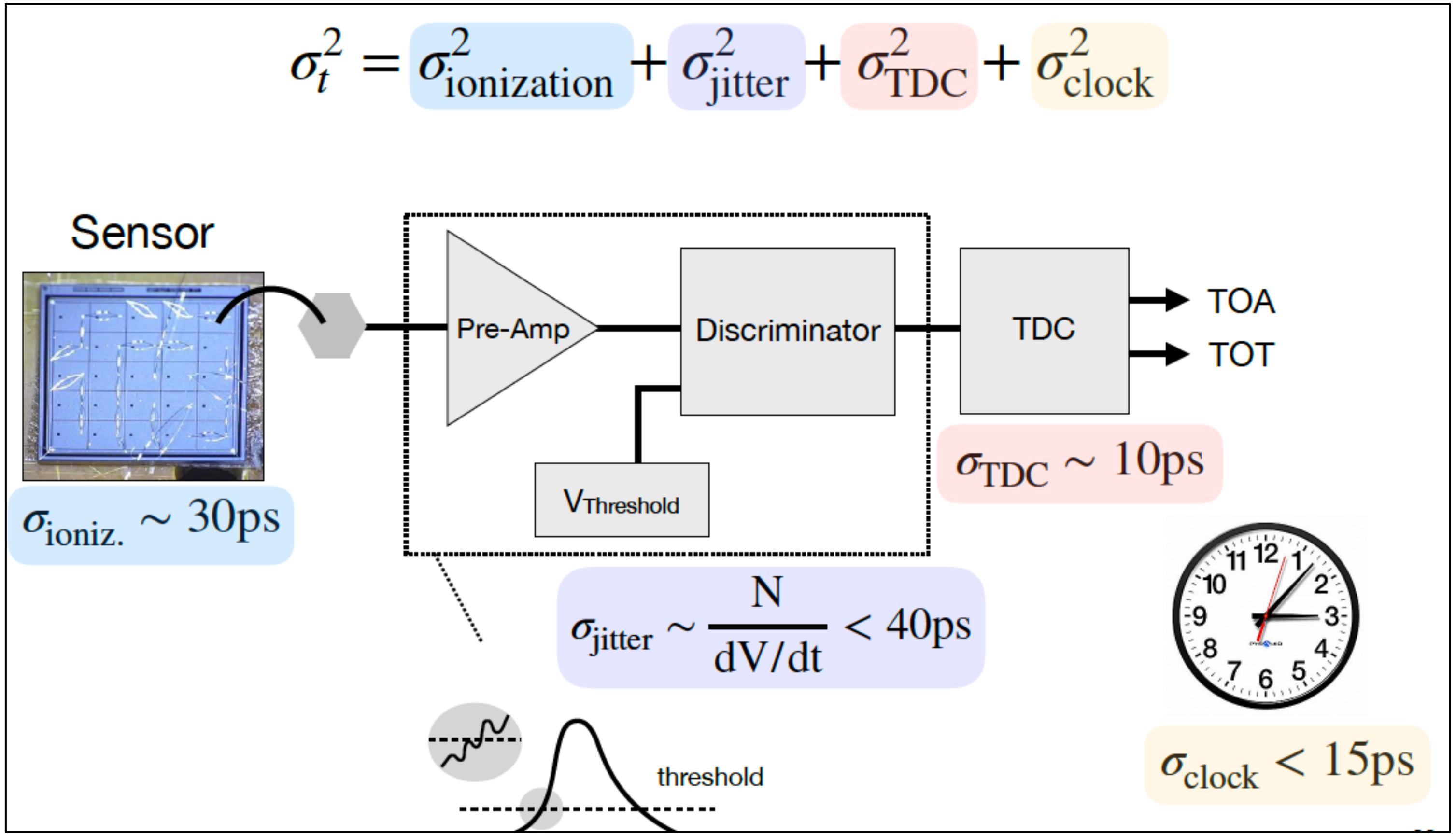
1: ETL Thermal Screen
2: Disk 1, Face 1
3: Disk 1 Support Plate
4: Disk 1, Face 2
5: ETL Mounting Bracket
6: Disk 2, Face 1
7: Disk 2 Support Plate
8: Disk 2, Face 2
9: HGCal Neutron Moderator
10: ETL Support Cone
11: Support cone insulation
12: HGCal Thermal Screen



- On the CE nose: $1.6 < |\eta| < 3.0$
- Radius: $315 < R < 1200\ mm$
- Position in Z: $\pm 3.0\ m$ (45 mm thick)
- Surface ~$15.8\ m^2$; ~8.6M 1.3x1.3 mm^2
- Weight 282 kg/side; Power: 26kW/side
- CO2 cooling at –30^{o}C

- **Two disks on each side allowing up to 2 times of measurements per track**
  - **50 ps per hit → 35 ps per track**
- **Stageable, serviceable, maintainable**

CMS Endcap Timing Layer – Time Resolution

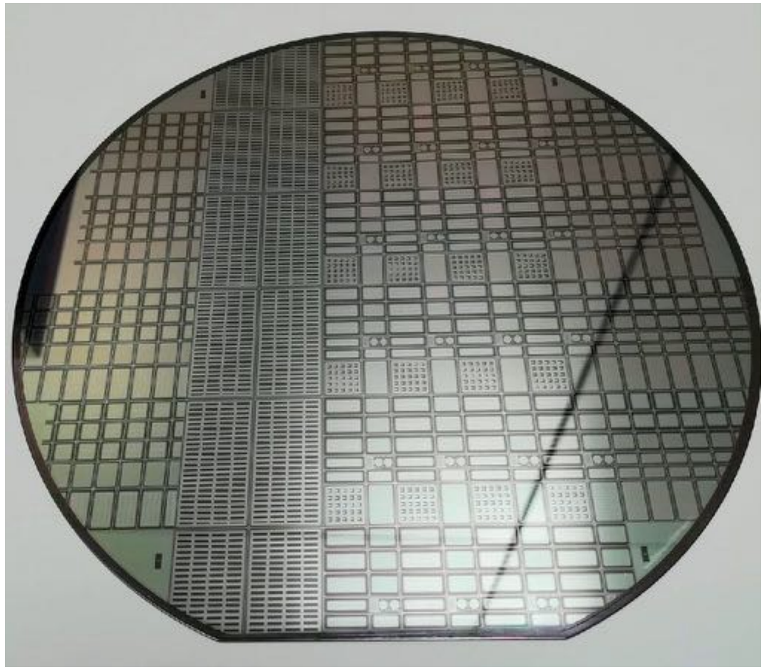


- $\sigma_{ionization}$: random variation in particle energy deposition, determining the amplitude and the shape of the signal
  ~30 ps up to 1x10^{15} n_{eq}/cm^2, and
  ~40 ps up to 2x10^{15} n_{eq}/cm^2
- σ_{jitter}: mostly due to electronics noise and depends on the amplifier slew rate (dV/dt)
  jitter <40 ps before irradiation.
  No degrading up to 100 Mrad
- σ_{TDC}: the effect of the TDC binning
- σ_{clock}: contribution from clock distribution

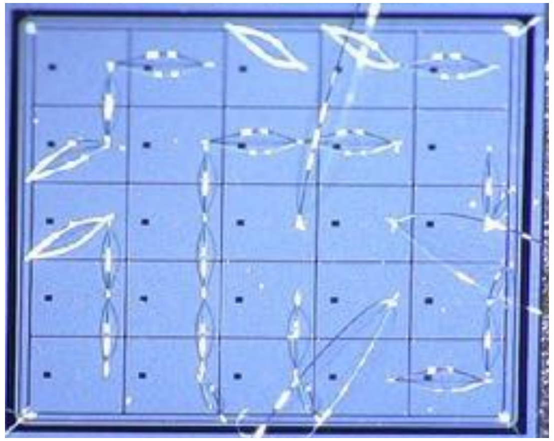
CMS Endcap Timing Layer - LGAD Sensor

Key Sensor Characteristics		
Depletion region thickness	50 μm	Minimize rise time, sufficient charge, gain uniformity
Pad size	$1.3\times1.3\ mm^2$	Minimize capacitance, Occupancy ~1%
Sensor size	$2\times2\ cm^2$ (16×16)	Optimize wafer usage
Interpad gap	$< 90\ \mu m$	Fill factor > 85%
Time resolution after irradiation	$< 40\ ps$	Up to $1.7\times10^{15}\ n_{eq}/cm^2$

FBK UFSD3

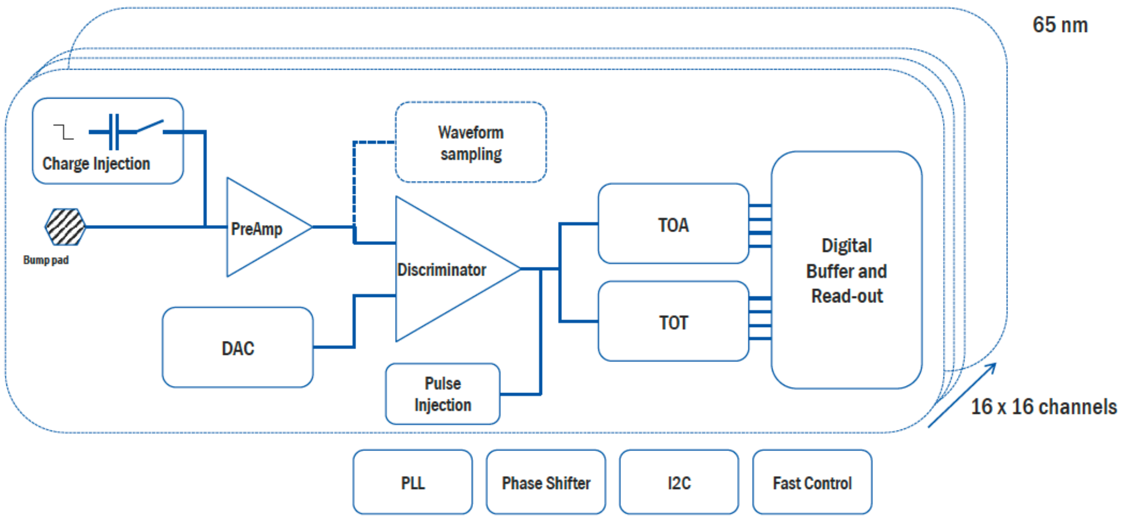


5x5 array from HPK



Recent prototypes from Hamamatsu (HPK) and Fondazione Bruno Kessler (FBK) focus on
- **improving the radiation hardness**
- **increasing fill factor**
- **large arrays**

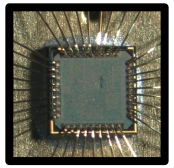
CMS Endcap Timing Layer –Readout ASIC (ETROC)

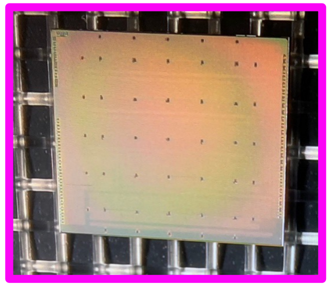


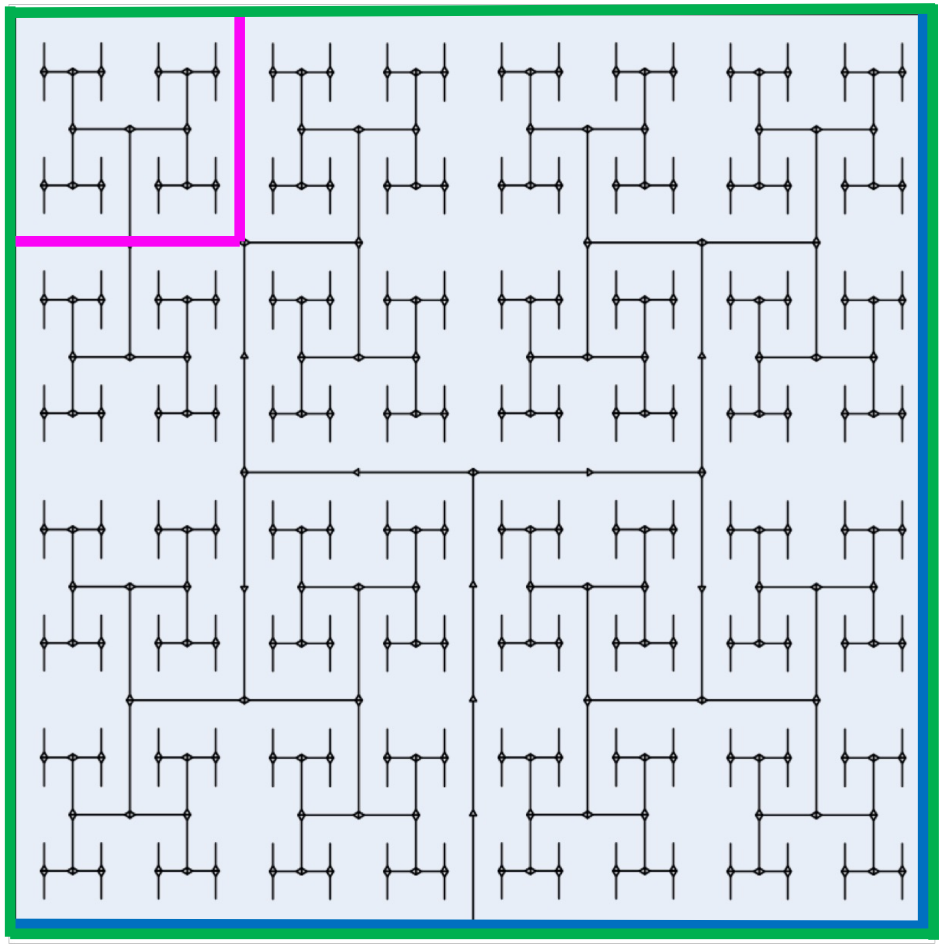
- **Dedicate balance act from:**
  - **Low noise & fast rise time**

$$\sigma_{jitter} \sim \frac{e_n C_d}{Q_{in}} \sqrt{t_{rise}} < 40\ ps$$

  - **Power budget: 1 W/chip, 4 mW/channel**
- **ETROC innovations:**
  - **Low power single TDC for both time of arrival and time over threshold measurements**
  - **Flexible low & high-power modes**

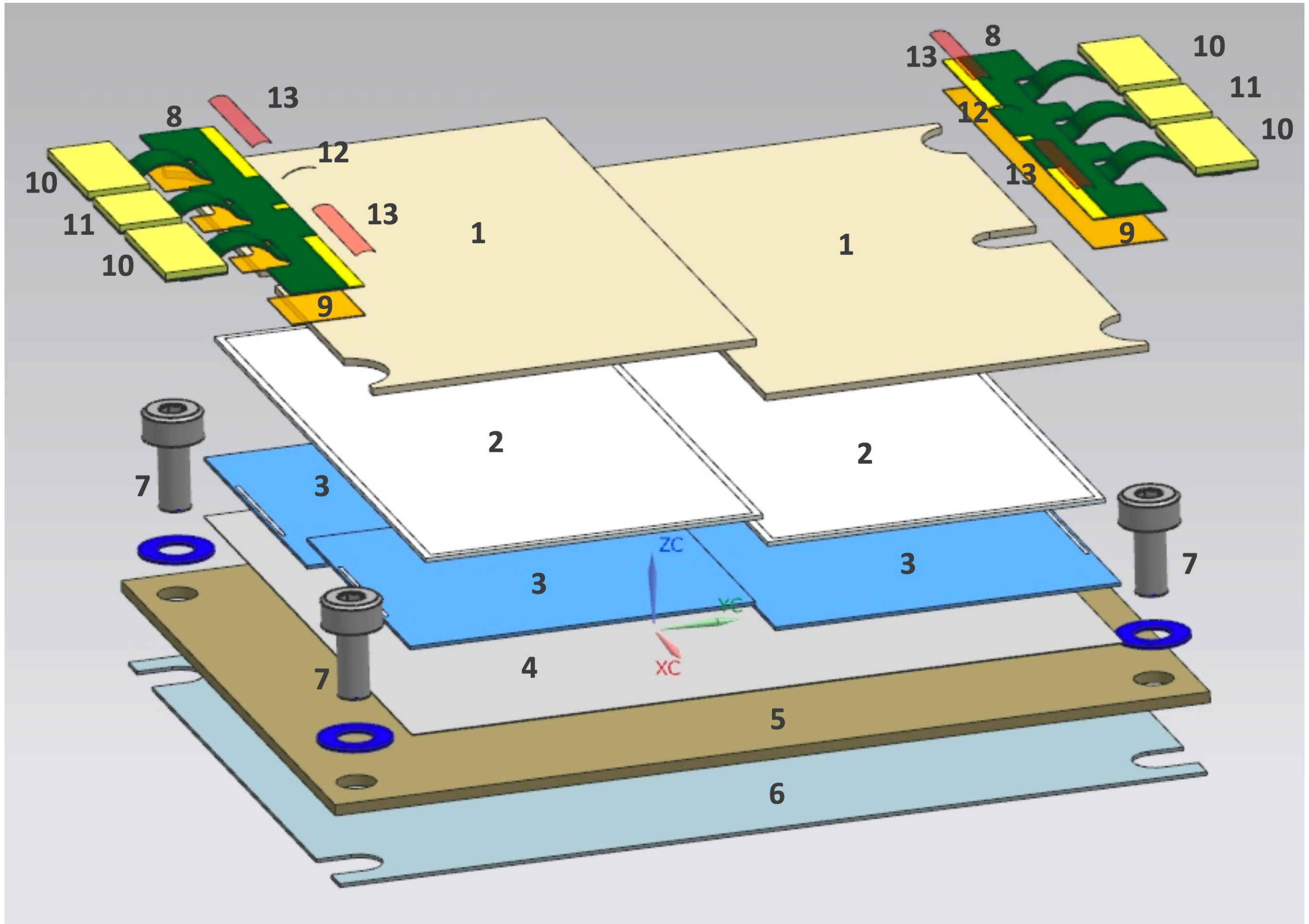






- ✓ ETROC0 : single analog channel
- ✓ ETROC1: with TDC and 4x4 clock tree
- ❑ ETROC2: 16x16 full functionality
- ❑ ETROC3: 16x16 preproduction chip

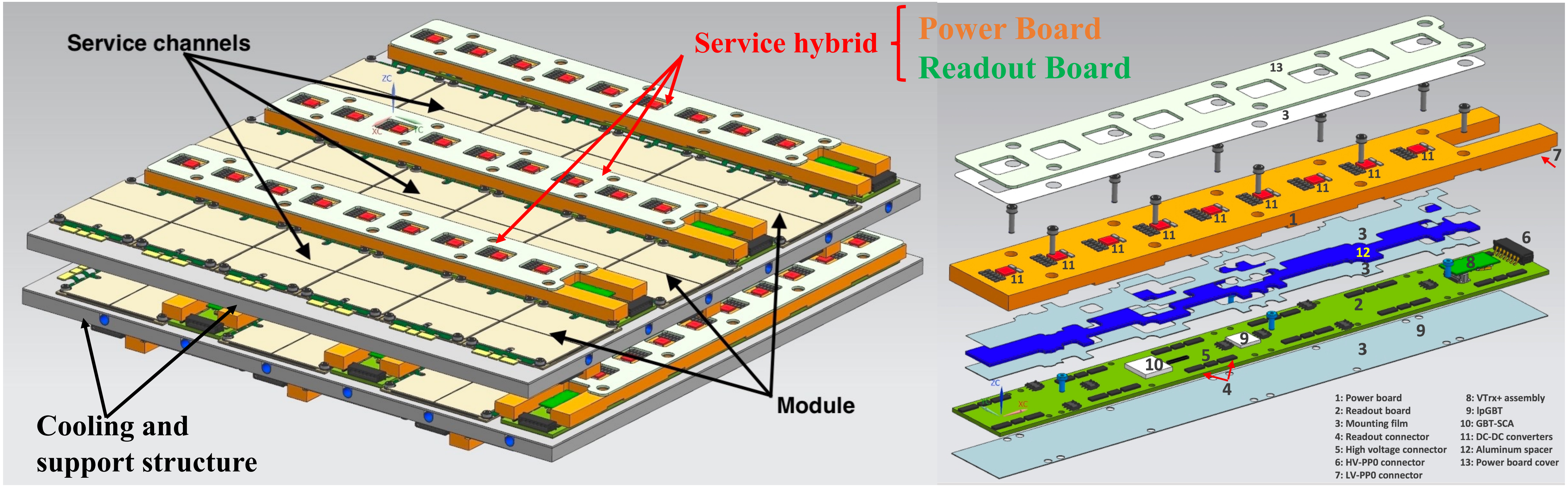
CMS Endcap Timing Layer – Module Design



1: AlN module cover
2: LGAD sensor
3: ETL ASIC
4: Mounting film
5: AlN carrier
6: Mounting film
7: Mounting screw
8: Front-end hybrid
9: Adhesive film
10: Readout connector
11: High voltage connector
12: LGAD bias voltage wirebond
13: ETROC wirebonds

ETL consists of ~9000 modules. LGAD sensors and ETROC chips are bump-bonded together and attached to AlN base plate with thermal adhesive film to make one module. Electric connection between flexible circuits and LGAD/ETROCs are made through wire-bonding.

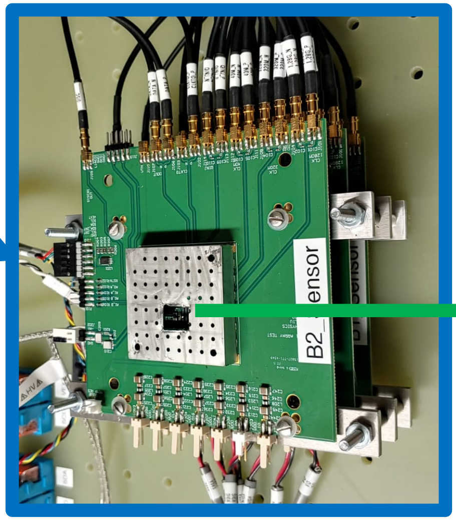
CMS Endcap Timing Layer – Service Hybrid



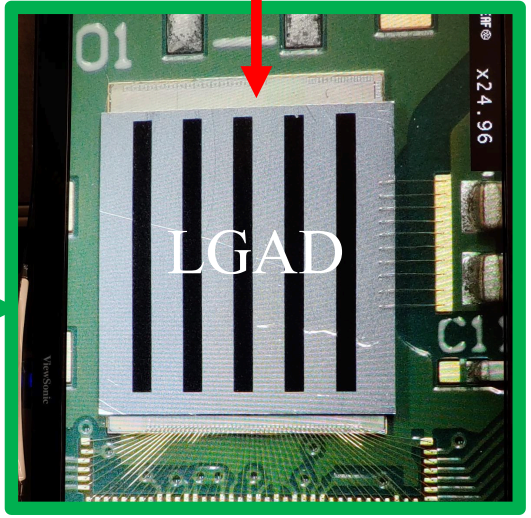
- **Service Hybrid** is an assembly of two PCBs, a Power Board and a Readout Board, servicing 12 modules.
- **Power Board** distributes low voltages provided by power supplies to ETROCs, slow control adapter chip, lpGBT, and VTRx+. The voltages are regulated by radiation hard and B-tolerant DC-DC converters on the power board.
- **Readout Board** distributes bias voltages to LGAD sensors, receives and distributes fast control signals and slow controls to ETROCs, and route data and monitoring information from ETROCs to backend DAQ.

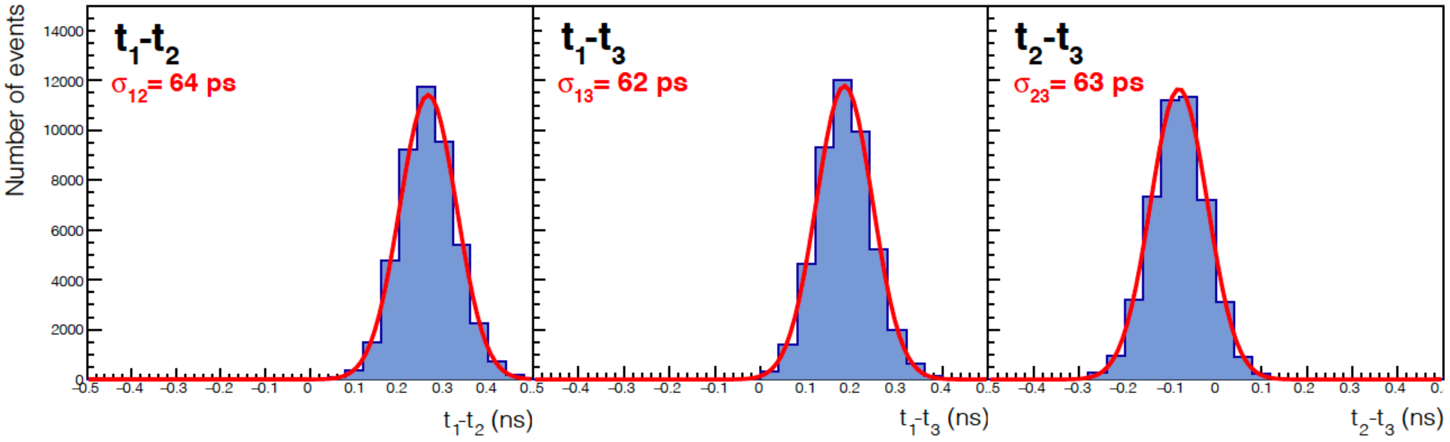
CMS ETROC1+LGAD – Test Beam Results

ETROC1 Test Board



ETROC1



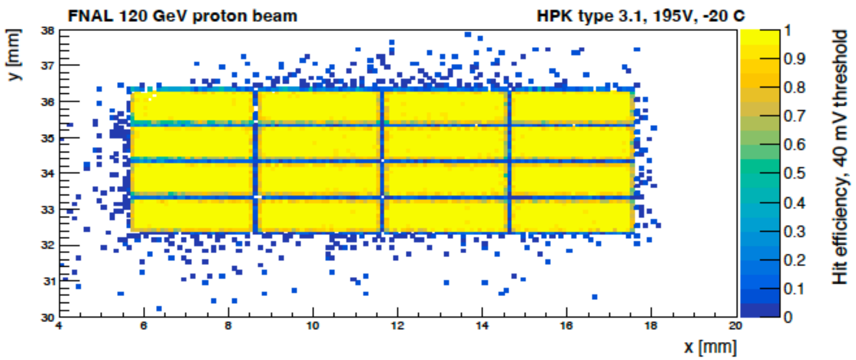


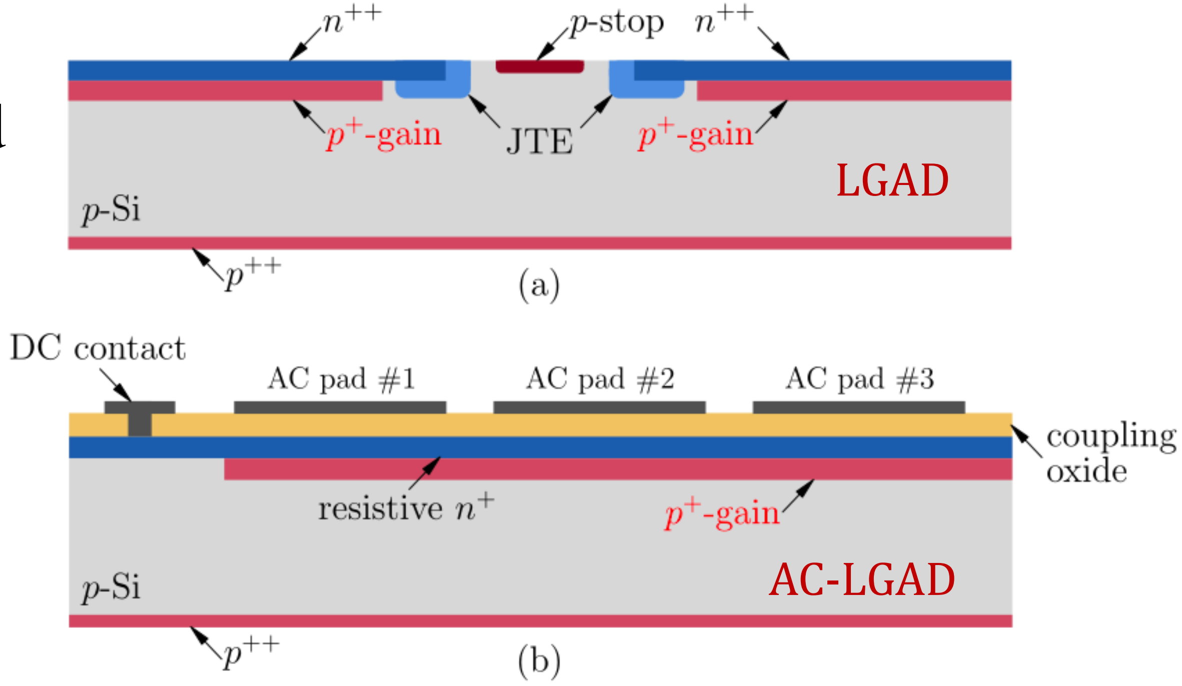
From preliminary analysis of the data from ongoing beam test at FNAL, the resolution of single LGAD+ETROC1 devices with large signal amplitude is 42-46 ps.

$$\sigma_i = \sqrt{0.5 \cdot \left(\sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2\right)}$$

AC-Coupled LGAD

- Due to the presence of JTE and the gap between LGAD cells, 100% fill factor can not be achieved in LGAD. The position resolution is limited to be $\sqrt{1/12}$ of cell size.





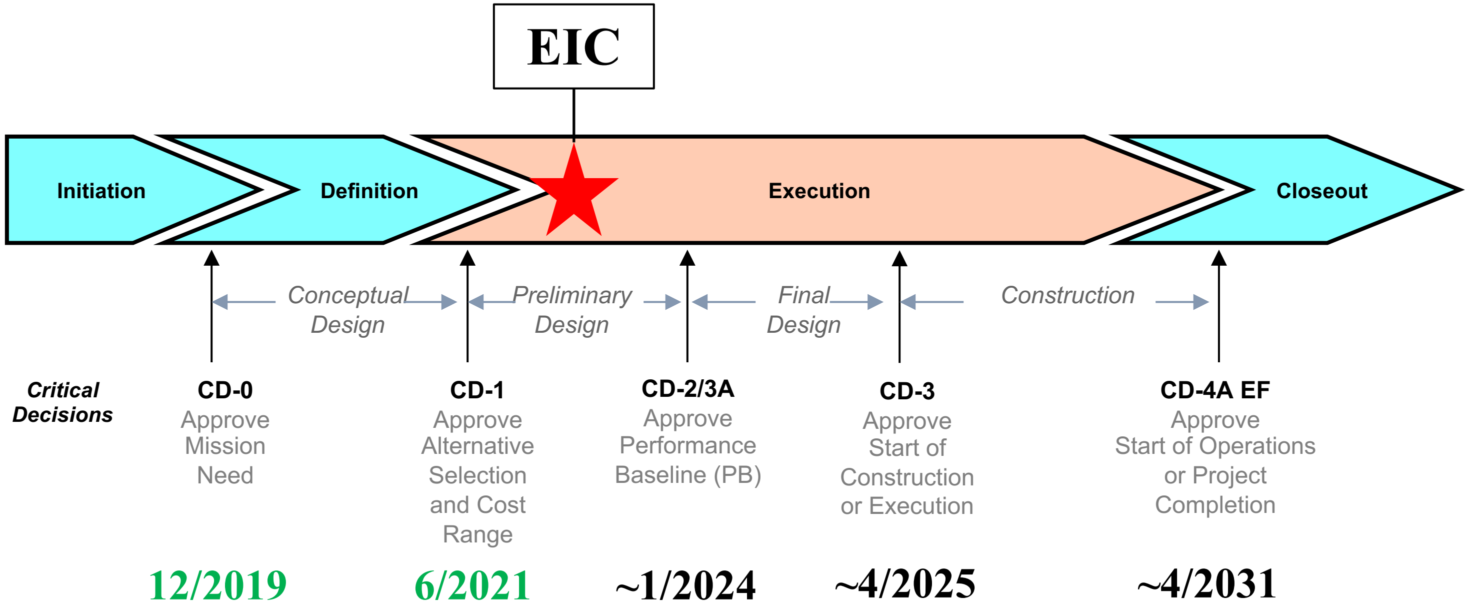
- AC-LGAD: replacement of the segmented n^{++} layer by a less doped but continuous n^{+} layer. Electrical signals in the n^{+} layer are AC-coupled to neighboring metal electrodes that are separated from the n^{+} layer by a thin insulator layer.

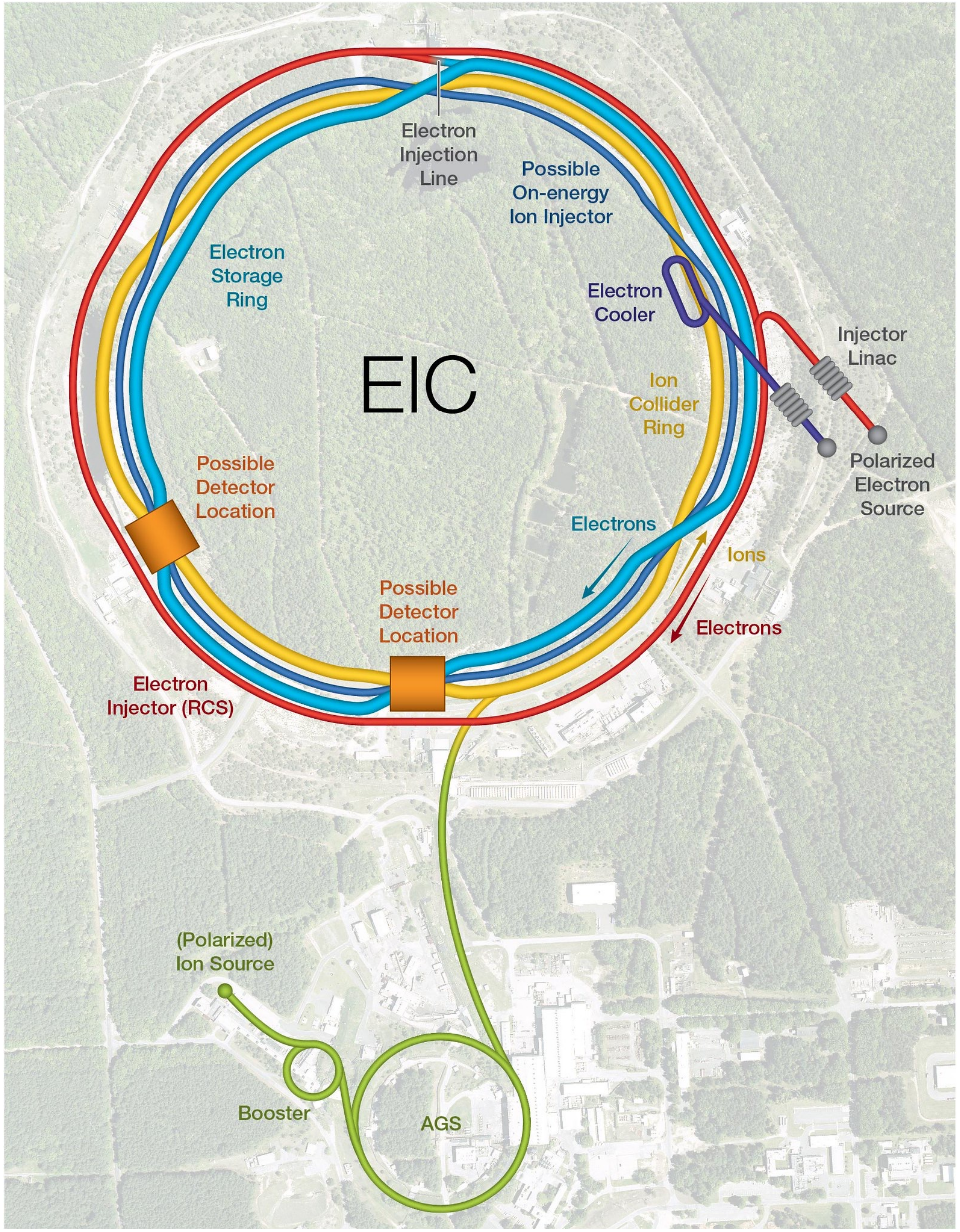
- AC-LGAD not only provides a timing resolution of a few tens of picoseconds, but also 100% fill factor and a spatial resolution that are orders of magnitude smaller than the cell size. Therefore, it is a good candidate for 4D detectors at future high energy experiments.

Electron Ion Collider (2031-)

Design Goals

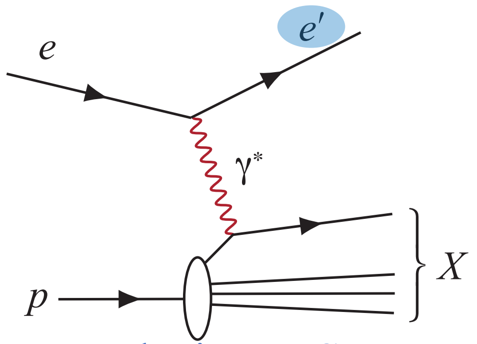
- High Luminosity: $L = 10^{33}$–10^{34} $cm^{-2}s^{-1}$, 10–100 fb^{-1}/year
- Highly Polarized Beams: ~70%
- Large Center of Mass Energy Range: E_{cm} = 20–140 GeV
- Large Ion Species Range: protons – Uranium
- Large Detector Acceptance and Good Background Conditions
- Accommodate two Interaction Regions (IR)



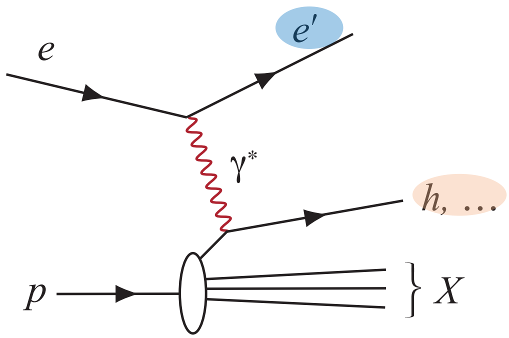


Electron Beam: 5-18 GeV **Ion: 40, 100-275 GeV**

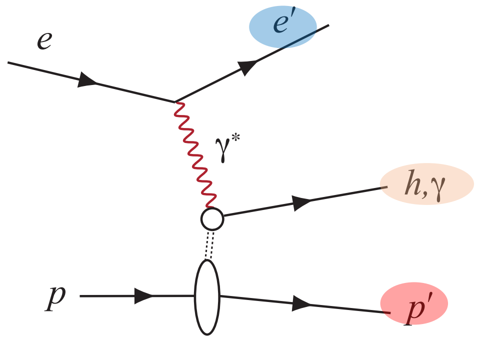
EIC Detectors



Inclusive DIS



Semi-inclusive DIS



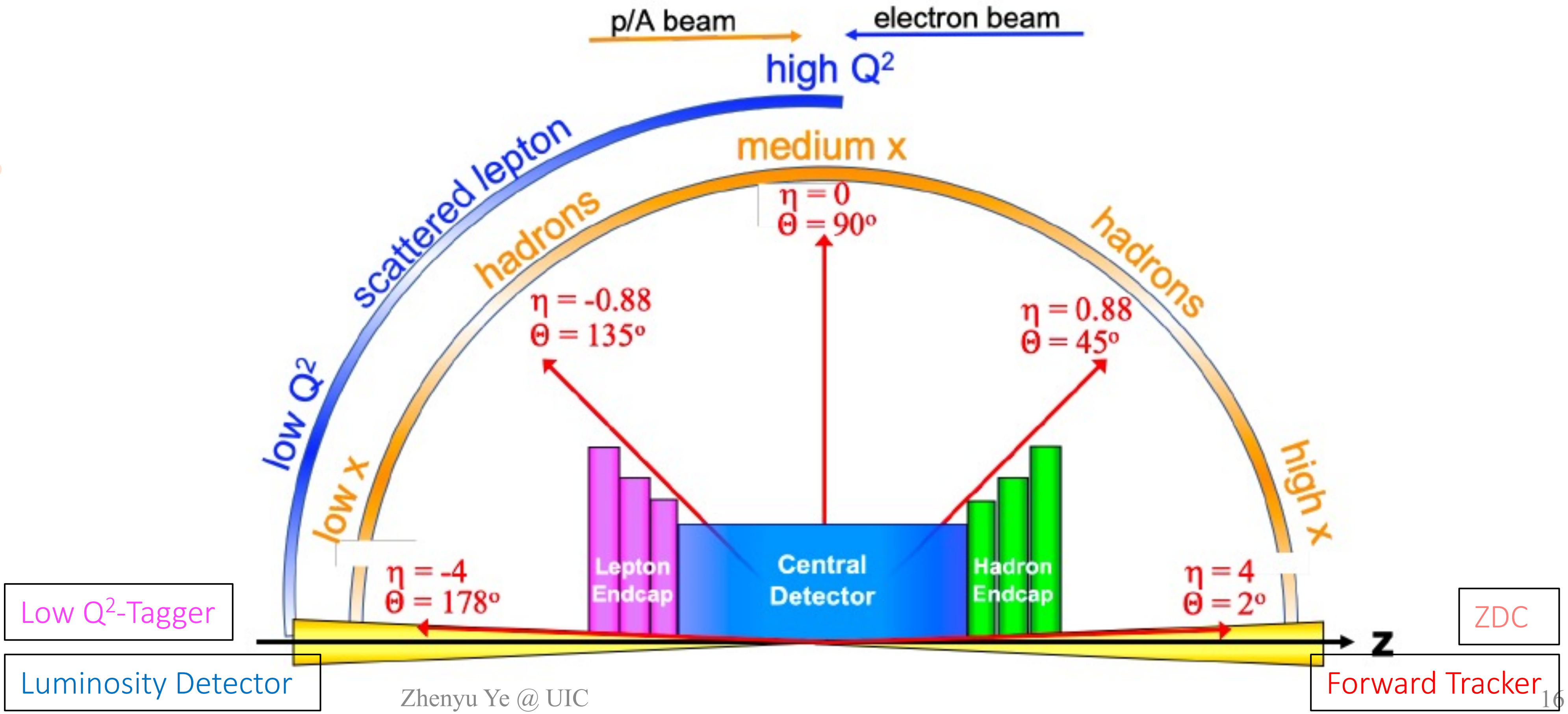
Exclusive

Detector-1 (project detector)

- IP6 (25 mrad crossing angle with crabbing)
- Addresses EIC science program as outlined in the EIC white paper and NAS report
- Ready for Day-1 operations in ~2031
- Working towards pre-TDR/CD-2

Detector-2 (strong comm. interests)

- IP8 (35 mrad crossing angle)
- Complementary to Detector-1
- Require development of 2nd IR
- Ready 2-5 years after Detector-1
- Development at WG level



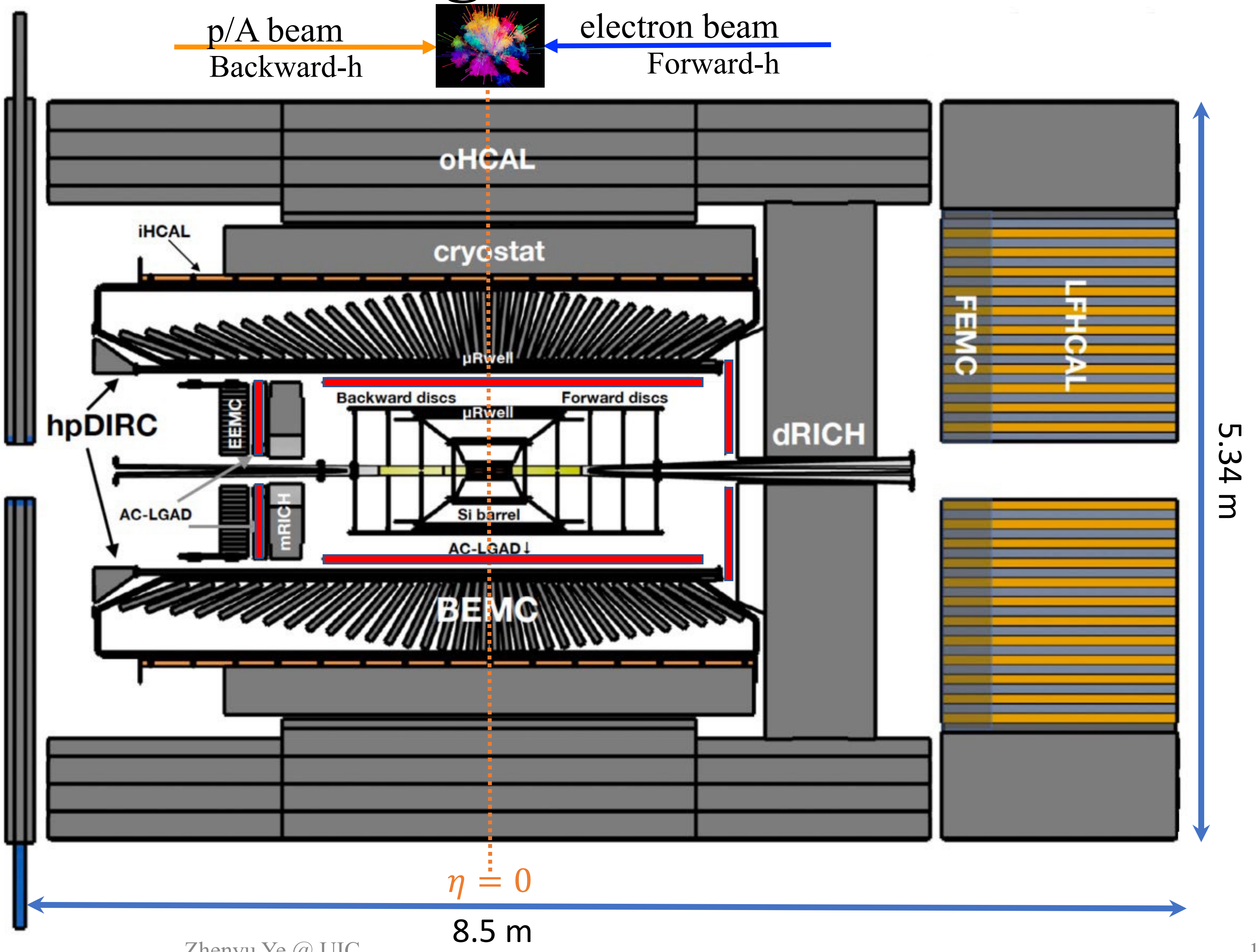
EIC Detector-1 Reference Design

Tracking:
- Si MAPS
- AC-LGAD (~30 μm)
- μRWELL

PID:
- hp-DIRC
- mRICH
- dRICH
- AC-LGAD (~25 ps)

Calorimetry:
- SciGlass Barrel EMCal
- PbWO EEMCal
- Longitudinally separated EM+Hcal
- Inner HCal (instrumented frame)
- Outer HCal (sPHENIX re-use)

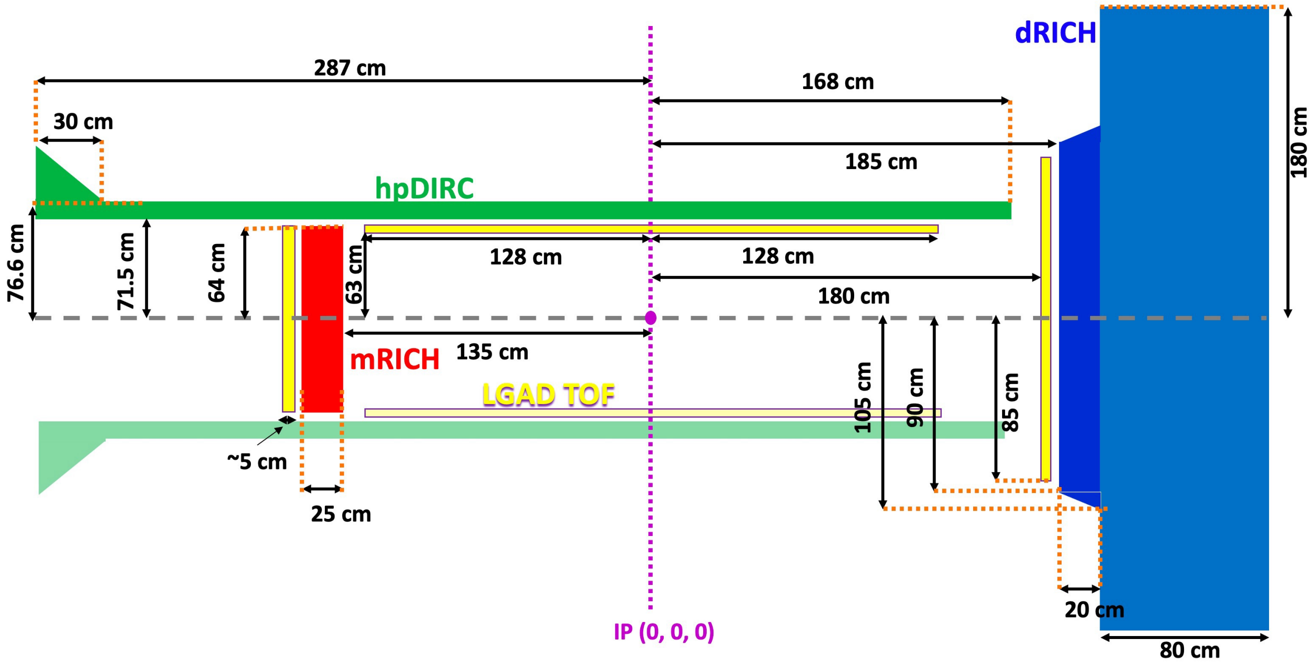
Different to LHC
- lower momentum
- lower occupancy
- less irradiation

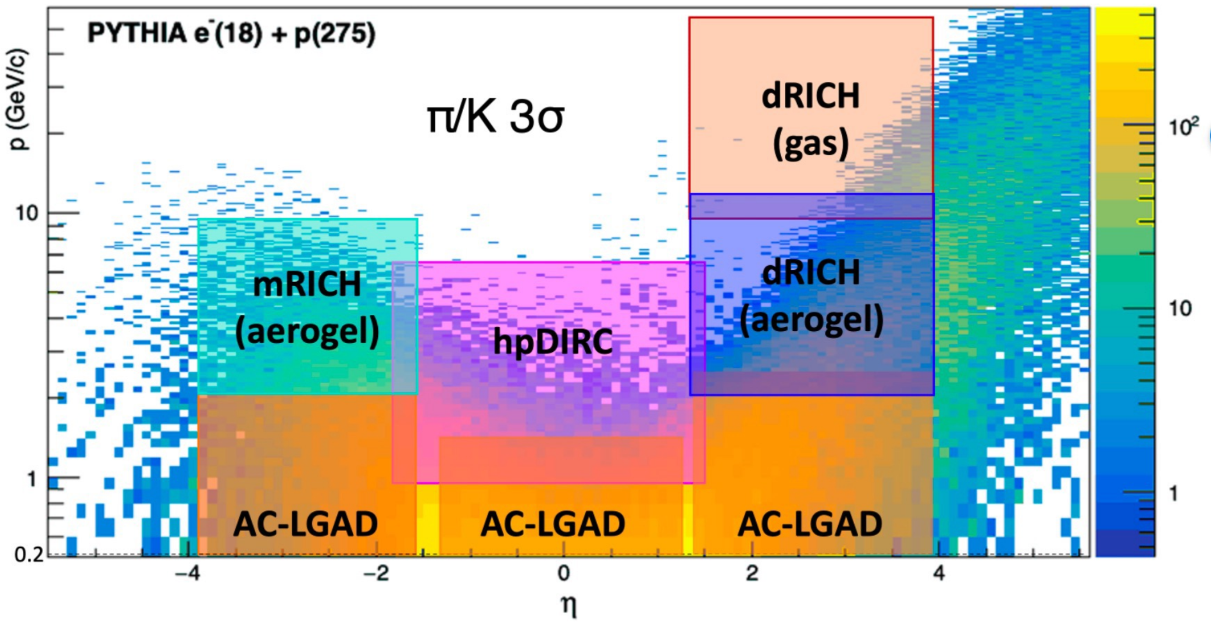


AC-LGADs in Central Detector: TOF PID + Tracking

Explore **AC-LGAD** technology and leverage established LHC **DC-LGAD** detector designs to minimize cost and risk

- **Time-of-flight for e/π/K/p identification** at low-to-intermediate momentum range
- Provide a **high spatial resolution point for tracking**





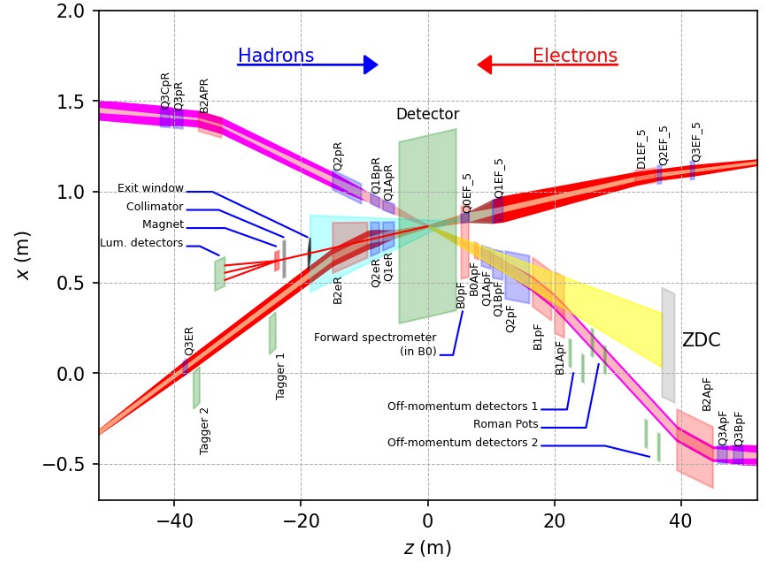
Reference Design (optimization ongoing)

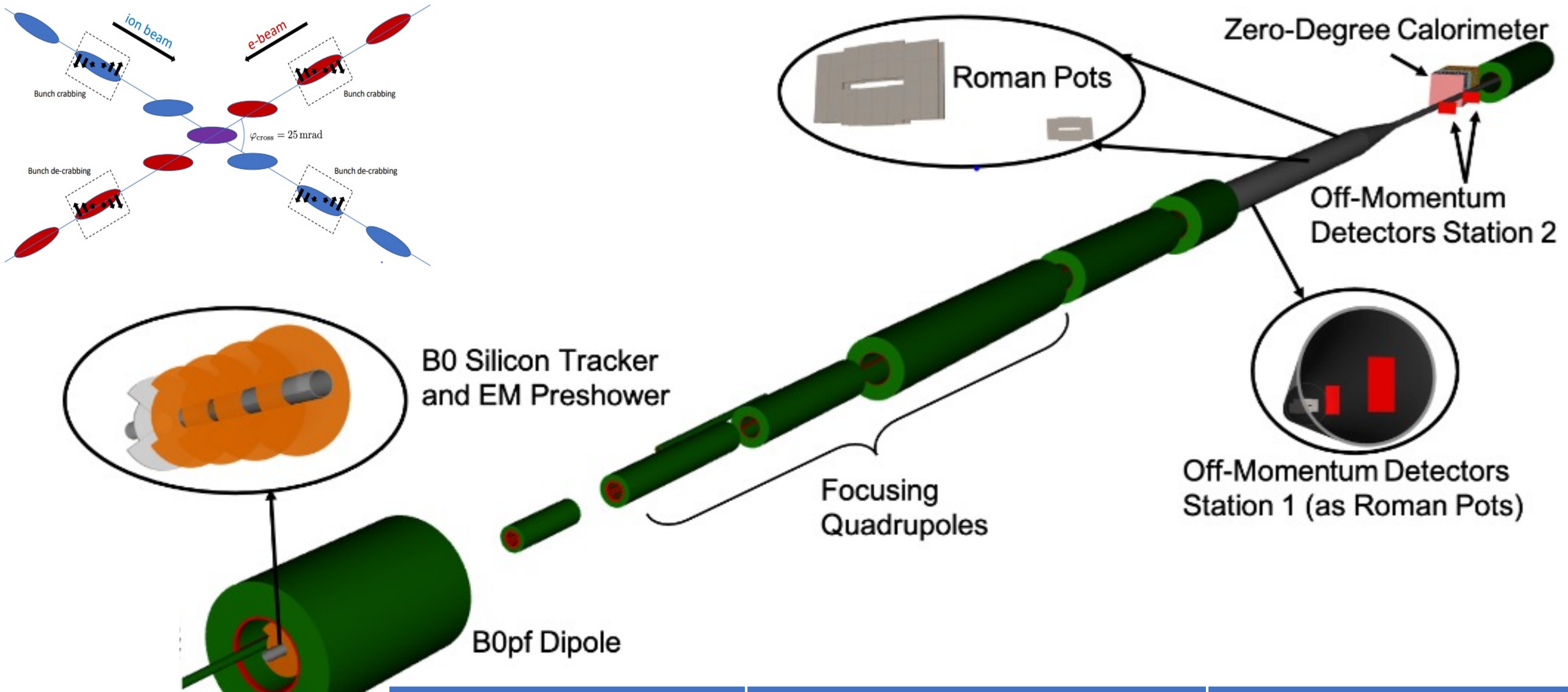
- Timing resolution: ~25 ps per hit
- Position resolution: ~30 μm with 500 μm pitch
- Material budget: ~8% X0
- Total area: ~ 15 m^2

TOF PID coverage

- ETTL: -3.7<η<-1.74   0.15 < p < 2.5 GeV
- FTTL: 1.5<η<3.5   0.15 < p < 2 GeV
- CTTL: |η|<1.4   0.15 < p_T < 1.5 GeV

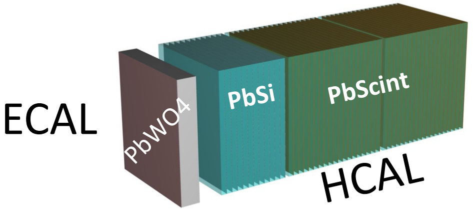
AC-LGADs in Forward Detectors: Timing + Tracking





Technologies defined

- Silicon: AC-LGAD & MAPS
- ZDC:
  - ECAL (PbWO4)
  - HCAL (PbSi + PbScint)



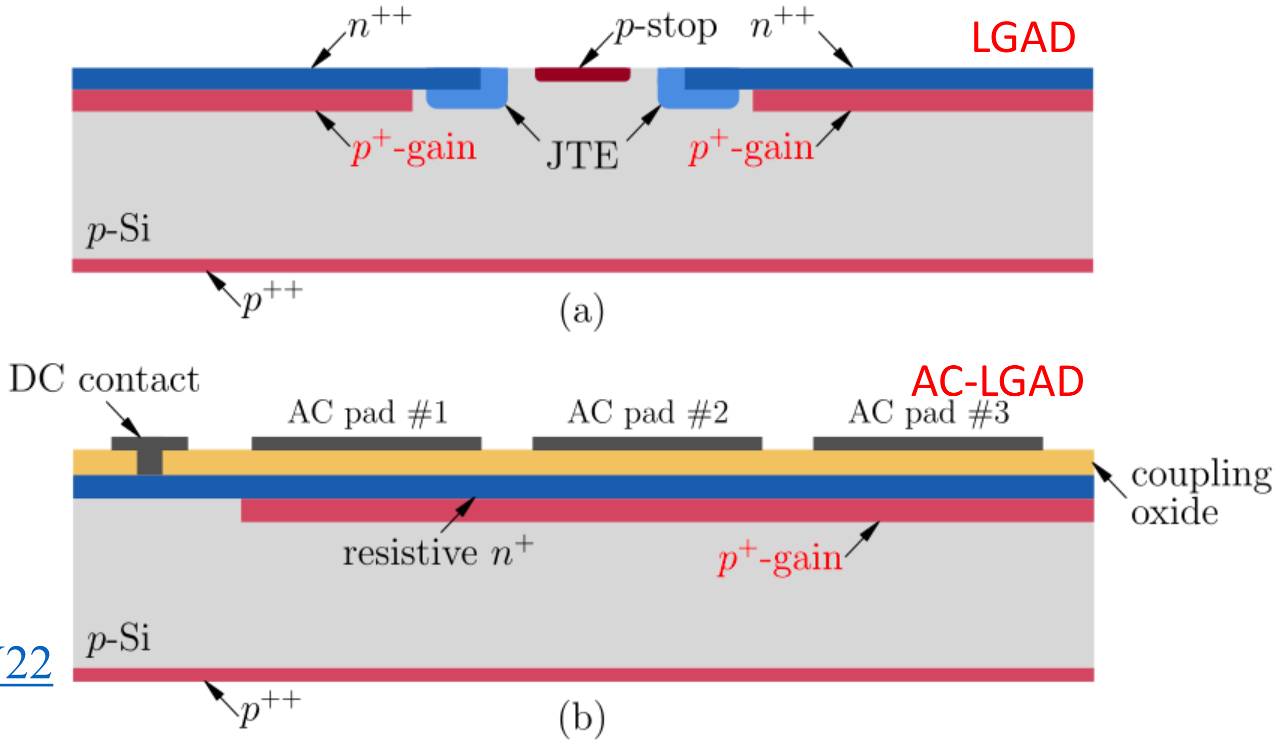
Detector	Angular accept. [mrad]	p_T coverage
ZDC @ ~30m	θ<5.5 (η > 6)	p_T<1.3 GeV
Roman Pots	0*<θ<5.0 (η > 6)	*Low p_T(t) cutoff (beam optics)
Off-Momentum Detectors	0.< θ < 5.0 (η > 6)	Low-rigidity particles from nuclear breakups
B0 forward spectrometer	5.5 < θ < 20.0 (4.6< η < 5.9)	High p_T(t)

eRD112: AC-LGAD R&D for EIC

- AC LGAD detectors proposed for EIC
  - TOF PID and tracking
  - Roman Pots and B0

- Have common designs in sensor, ASIC etc. when possible, combine R&D efforts [1]

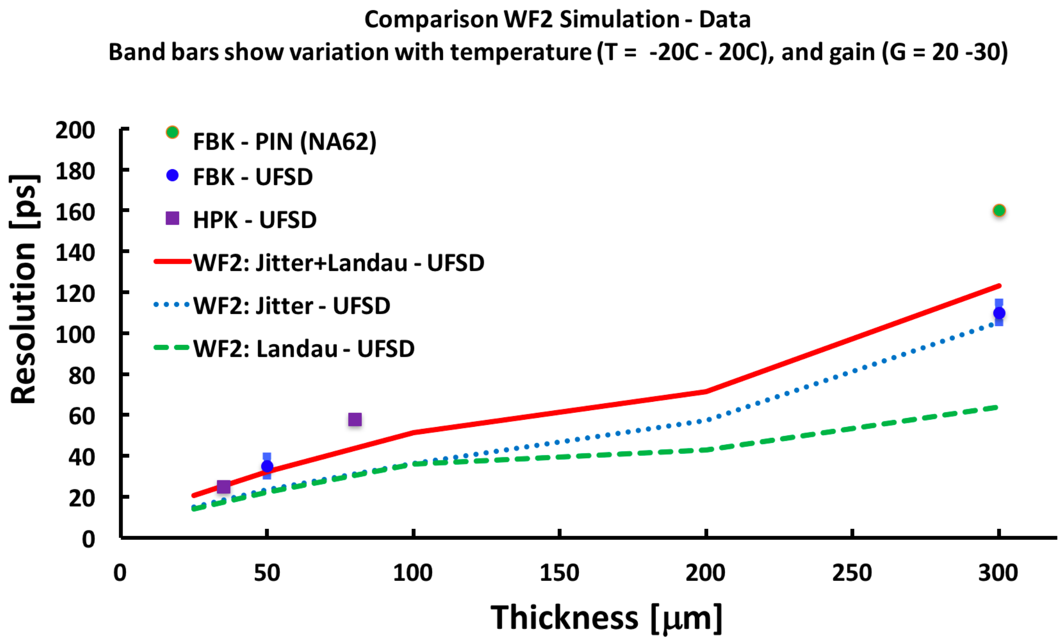
[1] https://wiki.bnl.gov/conferences/index.php/ProjectRandDFY22

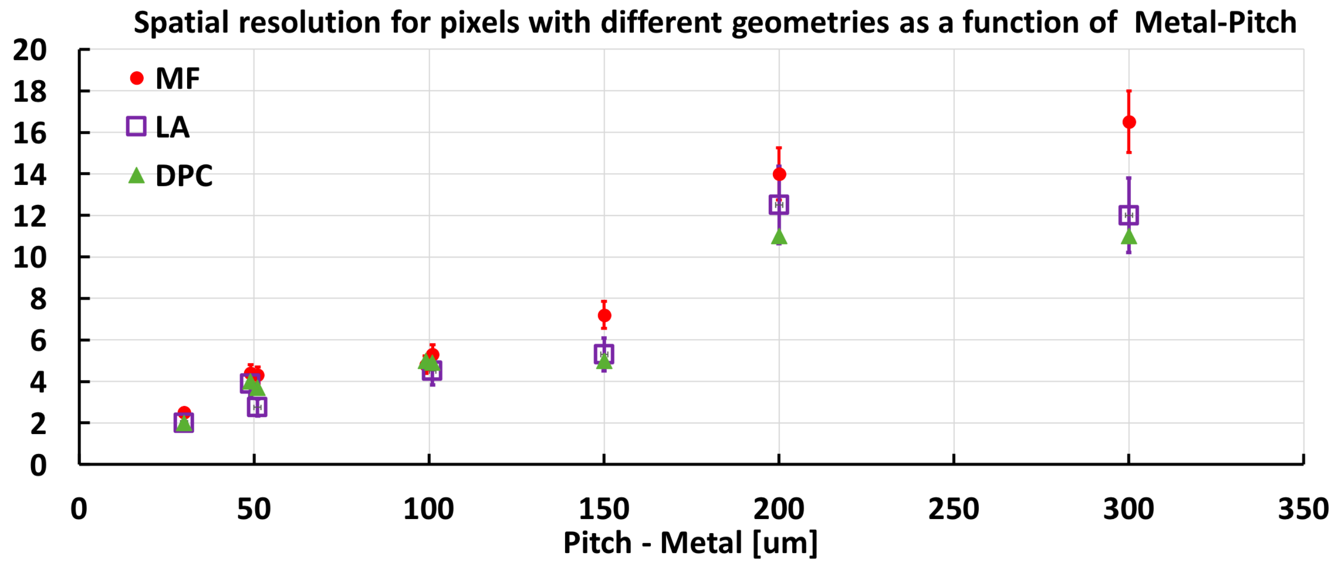


	Time resolution / hit	Position resolution / hit	Material budget / layer
Barrel ToF (Tracker)	<30 ps	(3-30 μm for Tracker)	$< 0.01\ X_0$
Endcap ToF (Tracker)	<25 ps	(30-50 μm for Tracker)	e-direction $< 0.05X_0$ h-direction $< 0.15X_0$
Roman Pots	<50 ps	$< 500/\sqrt{12}\ \mu m$	N/A
B0	<50 ps	$O(50)\ \mu m$	$< 0.01\ X_0$

eRD112: AC-LGAD Sensor R&D

Nicolo Cartiglia

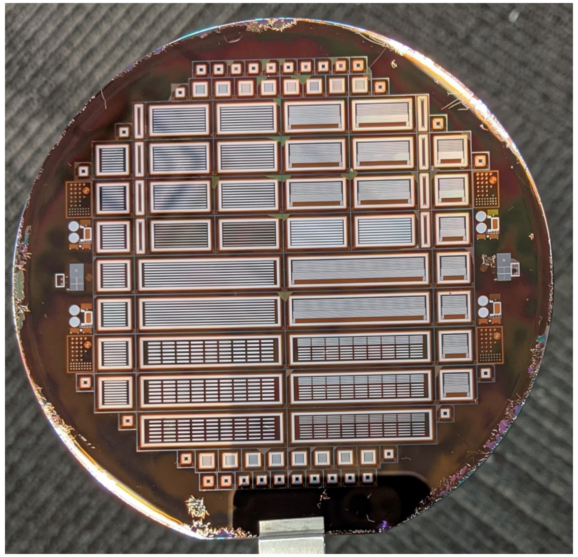




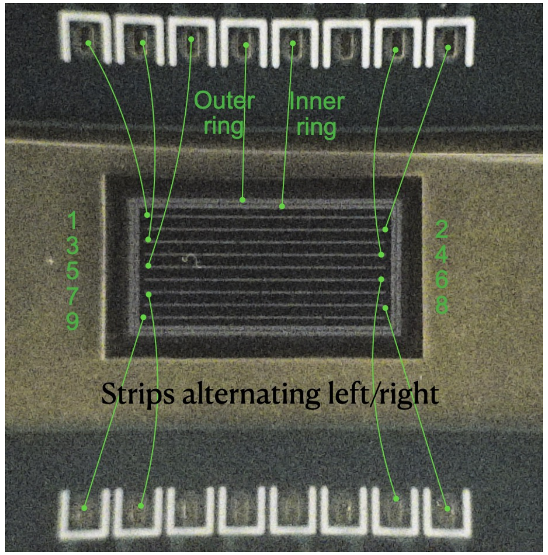
- **R&D Goals**
  - 15-20 ps timing resolution, O(3-50μm) position resolution where needed
  - Minimal readout channel density (long strip, rectangular pixel) for reduced power, material and cost
- **Plan**
  - Produce and test sensors with thinner active volume to achieve the desired timing resolution
  - Optimize implantation parameters and AC-pad segmentation through simulation and real device studies
  - Engage commercial vendors to improve fabrication process and yield

eRD112: AC-LGAD Sensor R&D

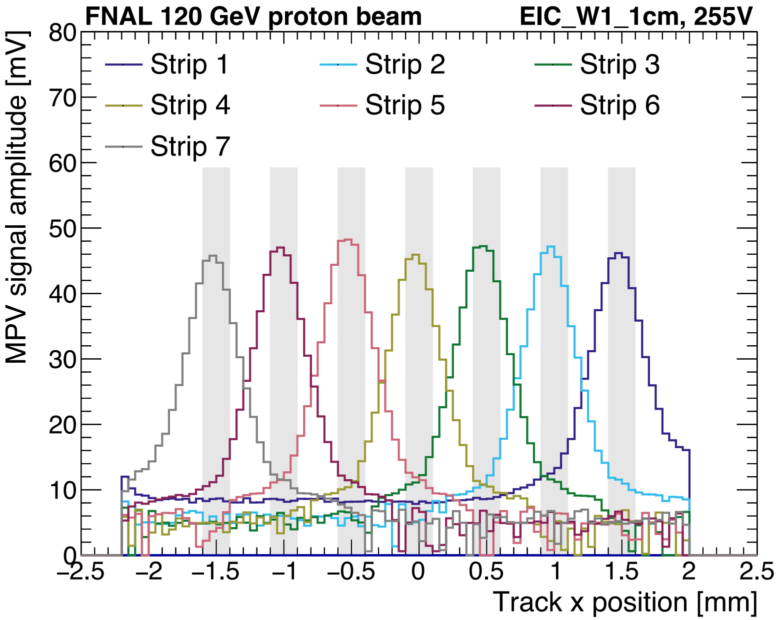
- **FY22**:
  - Production of thin (20 and 30 um) sensors for ToF application with time resolution ~20 ps by BNL IO.
  - Production of medium/large-area sensors with different doping concentration, pitch, and gap sizes between electrodes to optimize performance by BNL IO and HPK.
- **FY23 Q3**: Design and submission for fabrication of advanced sensor prototypes with <20 ps time resolution and space resolution that matches RPs, ToF, and Tracker requirements. This will be baseline for CD2/3A.
- **FY24 Q2**: Sensor batch submission with optimized sensor layouts and performance, based on laboratory and test-beam results. This sensor design will be used as baseline for the CD3 review.
- **FY25**: Module-size sensor fabrication with target time and space performance.



Strip AC-LGAD Sensor Wafer for EIC by BNL

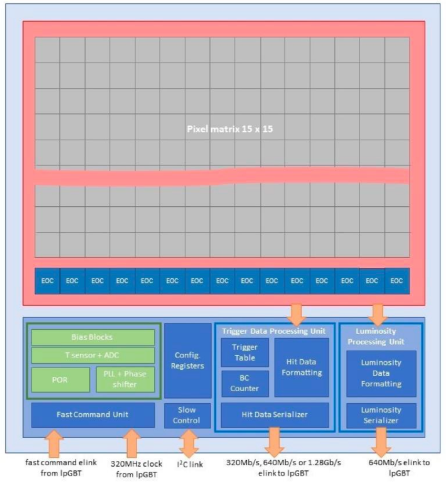


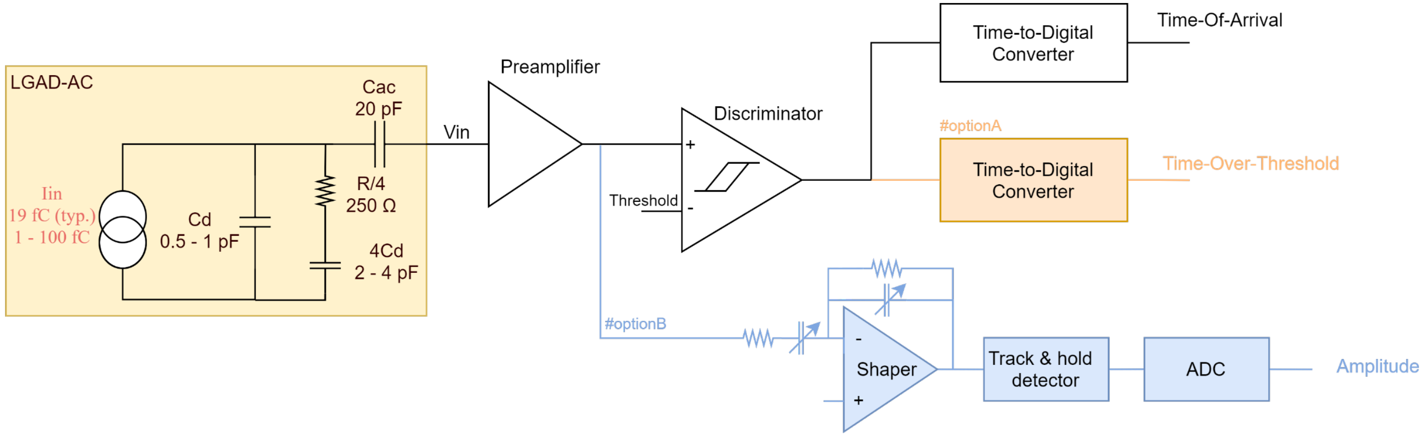
500 um*1cm strip AC-LGAD sensor mounted on test board



Signal amplitude vs x position at 2022 Fermilab test beam

eRD112: Frontend ASIC R&D





- **R&D Goal**
  - 15-20 ps jitter with minimal (1-2 mW/ch) power consumption, match AC LGAD sensors for EIC
- **Strategy**
  - Continue the ASIC prototyping effort for RPs by IJCLAB/Omega (1st submission in FY22 funded externally)
  - Utilize the design from ATLAS and CMS, and investigate common design for RP/B0 and ToF
- **Milestones**
  - **FY22 (funded externally):**
    - A first ASIC prototype that is compatible with EIC Roman Pot requirements and can read out an AC LGAD with ~500 um pitch and ~30 ps time resolution.
    - **Deliverable (Sept. 2022)**: A prototype ASIC design to readout AC LGADs using signal sharing across neighboring electrodes and has 30 ps time resolution with low power consumption.
  - **FY23 Q1**: 2nd prototype design and submission with better performance and extended features. Baseline for CD2 review.
  - **FY24 Q2**: 3rd ASIC submission, aiming to match ToF timing requirements. Baseline for the CD3 review.
  - **FY25**: Full-scale ASIC submission.

eRD112: Frontend ASIC R&D

EICROC0 (submitted in 3/2022) by Omega/Irfu/AGH

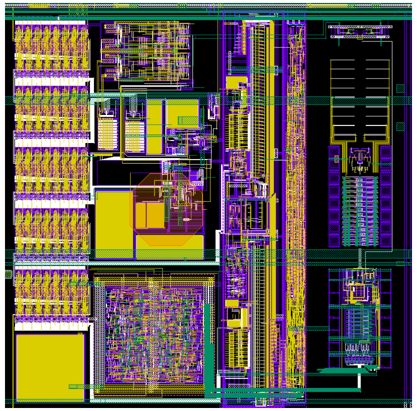
- Preamp, discri. taken from ATLAS ALTIROC
- I2C slow control taken from CMS HGCROC
- TOA TDC adapted by IRFU Saclay
- ADC adapted to 8bits by AGH Krakow
- Digital readout: FIFO depth8 (200 ns)

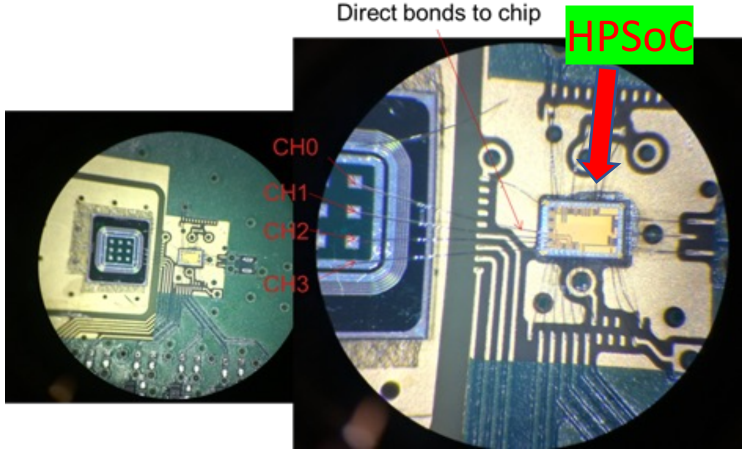
FCFD0 (submitted in 2021) at Fermilab

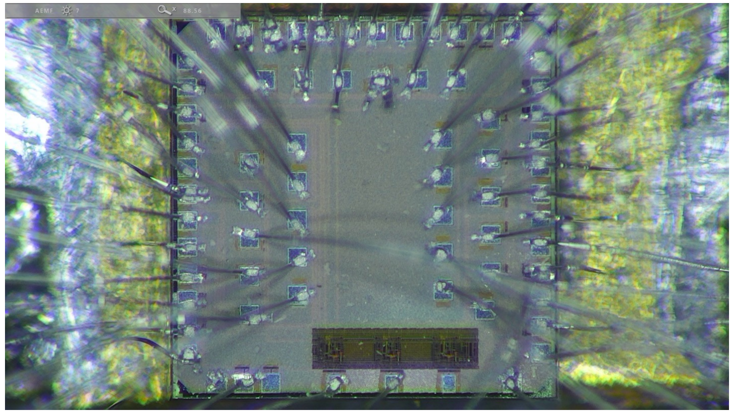
- Adapt the Constant Fraction Discriminator (CFD) principle in a pixel when a CFD is paired with a TDC, one time measurement gives the final answer.
- Charge injection consistent with simulations: ~30 ps at 5fC, and <10 ps at 30 fC, with LGAD like pulses
- Tests with beta sources and beam are planned

ASIC Efforts at UC Santa Cruz

Institution		Technology	Output	# of Chan	Funding	Specific Goals	Status
INFN Torino	FAST	110 nm CMOS	Discrim. & TDC	20	INFN	Large Capacitance TDC	Testing
NALU Scientific	HPSoC	65 nm CMOS	Waveform	5 (Prototype) > 81 (Final)	DoE SBIR	Digital back-end	Testing
Anadyne Inc	ASROC	Si-Ge BiCMOS	Discrim.	16	DoE SBIR	Low Power	Simulations, final Layout, Board design


EICROC0




FCFD0

Summary and Outlook

- **eRD112**: develop sensor, ASIC, and other key components for AC-LGAD detectors at EIC
  - **Continue sensor R&D, ramp up efforts on ASIC, start development of other components including mechanical structure, cooling, on- and off-detector electronics**
  - **Come up with preliminary system designs of AC-LGAD detectors for CD2/3A review (Oct 2023)**

  Mailing list: https://mailman.rice.edu/mailman/listinfo/lgads-eic
  Indico page: https://indico.bnl.gov/category/323/

- **AC-LGAD** is the selected technology by EIC Detector-1 for timing and tracking in central and far-forward detectors. Other fast timing technologies could be considered for Detector-2
  - **Opportunity**: new detector technology development; multi-million and multi-year projects.
  - **Challenge**: strict detector performance requirements; tight schedule.

Timeline – What is Coming for EIC

❑	CD-0 approval	December 19, 2019
❑	Community-wide Yellow Report effort	Dec 2019 – Feb. 2021
❑	CD-1 review (includes CDR)	January 26-29, 2021
❑	Call for Collaboration Proposals for Detectors	March 6, 2021
❑	CD-1 approval	June 29, 2021
❑	DOE/OPA Status Review	October 19-21, 2021
❑	Status Update to Federal Project Director	June 28-30, 2022
❑	Cost and Schedule Event(s)	May-June 2022
❑	Technical Subsystem Reviews	Jan. – Dec. 2022
❑	OPA Status Review	January 2023
❑	Preliminary Design Complete & Review	May 2023
❑	Final Design/Maturity Readiness for CD-3A Items	May 2023
❑	CD-2/3A review (expectation), requires pre-TDR	~October 2023
❑	CD-2/3A (expectation)	~January 2024
❑	CD-3 review (expectation)	~January 2025
❑	CD-3 (expectation), requires TDR	~April 2025

TOF WG Mailing list: eic-projdet-tofpid-l@lists.bnl.gov Indico page: https://indico.bnl.gov/category/414
FF WG Mailing list: eic-projdet-FarForw-l@lists.bnl.gov Indico page: https://indico.bnl.gov/category/407

- **Everyone is VERY welcome to join eRD112, TOF and/or Far-forward working groups**