

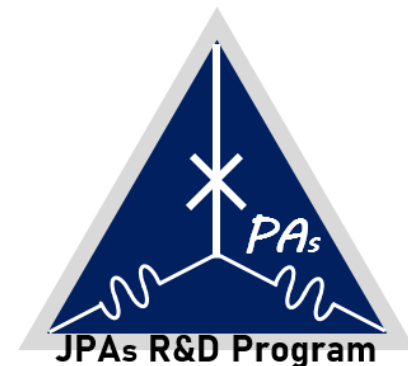
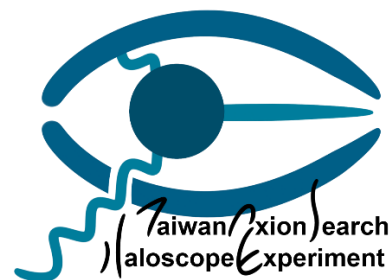
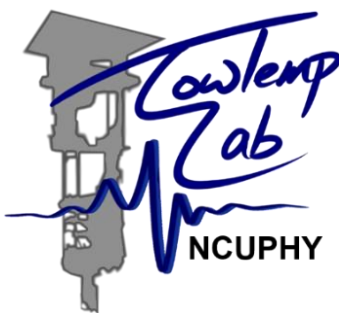
Development of JPAs for Axion Search in TASEH

洪偉晟 (Wei-Cheng Hung), TASEH Collaboration

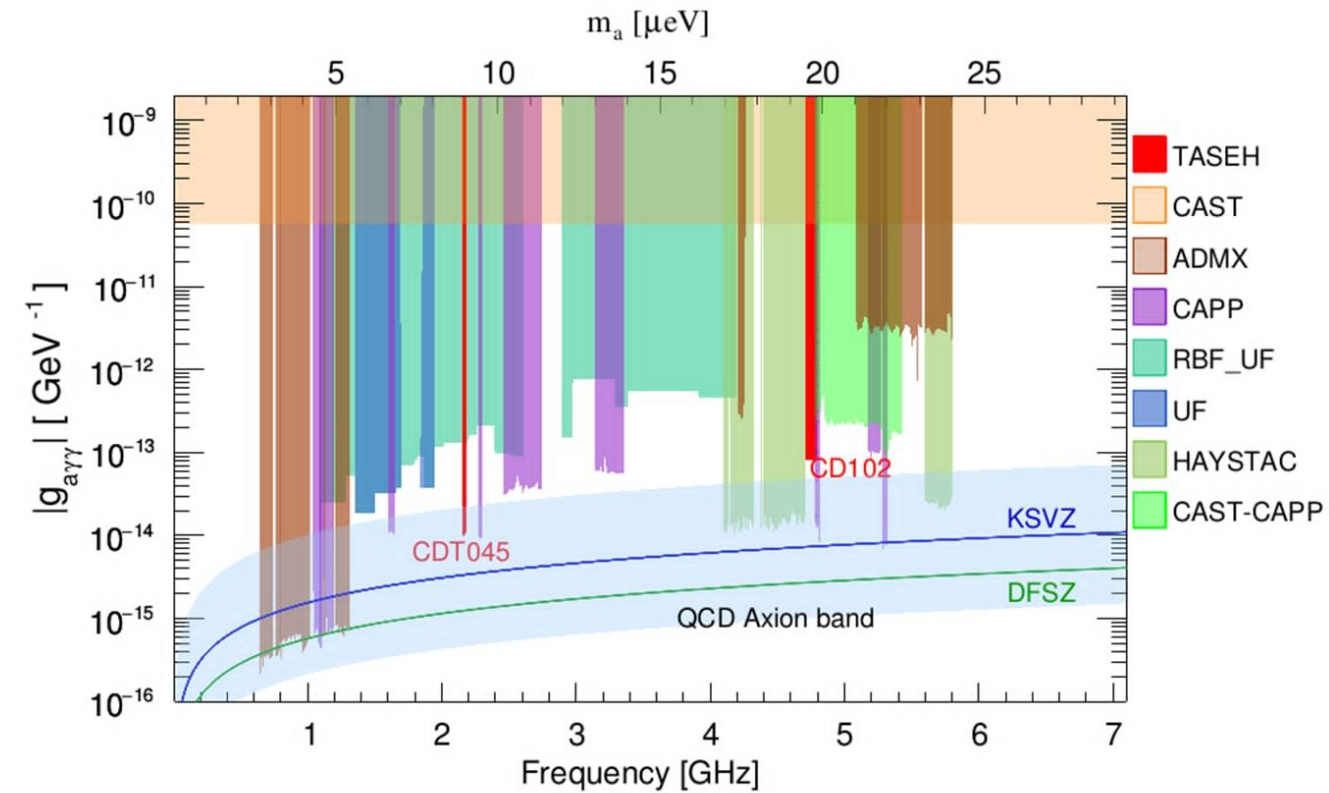
Advisor : 陳永富(Yung-Fu Chen), 張元翰(Yuan-Hann Chang)

JPAs team ,Low Temperature Physics Lab, NCU

Taiwan Axion Search Experiment with Haloscope, NCU



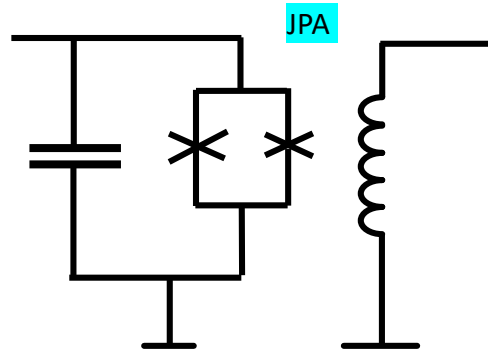
Progress Over the Past Years



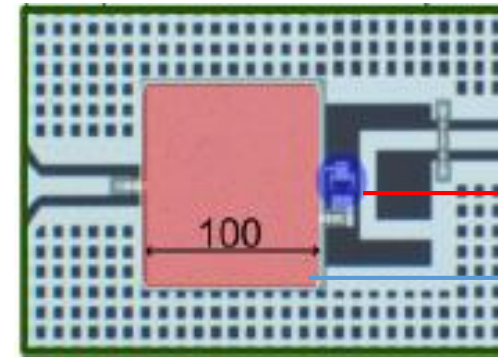
Parameter	CD102	CDT045
m_a (μeV)/ f_c (GHz)	19.47 – 19.84/ 4.71 – 4.80	8.93 – 9.02/ 2.156 – 2.180
T_{sys} (mK)	2300	350
η	0.69	0.67
B (Tesla)	7.8	6
V (L)	0.23	4
C	0.67	0.46
Q_L	2.0×10^4	6×10^3
$ g_{a\gamma\gamma}/g_{a\gamma\gamma}^{KSVZ} $	11	3.5

JPA Devices Integrated into CDT045

Lumped Element JPA



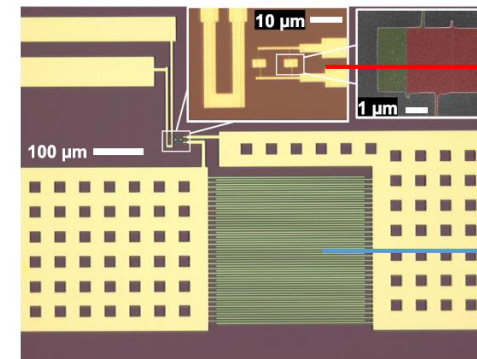
- **LJPA (Mutus)**
 - 20dB Gain
 - SQL system noise
 - 50MHz BW
 - -115dBm saturation power
 - citation 108
- Appl. Phys. Lett. 103, 122602 (2013)



SQUID
Parallel Capacitor

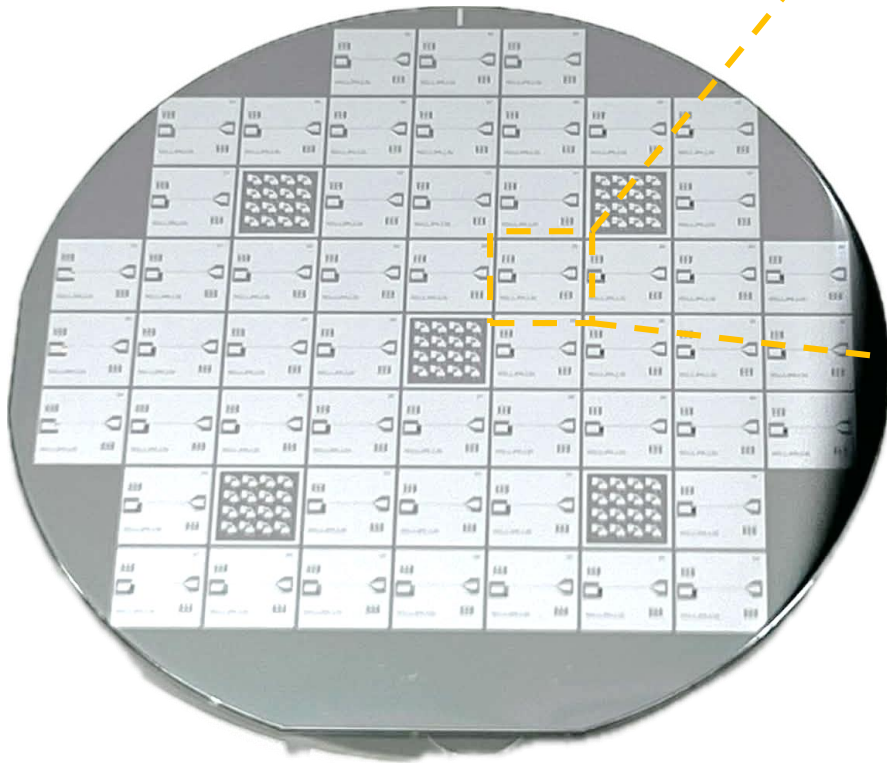
LC Circuit	Linear C/L
Nonlinear Element	Josephson Junction/ SQUID
Pump Feed line	3WM pump line

- **LJPA (Elo)**
 - 20dB Gain
 - SQL system noise
 - 100MHz BW
 - -125dBm saturation power
 - citation 14
- Appl. Phys. Lett. 114, 152601 (2019)

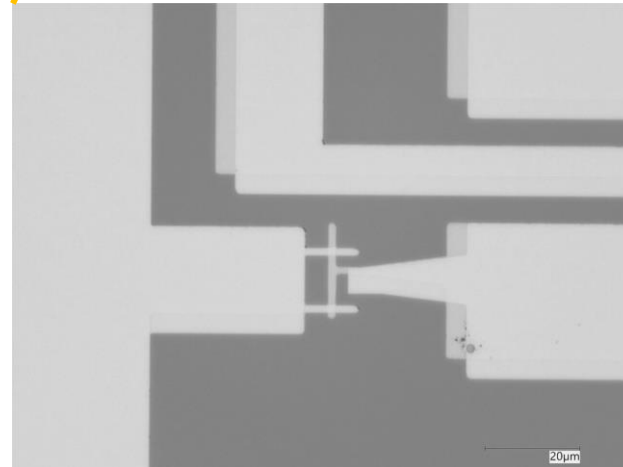
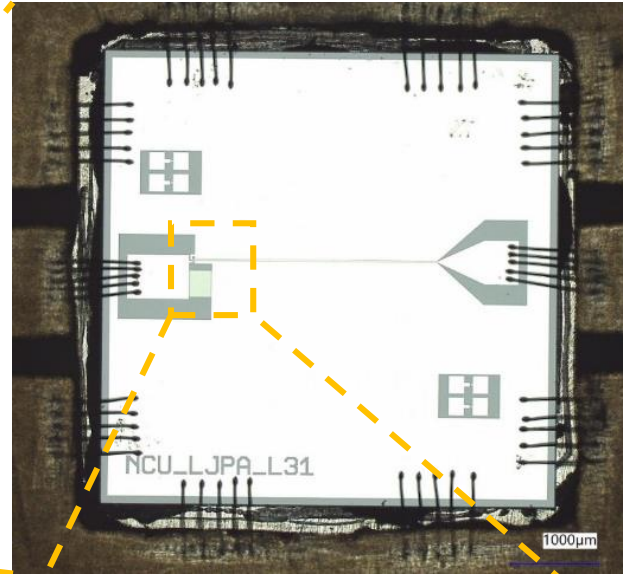


SQUID
interdigit Capacitor

JPA devices produced in TASEH



Single optical lithography process.

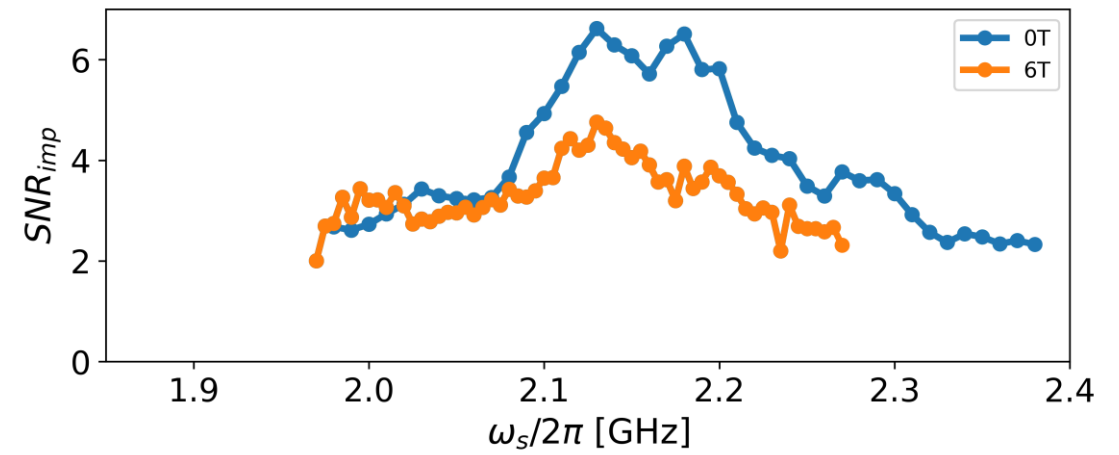
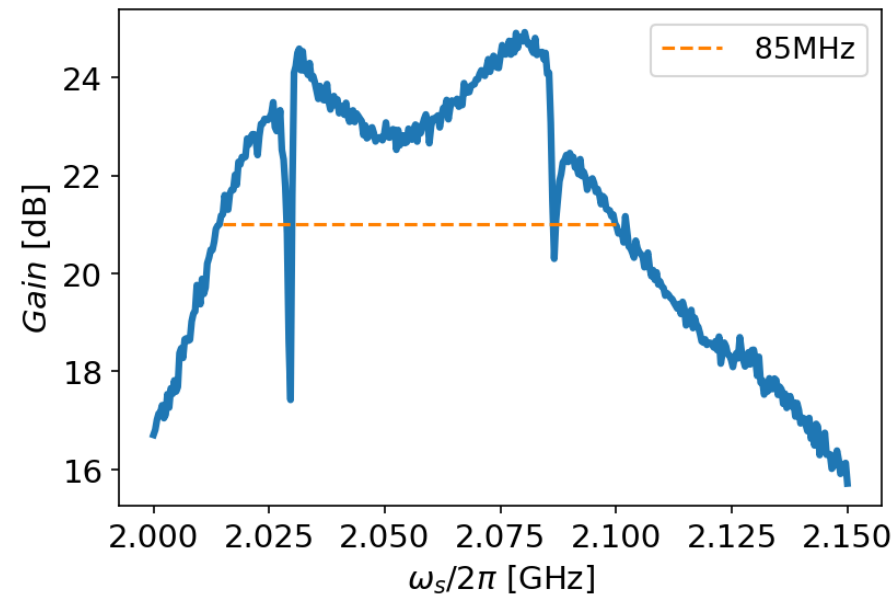
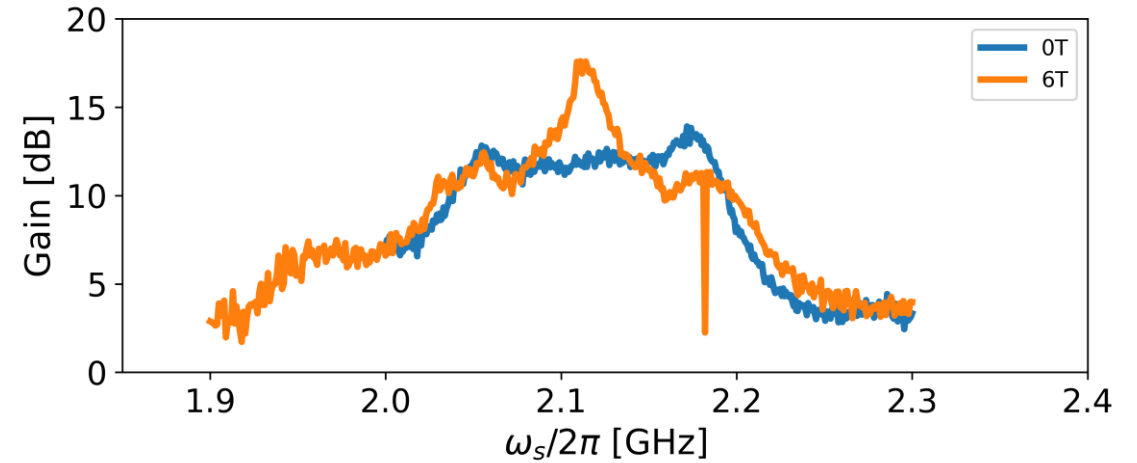
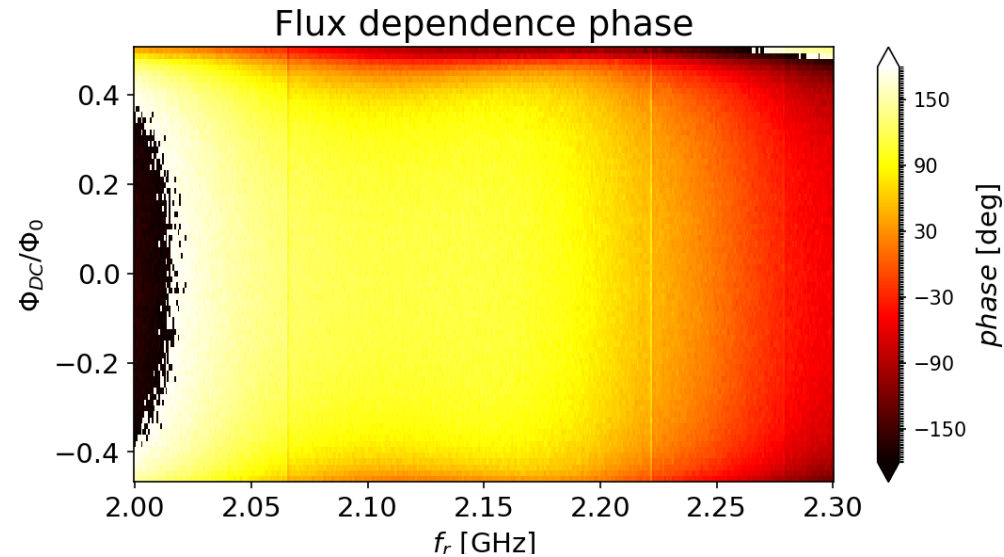


um-JJs compatible of the i-line masker aligner.

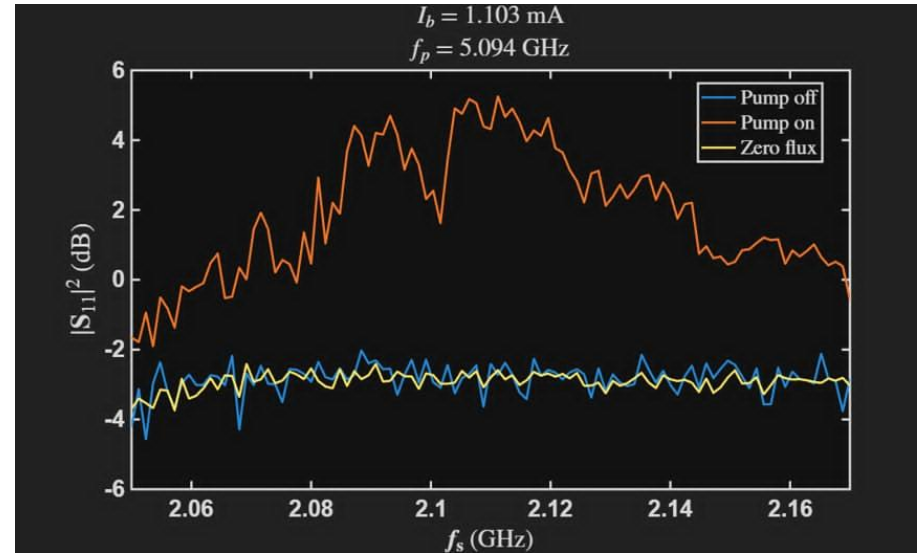
Features

- LJPA version :
low Q for few ten MHz bandwidth
- Interdigital capacitor :
compatible for single lithography
- um-JJs :
Overcoming the E-Beam Exposure Bottleneck
- optical lithography:
Compatible for heavily production (4', 8'..etc)
- single optical lithography:
Enhancing the device yield

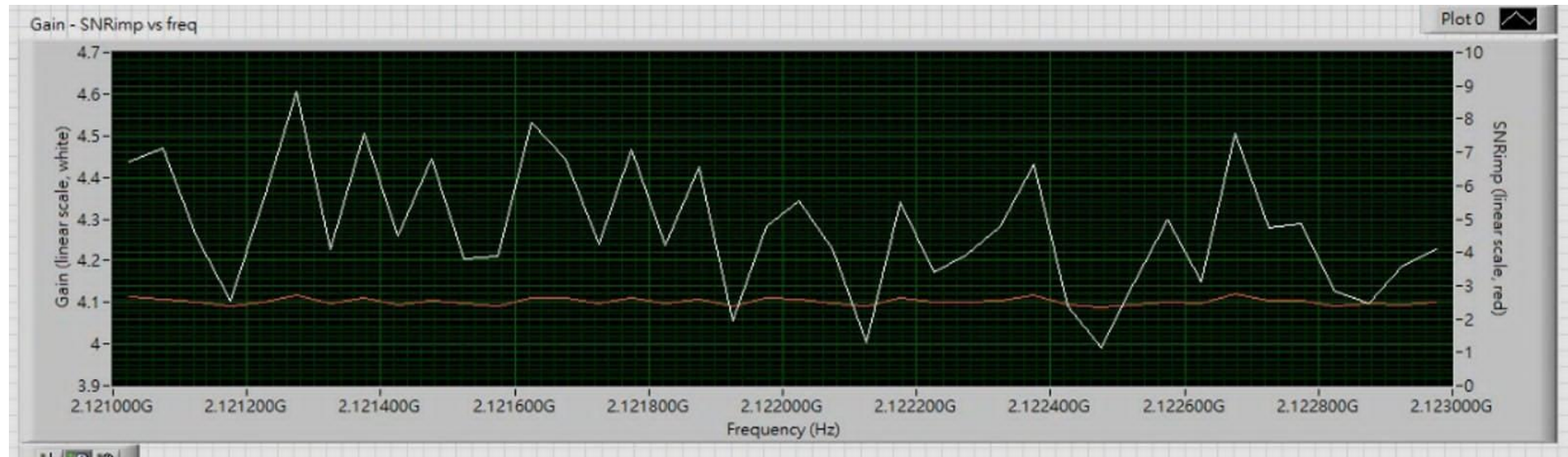
Device Characteristics



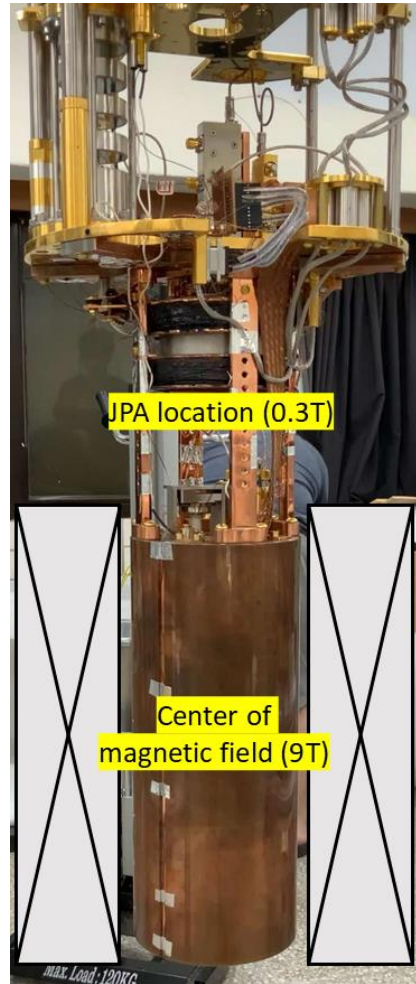
The Coming data taking run (CDT055)



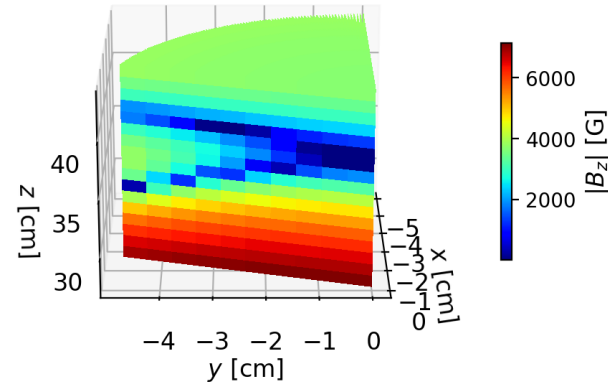
Gain~8dB
SNR_imp~3.5



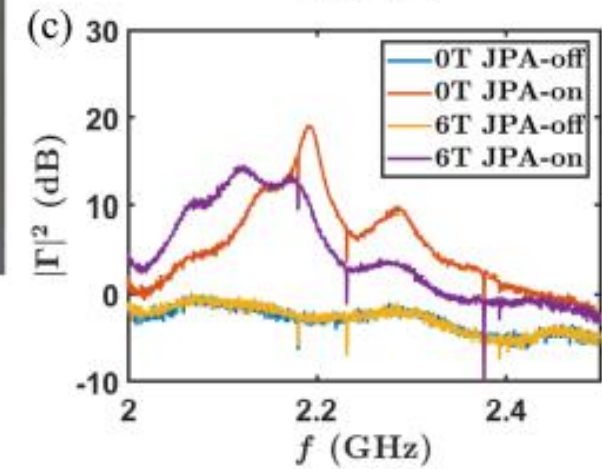
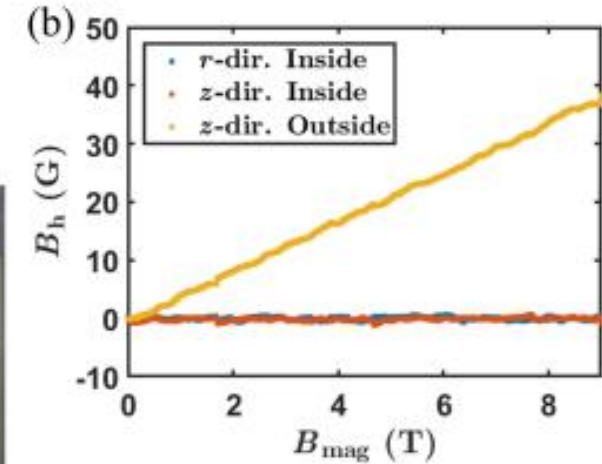
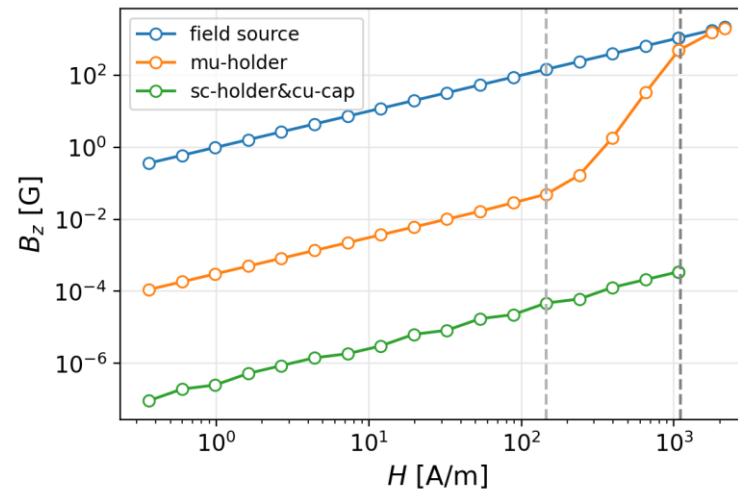
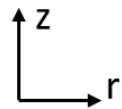
Superconducting Shielding



Center of the MX plate ($z=40, r=0$)

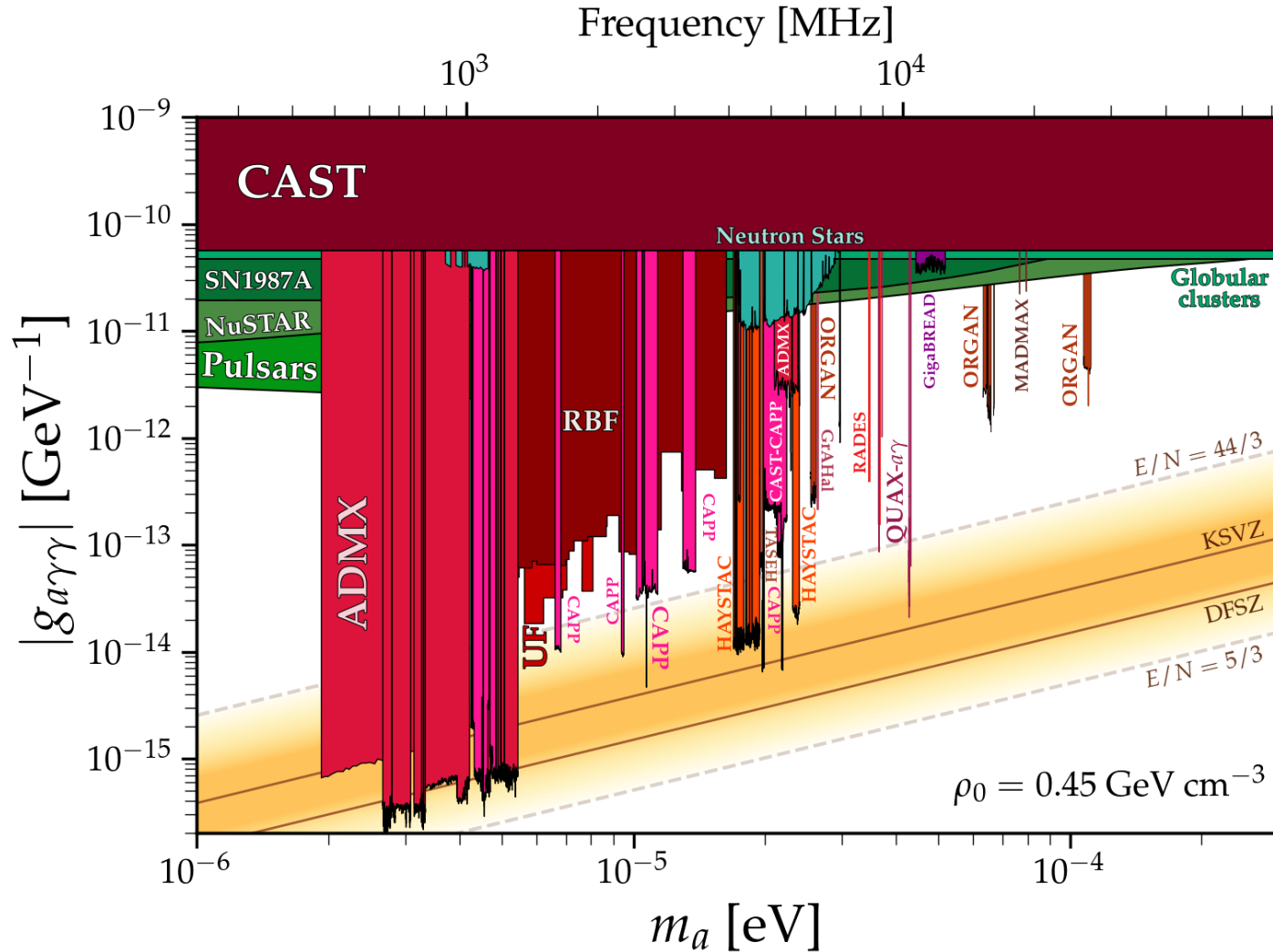


Center of the cavity ($z=0, r=0$)



Although magnetic shielding is in place, the JPA gain and noise performance are still affected when the magnet is turned on. (next session 羿翔 will update the result.)

JPA Development Roadmap in the TASEH



A single-layer optical lithography process was adopted as a rapid fabrication strategy for the initial development of the devices.

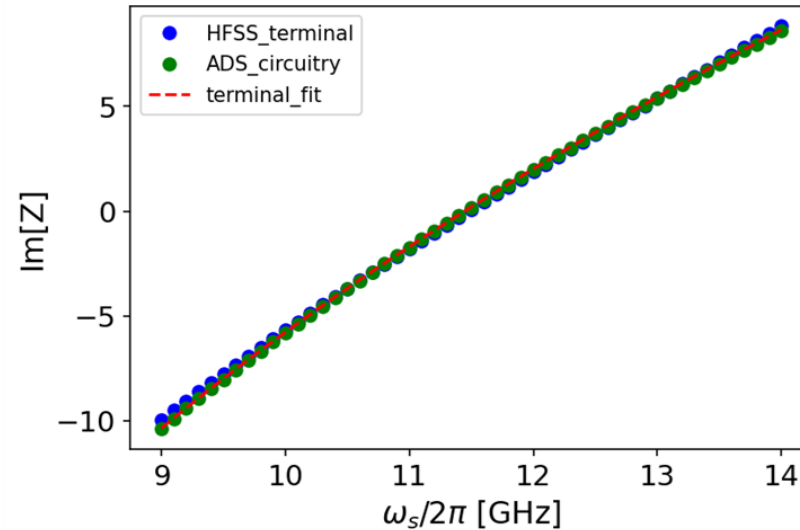
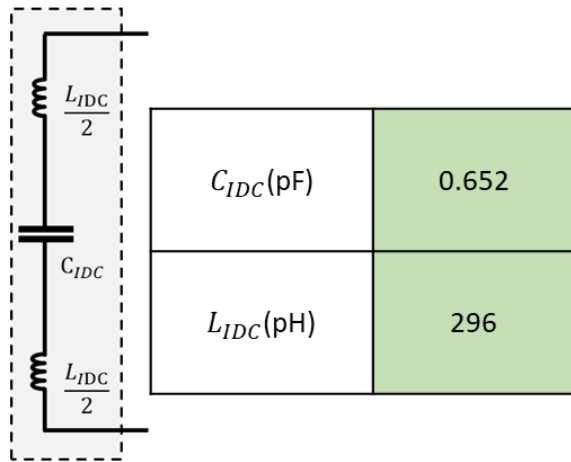
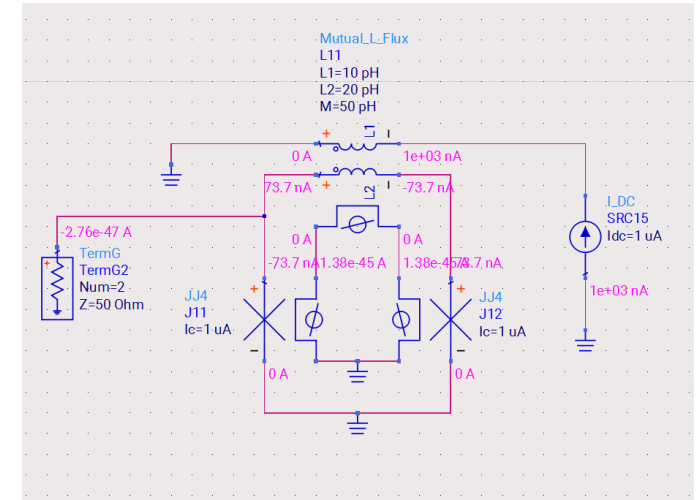
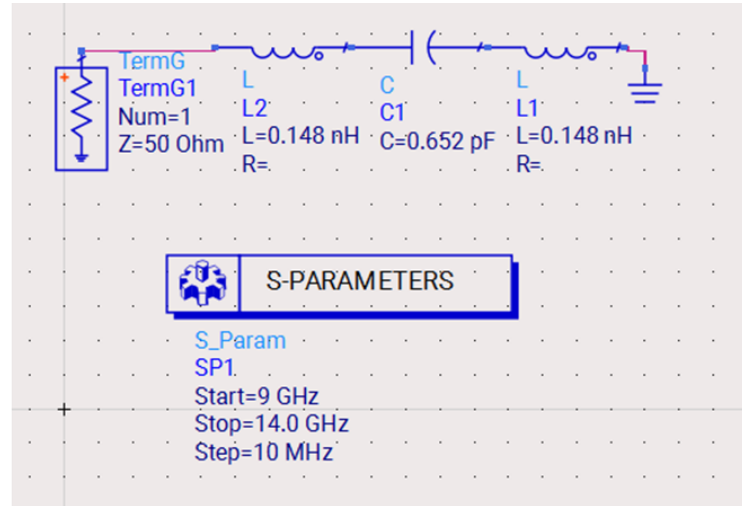
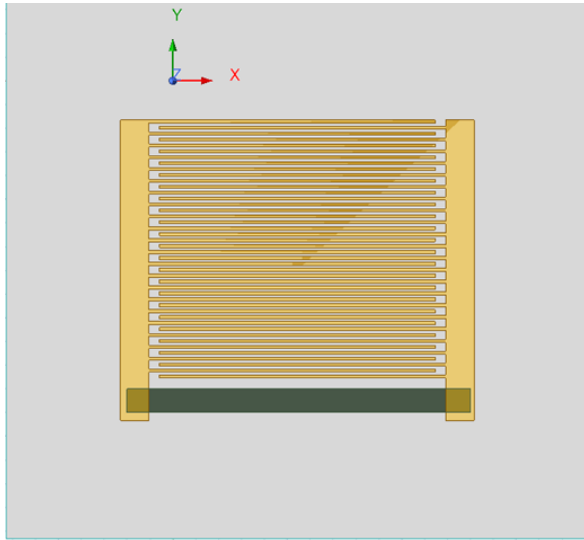
Device Development

1. Multi-frequency JPA devices
2. Wide-bandwidth JPA devices
3. High-saturation-power JPA devices

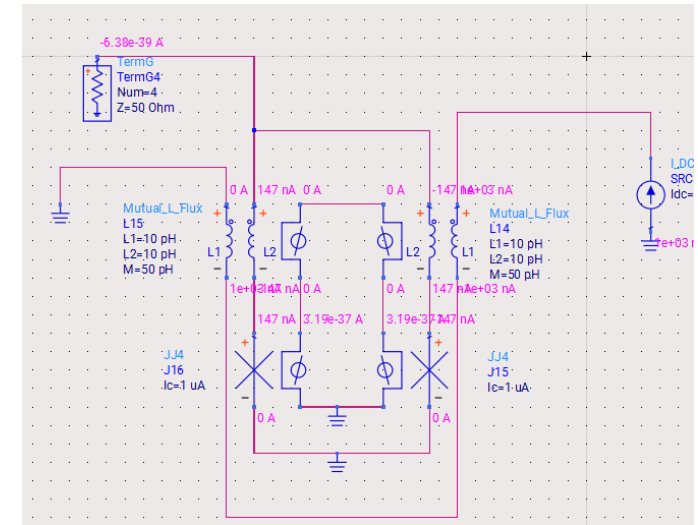
Technology Development

1. EDA and FEM simulation tools for device design
2. Multilayer fabrication processes

Building the Element Modules



IDC module in HFSS and ADS



ADS SQUID conformation

Incorporate with the Keysight Advance Design Simulator (ADS) and ANSYS desktop

Multilayer Fabrication

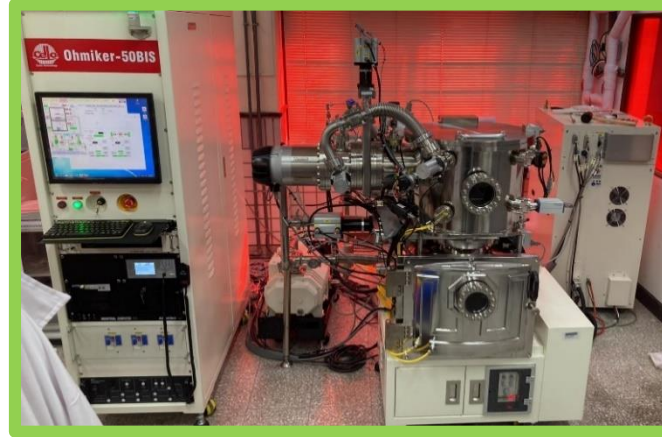
2' wafer / coupon chips(in dev.)

Most of them are in-lab tools



Lithography System

NANYTE beam Mk2 (NCU)



Al PVD System

OhmMiker-50BIS (NCU)



Dielectric deposition/etching

T19/ E11 (TSRI)



Wet Bench

--(NCU)

> 4' inch wafer (under dev.)

C09	BEOL 8" WET BENCH	Mr. Liu Ms. Peng	7699 7714	C09-A	C09-B	C09-C	C09-D	C09-E	C09-F	B2
L32	I-line Stepper($\leq 8"$)	Mr. Hsu Mr. Chang	7648 7535	L32_A			L32_D	L32_E		B2

Taiwan Semiconductor Research Institute(TSRI) offers the continuous manufacturing & high reliable fabrications.

Broadband Lumped-Element JPA With Optical Lithography

Publisher: **IEEE**

[Cite This](#)

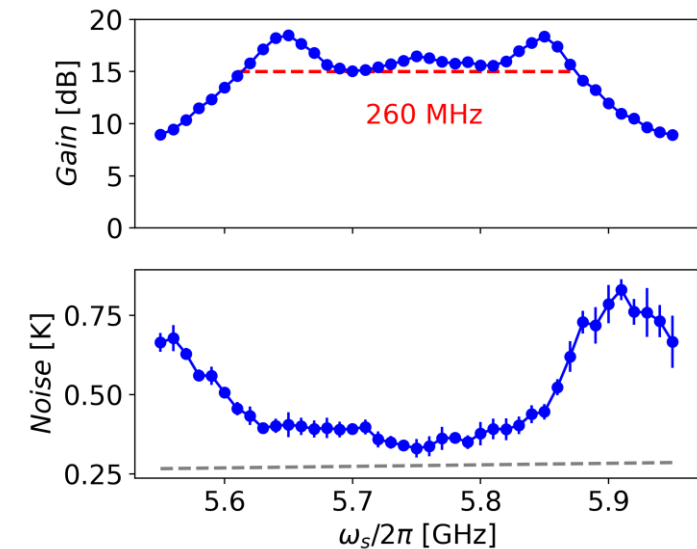
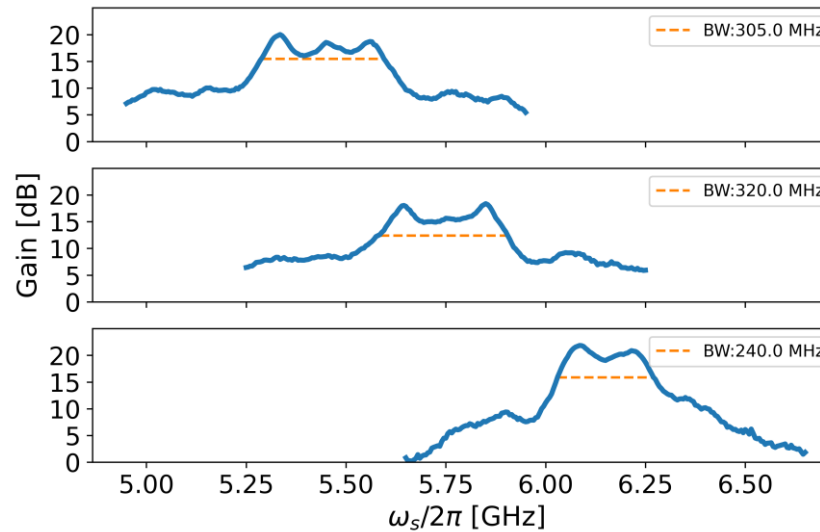
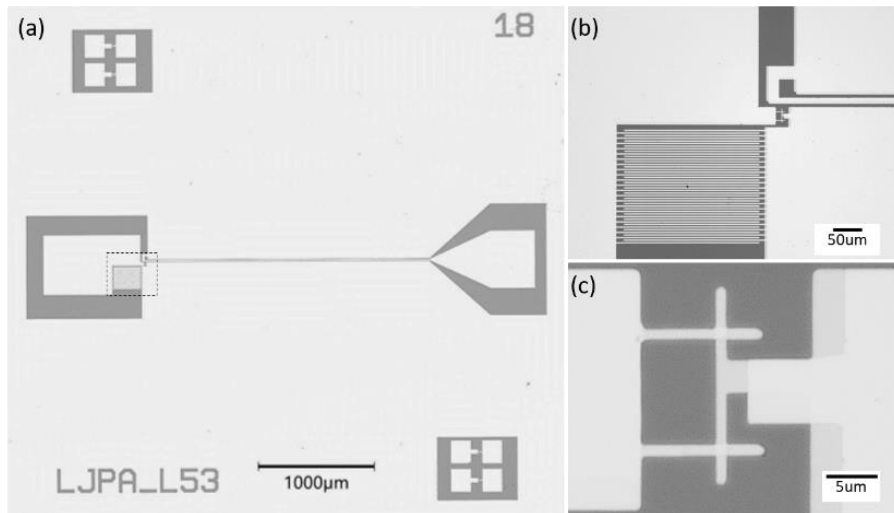
[PDF](#)

[Wei-Cheng Hung](#) ; [Jing-Yang Chang](#) ; [Yu-Hsuan Hung](#) ; [Yu-Chiun Chiu](#) ; [Ssu-Yu Liu](#) ; [Ting-Wei Hu](#) All Authors

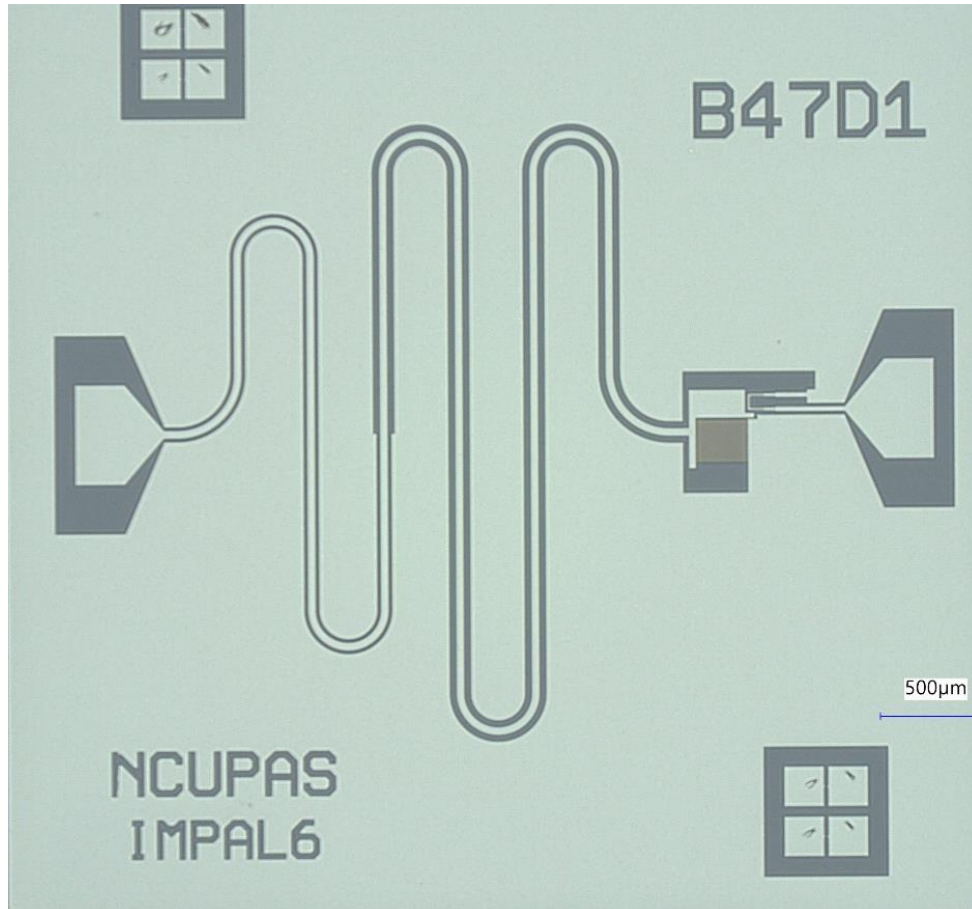
92

Full

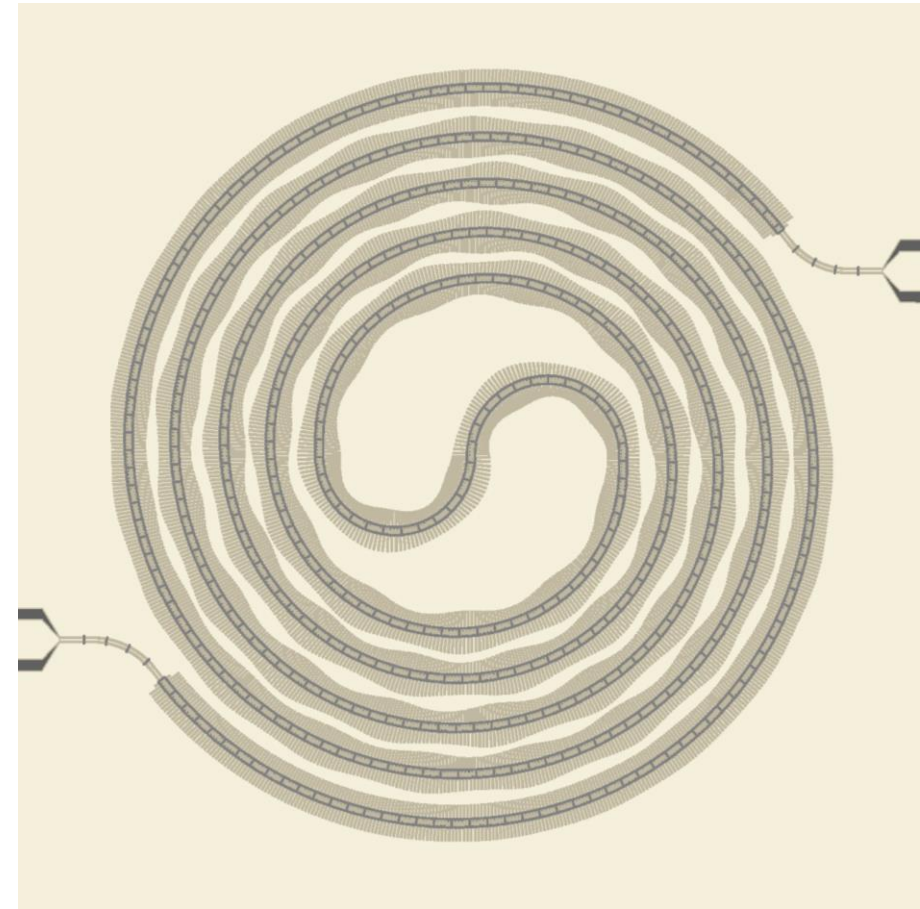
Text Views



Wide-bandwidth JPA devices



Impedance Matching Parametric Amplifier (in dev.)



Traveling Wave Parametric Amplifier (in dev.)